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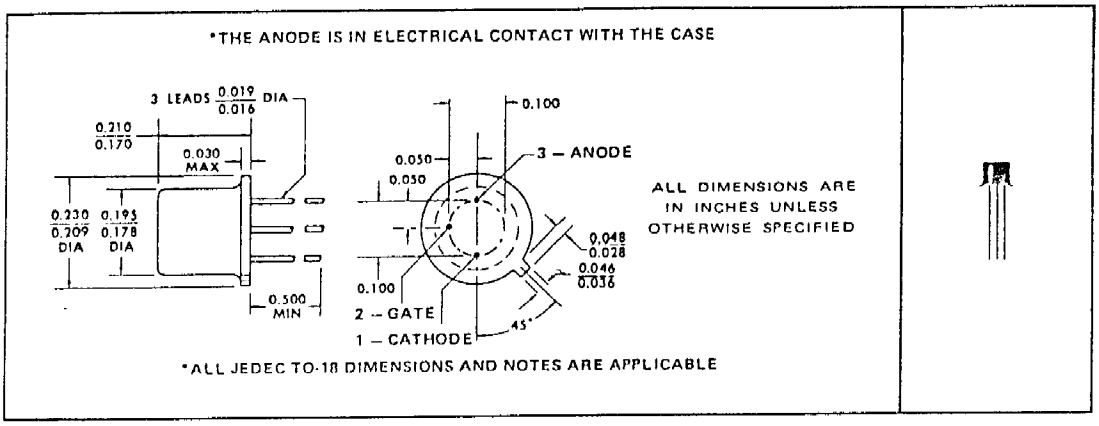
2N3004

P-N-P-N PLANAR SILICON REVERSE-BLOCKING TRIODE THYRISTOR

mechanical data

The devices are in a hermetically sealed welded case with a glass-to-metal seal between case and leads. Approximate weight is 0.35 grams.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	2N3004	UNIT
*Static Off-State Voltage, V_D (See Note 1)	200	V
*Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	200	V
*Static Reverse Voltage, V_R (See Note 2)	200	V
*Repetitive Peak Reverse Voltage, V_{RRM} (See Note 2)	200	V
*Continuous or RMS On-State Current at (or below) 55°C Free-Air Temperature (See Note 3)	350	mA
*Average On-State Current (180° Conduction Angle) at (or below) 55°C Free-Air Temperature (See Note 4)	250	mA
*Surge On-State Current (See Note 5)	6	A
Peak Negative Gate Voltage	8	V
*Peak Positive Gate Current (Pulse Width < 8 ms)	250	mA
*Average Gate Power Dissipation	100	mW
*Operating Free-Air Temperature Range	−65 to 150	°C
*Storage Temperature Range	−65 to 200	°C
*Lead Temperature 1/16 Inch from Case for 10 Seconds	300	°C

NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} \leq 1\ k\Omega$.
2. These values apply when the gate-cathode resistance $R_{GK} \leq \infty$.
3. This value applies for continuous d-c or single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C, derate according to Figure 1.
4. This value may be applied continuously under single-phase, 60-Hz, half-sine-wave operation with resistive load. Above 55°C, derate according to Figure 1.
5. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_D	Static Off-State Current	V_D = Rated V_D, R_{GK} = 1 kΩ					0.1	μA
		V_D = Rated V_D, R_{GK} = 1 kΩ,		T_A = 150°C			100	
I_R	Static Reverse Current	V_R = Rated V_R, R_{GK} = ∞					0.1	μA
		V_R = Rated V_R, R_{GK} = ∞,		T_A = 150°C			100	
I_G	Gate Current	V_G = −5 V,	I_A = 0				−5	μA
I_{GT}	Gate Trigger Current	V_{AA} = 5 V,	R_L = 12 Ω,	$t_{p(g)} \geq 10\ \mu s$		5	20	μA
V_{GT}	Gate Trigger Voltage	V_{AA} = 5 V,	R_L = 12 Ω,	$t_{p(g)} \geq 10\ \mu s$, T_A = −65°C			0.9	V
		V_{AA} = 5 V,	R_L = 12 Ω,	$t_{p(g)} \geq 10\ \mu s$	0.55		0.7	
		V_{AA} = 5 V,	R_L = 12 Ω,	$t_{p(g)} \geq 10\ \mu s$, T_A = 150°C	0.2			
I_H	Holding Current	R_{GK} = 1 kΩ,	R_L = 2 kΩ			1.2	3	mA
		R_{GK} = 1 kΩ,	R_L = 2 kΩ,	T_A = −65°C			4	
V_T	On-State Voltage	I_T = 350 mA,	$R_{GK} \geq 1\ k\Omega$,	See Note 6			1.2	V
dv/dt	Critical Rate of Rise of Off-State Voltage	V_D = 1 V				400		V/μs

NOTE 6: The initial instantaneous value is measured using pulse techniques. On-state pulse width = 300 μs, PRR = 100 pps.

*JEDEC registered data