National Semiconductor

NMC87C257
262,144-Bit (32K x 8) CMOS EPROM with On-Chip Address Latches

General Description

The NMC87C257 is a CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC87C257 has latched addresses for direct interfacing with address/data multiplexed microprocessors and microcontrollers. The A0–A7 pins can be tied to the respective O0–O7 pins and then bused to the microprocessor or microcontroller directly. No latch device is needed for interfacing.

The part is designed to operate with a single +5V power supply with ±10% tolerance.

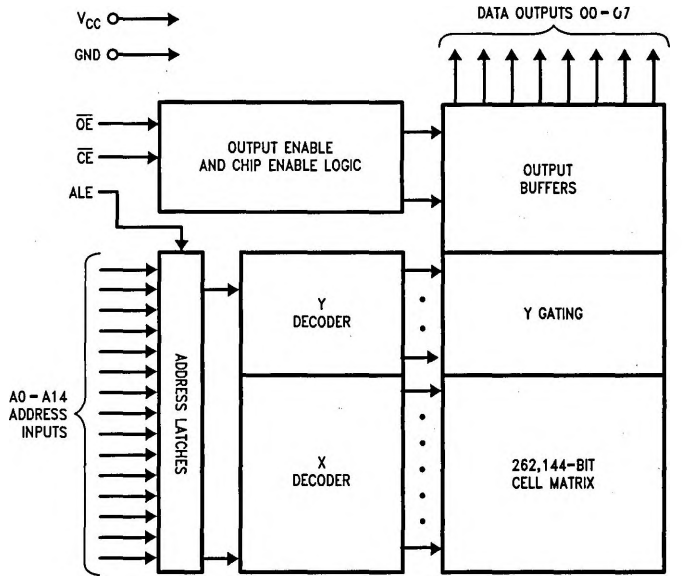
The part is packaged in a 28-pin dual-in-line package with a quartz window or PLCC. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure. The PLCC is not erasable.

This EPROM is fabricated with National's proprietary CMOS double-poly silicon gate technology.

Features

- Address latches for direct interfacing with address/data multiplexed microprocessors
- Low CMOS power consumption:
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Pin compatible with standard 256K EPROM
- Fast and reliable programming
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control use NMC27C256B PGM Algorithm
- High current CMOS level output drivers

Block Diagram



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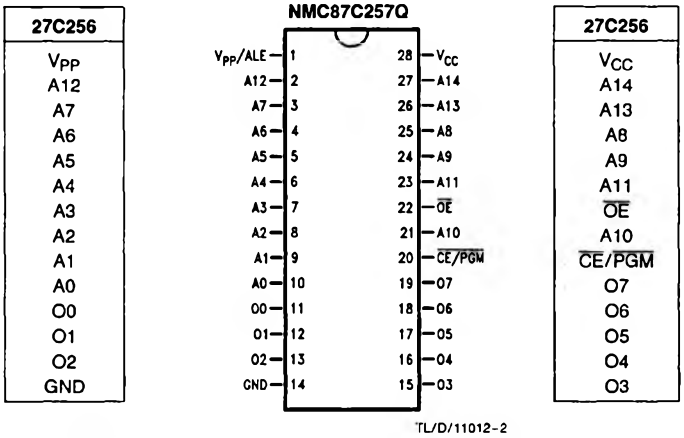
Connection Diagram



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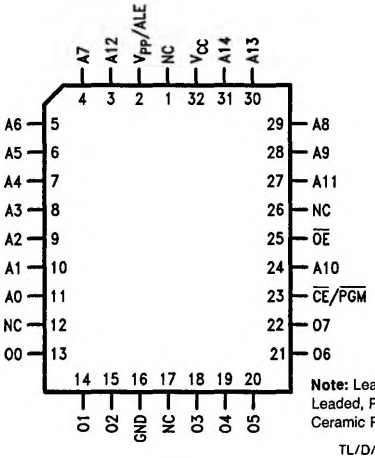
Note: Socket compatible 27C256 EPROM pin configuration is shown in the block adjacent to the NMC87C257 pins.

Pin Names

Symbol	Description
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
ALE	Address Latch Enable
V_{PP}	Programming Supply
V_{CC}	Power Supply
GND	Ground
NC	No Connection

PLCC Pin Configuration



Note: Leadless or Leaded, Plastic or Ceramic Package

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Top

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC87C257Q150, V150	150
NMC87C257Q200, V200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC87C257QE150	150
NMC87C257QE200	200

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature under Bias	−65°C to +150°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltages with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 with Respect to Ground (Note 2)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 2)	V_{CC} + 1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 Seconds)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	1700V

Operating Conditions (Note 3)

V_{CC} Power Supply	5V ±10%
Temperature Range	
Commercial	0°C to +70°C
Extended	−40°C to +85°C

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current		$V_{IN} = V_{CC}$ or GND		0.01	1.0	μA
I_{LO}	Output Leakage Current		$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1.0	μA
I_{CC1} (Note 4)	V_{CC} Current (Active) TTL Inputs		ALE = V_{IH}, f = 5 MHz All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 4)	V_{CC} Current (Active) CMOS Inputs		ALE = V_{CC}, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	Switching	$\overline{CE} = V_{IH}$, ALE = V_{IH}		10	12	mA
		Stable	$\overline{CE} = V_{IH}$, ALE = V_{IL}		0.3	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	Switching	$\overline{CE} = V_{CC}$, ALE = V_{CC}		8	10	mA
		Stable	$\overline{CE} = V_{CC}$, ALE = GND		0.5	100	μA
I_{PP}	V_{PP} Load Current		$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage			−0.2		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage		I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.1			V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 3: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 4: V_{PP} may be connected to V_{CC} except during programming.

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC87C257				Units
			150		200		
			Min	Max	Min	Max	
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	Chip Enable Access Time	$\overline{OE} = V_{IL}$		150		200	ns
t_{LL}	Chip Deselect Width		30		50		ns
t_{AL}	Address to ALE Latch Set-Up		5		15		ns
t_{LA}	Address Hold from ALE Latch		20		30		ns
t_{OE}	Output Enable to Output Valid	$\overline{CE} = V_{IL}$		50		75	ns
t_{LOE}	ALE to Output Enable		20		30		ns
t_{CF} (Note 1)	Chip Disable to Output in High Z	$\overline{OE} = V_{IL}$	0	50	0	55	ns
t_{DF} (Note 1)	Output Disable to Output in High Z	$\overline{CE} = V_{IL}$	0	50	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		ns

Note 1: This parameter is only sampled and is not 100% tested.

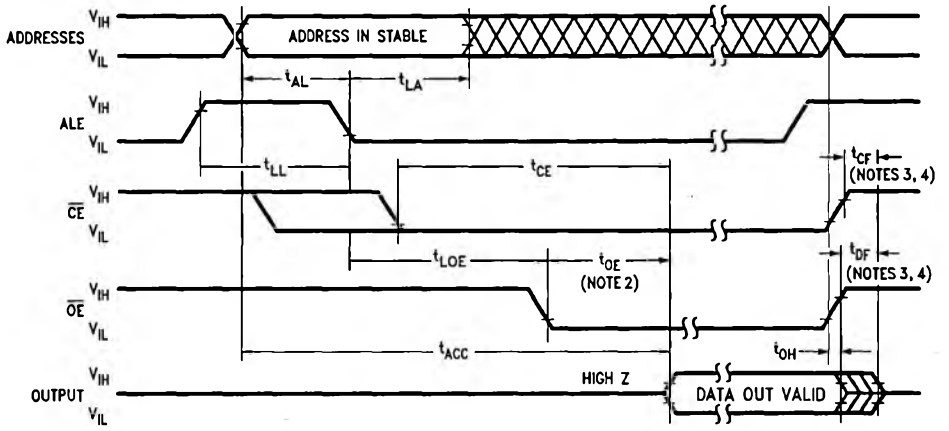
Capacitance $T_A = +25°C$, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 7)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 5, 6 and 8)



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Note 1: This parameter is only sampled and is not 100% tested.

Note 2: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 3: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 4: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 5: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 6: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

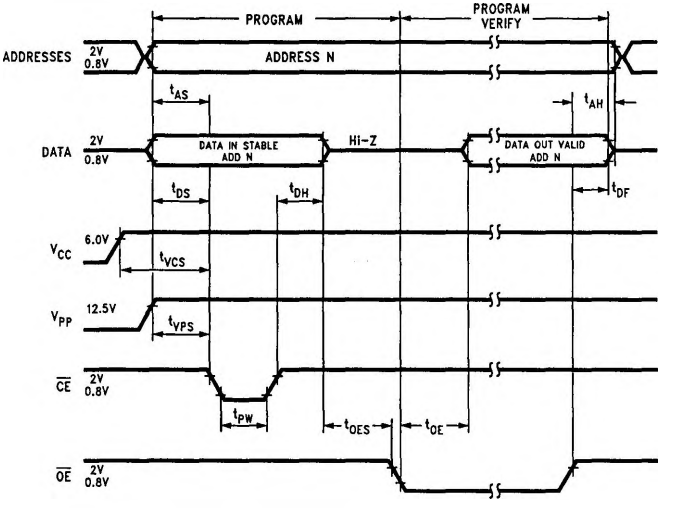
Note 7: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 8: V_{PP} may be connected to V_{CC} except during programming.

Programming Characteristics (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay		0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{OE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Note 1) (Same as NMC27C256B)

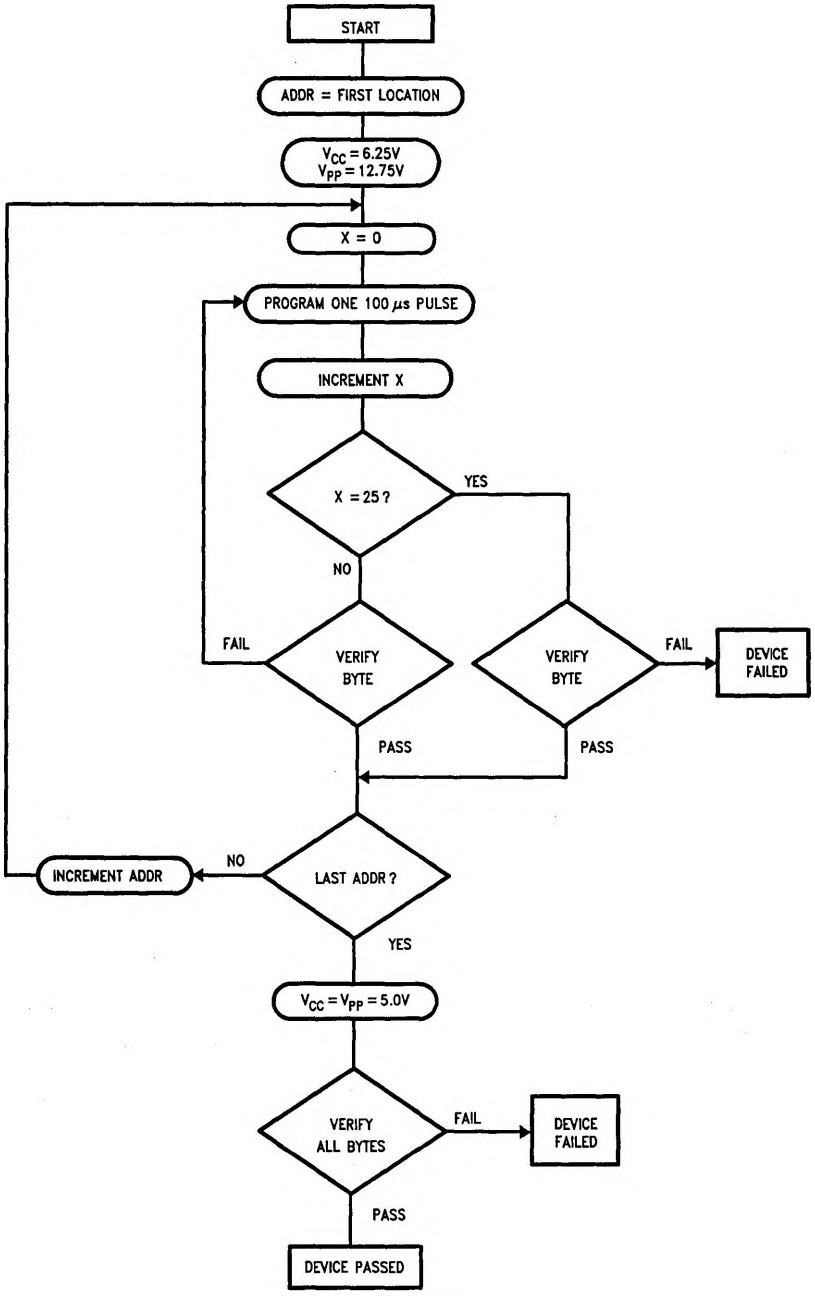

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FIGURE 1

Note 1: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Functional Description

DEVICE OPERATION

The seven modes of operation of the NMC87C257 are listed in Table I. It should be noted that all inputs for the seven modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other modes.

Read Mode

The NMC87C257 has a chip enable (CE) and an output enable (OE), both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}), is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Address Latch Operation

The NMC87C257 has an Address Latch Enable (ALE) pin which latches the address inputs on a negative transition. Addresses must be stable for the address setup time (t_{AL}) before the ALE transition, and they must hold for the address hold time (t_{LA}) after the transition. After the hold time has transpired the address drive can be removed from the address input pins and the bus can be used for other signals. The ALE pin is a feed-through latch and the part will operate as a normal unlatched device when the ALE pin is held high.

An important application for the NMC87C257 is memory in an address/data multiplexed microprocessor system. In an 8 bit system the low order memory address pins, A0–A7, can be tied to the respective memory output pins, O0–O7 and run on an 8-bit bus to the AD0–AD7 pins of the microprocessor. This reduces the bus width and it can be done without adding an address latch interface device. In this application the Output Enable ($\overline{OE}$) pin should be held high until after the address hold time (t_{LA}) has transpired, to avoid bus contention.

Standby Mode

The NMC87C257 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC87C257 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input and a CMOS low signal to the ALE input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC87C257s are usually used in larger memory arrays, National has provided a 3-line control function that accommodates this use of multiple memory connections. The 3-line control function allows for:

a. the lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To most efficiently use these control lines, it is recommended that $\overline{CE}$ and ALE be decoded and used as the primary device selecting functions while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC87C257.

Initially, and after each erasure, all bits of the NMC87C257 are in the "1" state. Data is introduced by selectively programmings "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by untraviolet light erasure.

The NMC87C257 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC87C257 is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC87C257 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Functional Description (Continued)

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP}/ALE (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	D_{OUT}
Latched	V_{IL}	V_{IL}	V_{IL}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	V_{IL}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	Hi-Z
Program	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Hi-Z

Programming multiple NMC87C257s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC87C257 may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC87C257.

Program Inhibit

Programming multiple NMC87C257s in parallel with different data is also easily accomplished. Except $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC87C257s may be common. A TTL low level program pulse applied to an NMC87C257 $\overline{CE}$ input with V_{PP} at 12.75V will program that NMC87C257. A TTL high level $\overline{CE}$ input inhibits the other NMC87C257 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC87C257 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for NMC87C257 is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256K part.

The code is accessed by applying 12.0V ± 0.5V to address pin A9. Addresses A1–A8, A10–A14, and all control pins are held at V_{IL} and V_{PP}/ALE is held at V_{IH}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0–O7. Proper code access is only guaranteed at 25°C ± 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC87C257 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC87C257 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC87C257 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC87C257 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC87C257 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Functional Description (Continued)

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

TABLE III. Minimum NMC87C257 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50