National Semiconductor

NMC6508 1024-Bit (1024 × 1) Static RAM

General Description

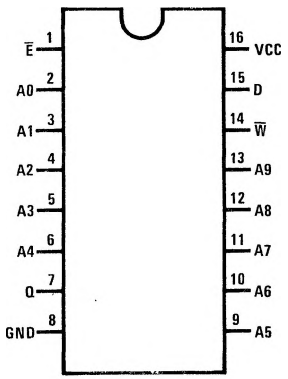
The NMC6508 is a static CMOS random access read/write memory organized as 1024 words of 1 bit each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible to the TTL environment. Synchronous operation is provided by the on-chip latches for the address inputs. The NMC6508 may be used in common I/O applications by externally connecting the data input and output terminals. The TRI-STATE® output, in conjunction with the ENABLE input, allows for easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- 16 pin — high density packaging
- Output data latches

Connection Diagram

Dual-In-Line Package

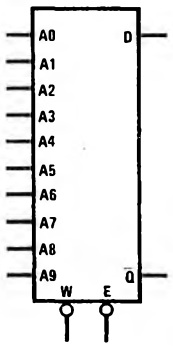


TOP VIEW

Order Number NMC6508J-2, NMC6508J-9 or NMC6508J-5
See NS Package J18A

Order Number NMC6508N-5
See NS Package N18A

Logic Symbol



Pin Names

A0–A9	Address Inputs
Ē	Chip Enable
W̄	Write Enable
D	Data Input
Q	Data Output

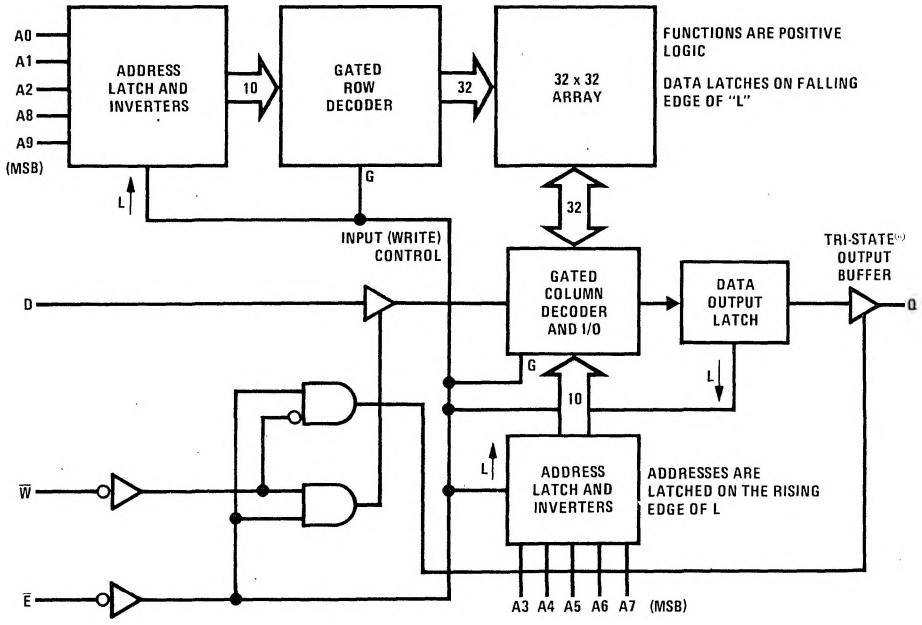
Functional Description

An NMC6508 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the address information into the on-chip registers. The output buffer is enabled when the WRITE ($\overline{W}$) input is HIGH and the ENABLE input is LOW.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next memory cycle.

When performing a write cycle, the minimum ENABLE LOW time is required to enter new data. The write pulse is created by the coincident LOW of the ENABLE and WRITE inputs. The data set-up and hold times are referenced to the rising edge of either the ENABLE or WRITE input, whichever occurs first.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6508B-9	4.5V	5.5V
NMC6508B-2	4.5V	5.5V
NMC6508-9	4.5V	5.5V
NMC6508-2	4.5V	5.5V
NMC6508-5	4.75V	5.25V
Temperature		
NMC6508B-9	−40°C	85°C
NMC6508B-2	−55°C	125°C
NMC6508-9	−40°C	85°C
NMC6508-2	−55°C	125°C
NMC6508-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

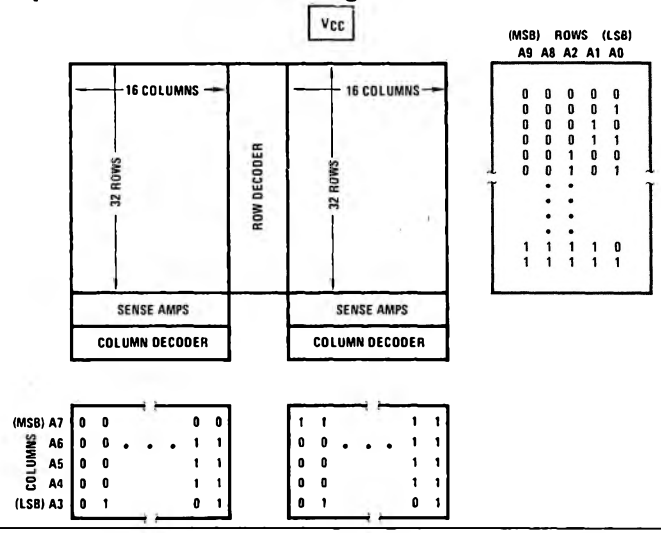
Symbol	Parameter	Conditions	NMC6508B-9, NMC6508B-2 NMC6508-9, NMC6508-2		NMC6508-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC − 2.0	VCC + 0.3	VCC − 2	VCC + 0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

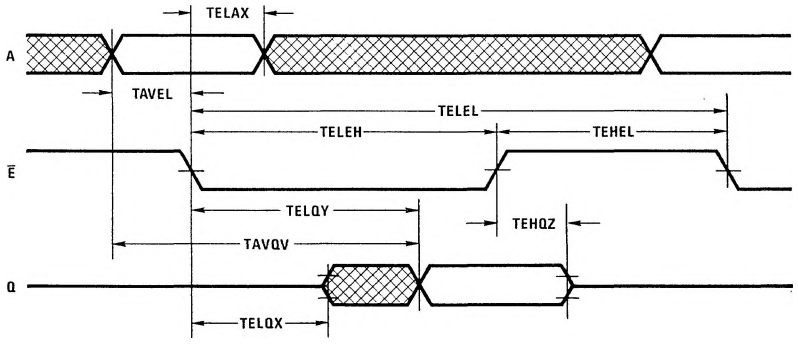
NMC6508 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6508B-9 NMC6508B-2		NMC6508-9 NMC6508-2		NMC6508-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	180		250		300		ns
TELQX	Output Enable from Enable ($\bar{E}$)		120		160		200	ns
TEHQZ	Output Disable from Enable ($\bar{E}$)		120		160		200	ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	100		100		150		ns
TELEL	Read or Write Cycle Time	280		350		450		ns

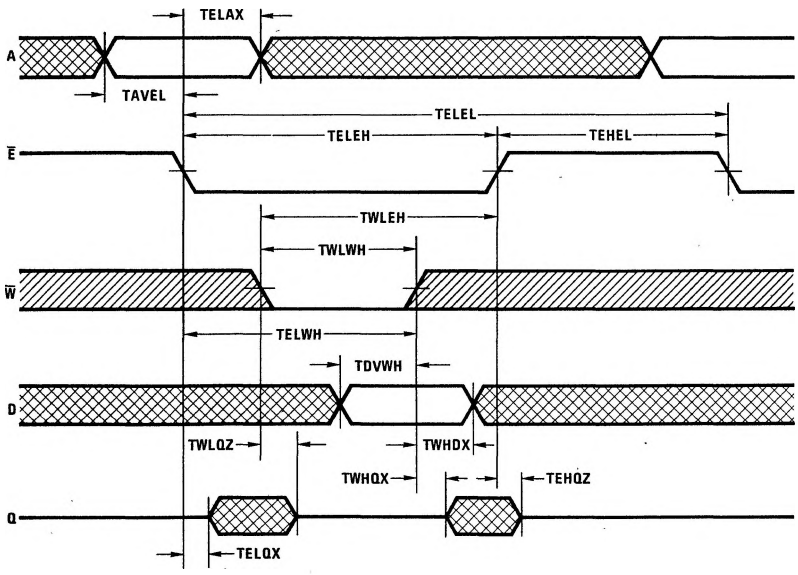
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6508B-9 NMC6508B-2		NMC6508-9 NMC6508-2		NMC6508-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TDVWH	Data Set-up Time	80		110		130		ns
TELWH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	100		130		160		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TELEL	Read or Write Cycle Time	280		350		450		ns
TWHDM	Data Hold Time	0		0		0		ns
TWLEH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	100		130		160		ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	180		250		300		ns
TELQX	Output Enable from $\overline{E}$		120		160		200	ns
TWLQZ	Output Disable from $\overline{W}$		120		160		200	ns
TWHQX	Output Enable from $\overline{W}$		120		160		200	ns
TEHQZ	Output Disable from $\overline{E}$		120		160		200	ns

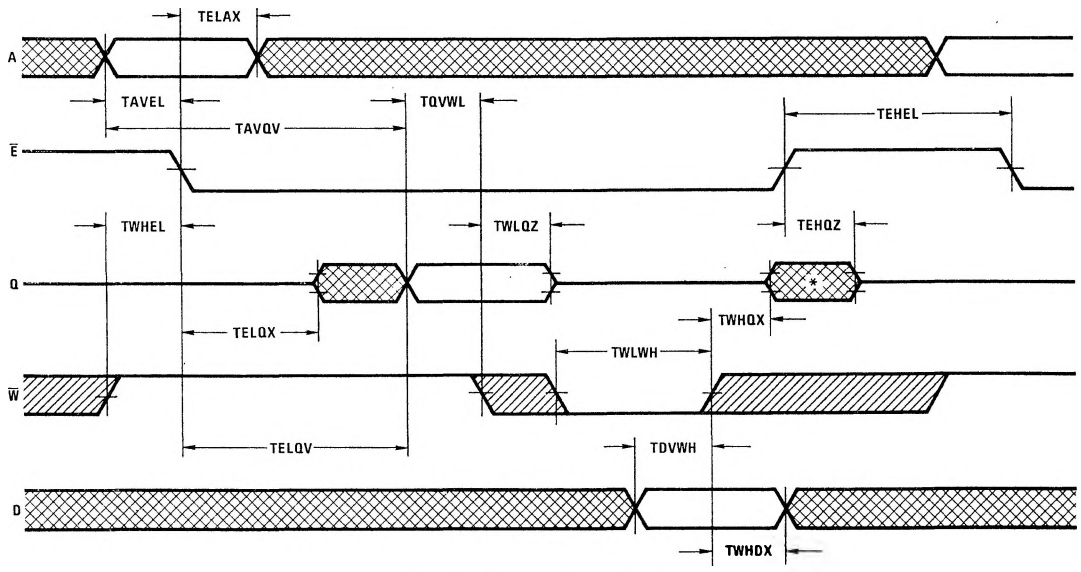
Write Cycle Waveforms



Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6508B-9 NMC6508B-2		NMC6508-9 NMC6508-2		NMC6508-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TWHDM	Data Hold Time	0		0		0		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWHEL	$\overline{W}$ Read Mode Set-up Time	0		0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TELQX	Output Enable from Enable ($\overline{E}$)		120		160		200	ns
TEHQZ	Output Disable from Enable ($\overline{E}$)		120		160		200	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		120		160		200	ns
TDVWH	Data Set-up Time	80		110		130		ns
TWHQX	Output Enable from Write ($\overline{W}$)		120		160		200	ns

Read-Modify-Write Cycle Waveforms



* Output enable can be avoided by preceding the rising edge of $\overline{W}$ with the rising edge of $\overline{E}$ by time; TEHQZ