LED DECODER/DRIVER

NE589

DESCRIPTION

The NE589 is a latch/decoder/driver for 7-segment common cathode LED displays. The NE589 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

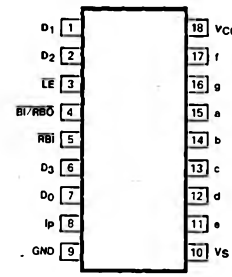
- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing edge zeros**

APPLICATIONS

- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

PIN CONFIGURATION

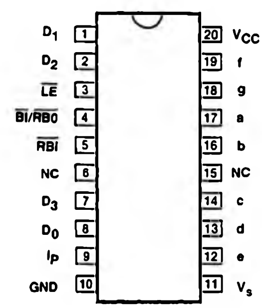
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE589F NE589N

D2 PACKAGE



TOP VIEW
NE589D[2]

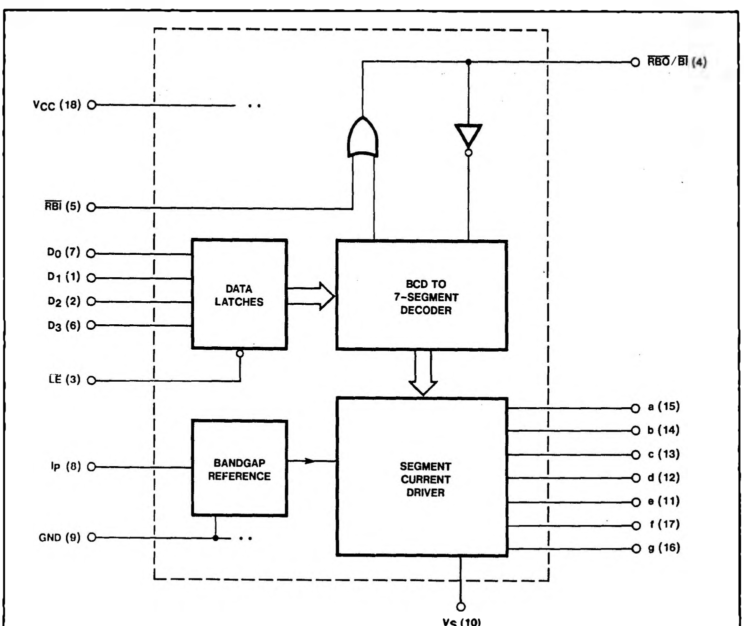
NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified

	PARAMETER	RATING	UNIT
V_{CC}, V_S	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

NOTE
Derate power dissipation as indicated
N package - 95°C/watt above 55°C
F package - 100°C/watt above 50°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C. Typical values are at $V_{CC} = V_S = 5V$, $T_A = 25°C$, $R_p = 7k\Omega$ (±1%) unless otherwise stated.

	PARAMETER	TEST CONDITIONS	NE589			UNIT
			Min	Typ	Max	
V_{CC}, V_S	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All Inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN} = −12mA, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs D_0 −D_3, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V		 0.1 10	 10 15	 μA μA
I_{IH}	Input high current	Input $\overline{BI}$ (pin 4) $\overline{RBI}$ = H V_{IN} = V_{CC} = 5.25V		10		μA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs D_0 − D_3 $\overline{LE}$, $\overline{RBI}$		−5 −200		μA
I_{IL}	Input low current	Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{OUT} = 3.0mA		0.2	0.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$ I_{OUT} = −50μA $\overline{RBI}$ = H	3.5	4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" thru "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g"		20	250	μA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		25	55	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		30	65	mA

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AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_S = 5V$ $T_A = 25°C$, $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

PARAMETER		TEST CONDITIONS	NE589			UNIT
			Min	Typ	Max	
$t_{Dav.}$	Propagation delay Figure 2	From data to output		135		ns
$t_{Dav.}$	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		85			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	75			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

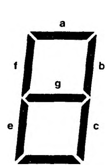
NOTE:
$t_{DAV.} = \max(t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	•	X	X	X	X	STABLE								STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	H	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	a
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	c
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	e
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	f
••BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L••	blank

NOTES
H = HIGH voltage level, output is "ON"
L = LOW voltage level, output is "OFF"
X = Don't care
• The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
•• $\overline{RBO/BI}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



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NE589 PROGRAMMING

NE589 output current can be programmed by using a programming resistor, R_P, connected between r_P (pin 8) and Gnd (pin 9). The voltage at r_P (pin 8) is constant ($\approx$ 1.3V). A partial schematic of the voltage reference used in the NE589 is shown in figure 1.

Output current to program current ratio, I_O/I_P, is 120 in the 10mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

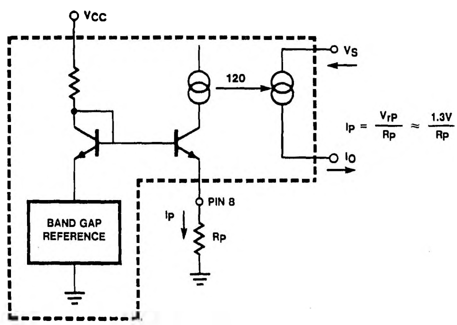


Figure 1

TIMING DIAGRAMS

PROPAGATION DELAY, DATA TO OUTPUT

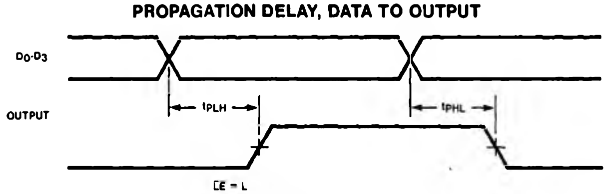


Figure 2

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

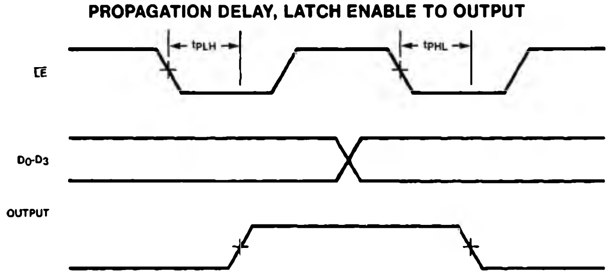


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 5, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

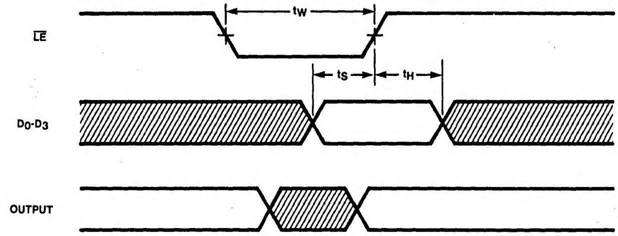


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

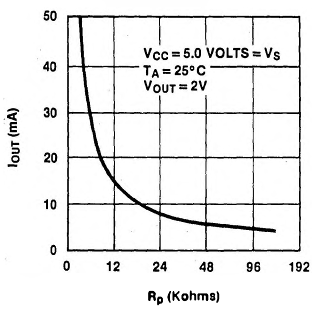
$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$

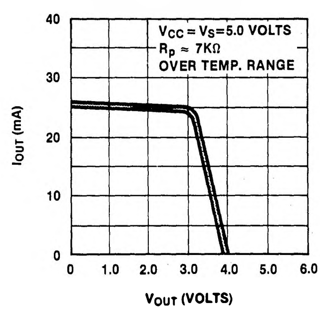
$P_{d\,max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW
$= 945$ mW

TYPICAL PERFORMANCE CURVES

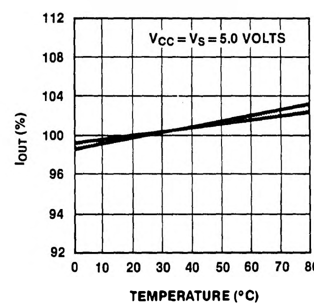
OUTPUT CURRENT VS PROGRAM RESISTOR



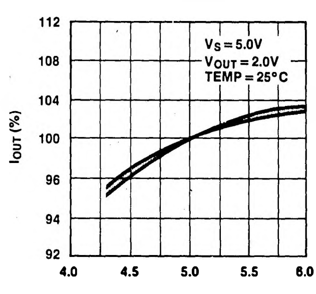
OUTPUT CURRENT VS OUTPUT VOLTAGE



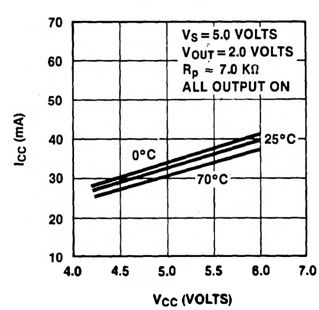
NORMALIZED OUTPUT CURRENT VS TEMPERATURE



NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE

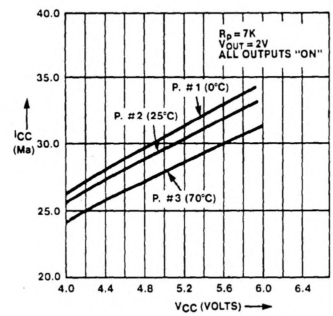


SUPPLY CURRENT VS SUPPLY VOLTAGE



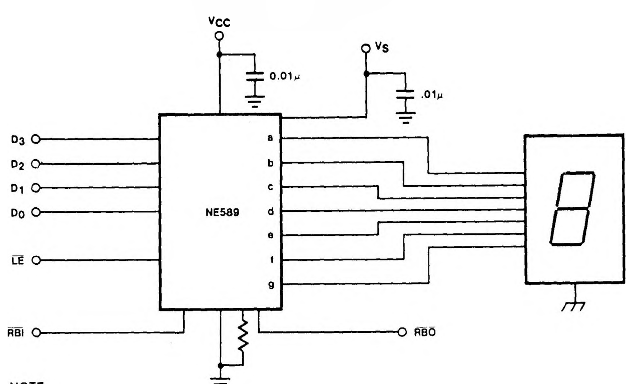
TYPICAL PERFORMANCE CURVES (Cont'd)

SUPPLY CURRENT VS SUPPLY VOLTAGE NE589



TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 μF ceramic

Figure 5

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$P_{d\,av}$ = 5.0 × 30 + 3.00 × 5 × 25 mW
= 525 mW

Operating temperature range limitations can be deduced from the power dissipation graph in figure 9.

However, a major portion of this power dissipation ($P_{d\,max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega \text{ (½ W rating)}$$

assuming worst case I_{seg} of 30 mA

Hence now $P_{d\,max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times X\, I_{seg} \times K_{DC}$
= 5.25 × 50 + 1.25 × 7 × 30 mW
= 525 mW

and $P_{d\,av}$ = 5.0 × 30 + 1.25 × 5 × 25
= 306 mW

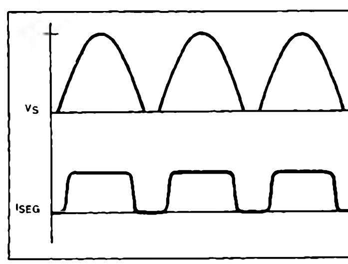
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d \,.\, V_D \simeq 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 8. For example a darlington PNP or NPN emitter follower may be preferable. Figure 7 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
V_S = 4.9V pk.
V_F = 2.0V

The duty cycle is approximately 60%.

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TYPICAL APPLICATIONS (Cont'd)

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL AND LEADING EDGE RIPPLE BLANKING

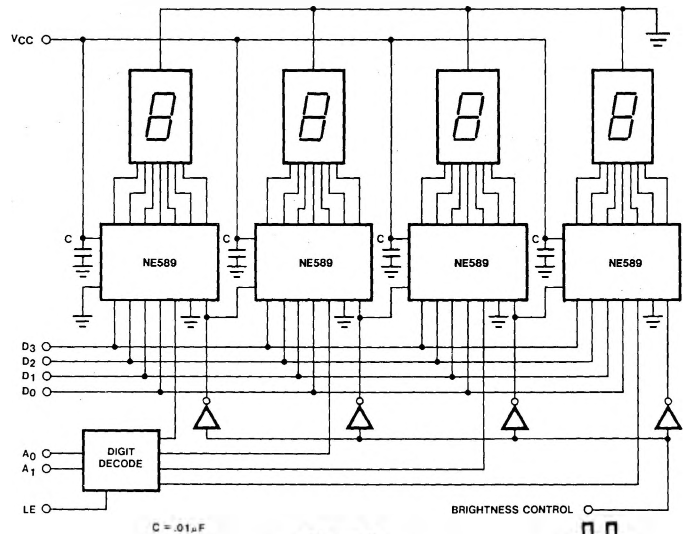

Figure 6

INTERFACING 8-DIGIT LED DISPLAY WITH μP BUS

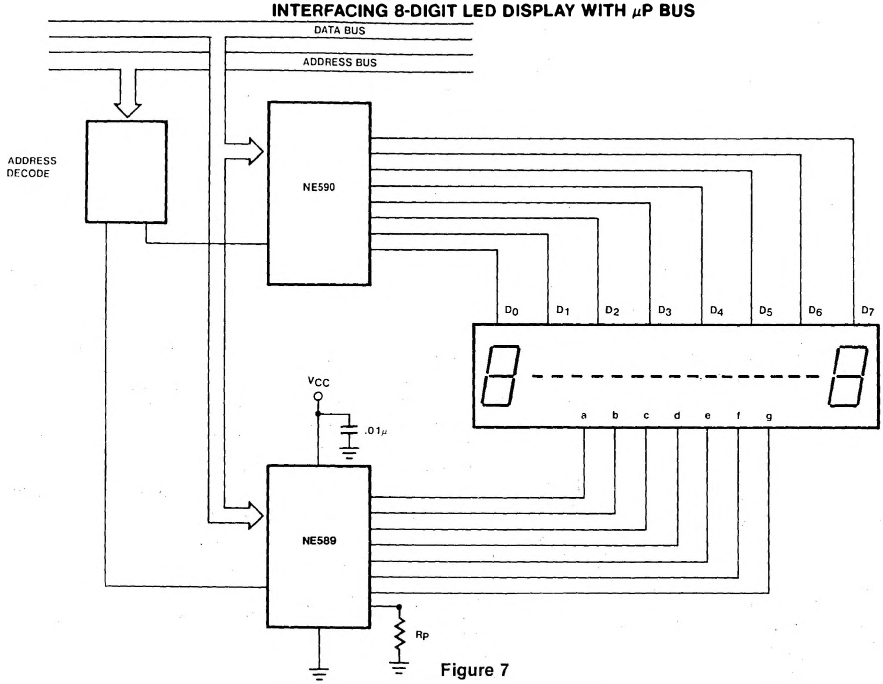

Figure 7

LED DECODER/DRIVER NE589

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT MULTIPLEXED LED DISPLAY

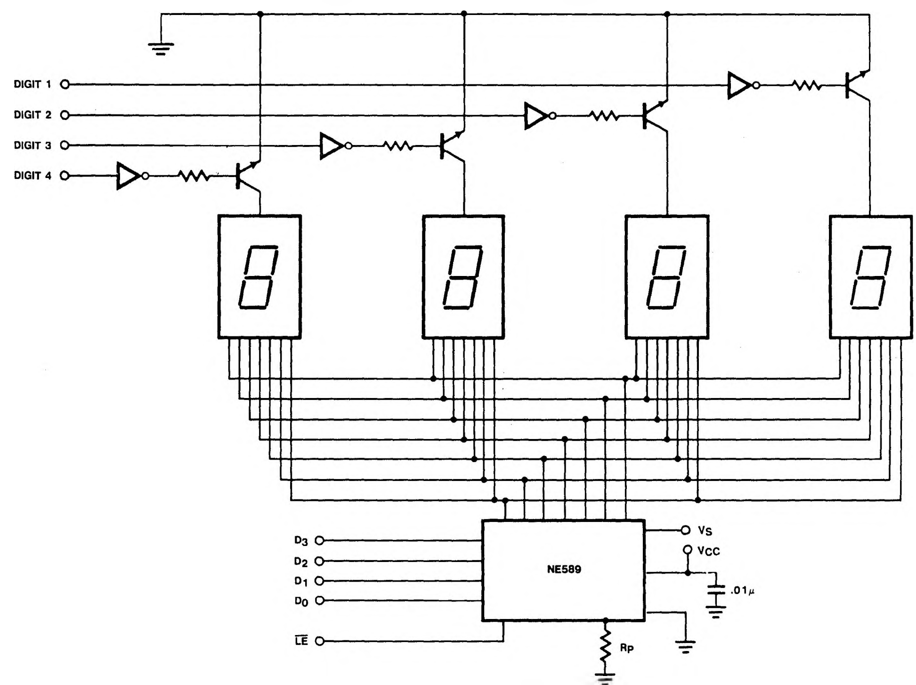

Figure 8

For additional information, refer to the Applications Section.