Signetics

NE568
150MHz Phase-Locked Loop

Preliminary Specification

Linear Products

DESCRIPTION

The NE568 is a monolithic phase-locked loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz. The integrated circuit consists of a limiting amplifier, a current-controlled oscillator (ICO), a phase detector, a level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568 is particularly well-suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568 will demodulate ±10% deviations with less than 4.0% non-linearity (1.5% typical). In addition to high linearity, the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568 is available in 20-pin dual in-line and 20-pin SO (surface-mounted) plastic packages.

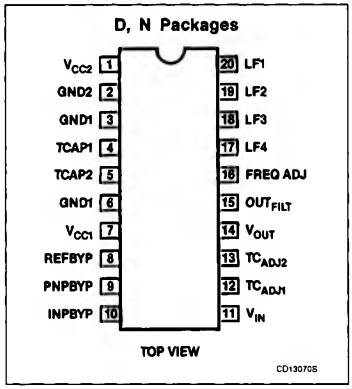
FEATURES

- **Operation to 150MHz**
- **High linearity buffered output**
- **Series or shunt loop filter component capability**
- **Temperature compensated**

APPLICATIONS

- **Satellite receivers**
- **Fiber-optic video links**
- **VHF FSK demodulators**
- **Clock recovery**

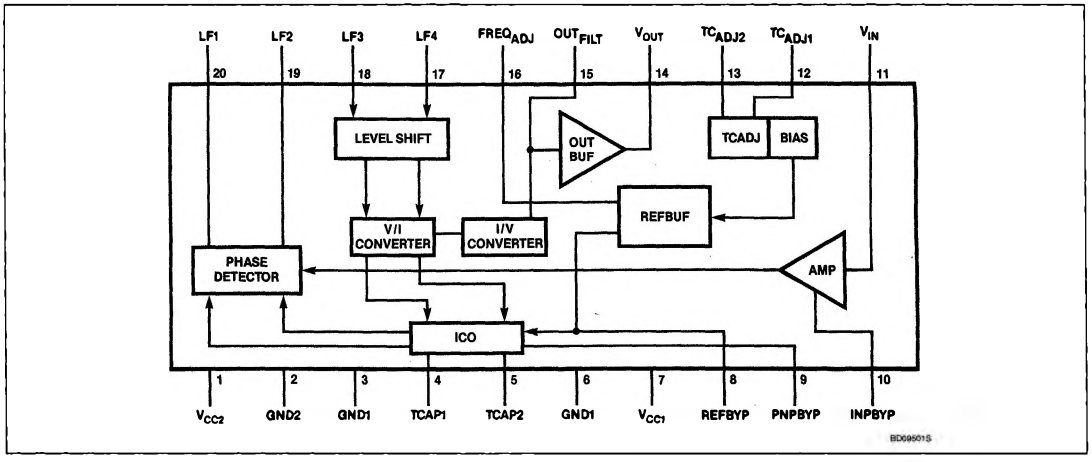
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL Package	0 to +70°C	NE568D
20-Pin Plastic DIP	0 to +70°C	NE568N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6	V
T_A	Operating free-air ambient temperature range	0 to +70	°C
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Maximum power dissipation	500	mW

ELECTRICAL CHARACTERISTICS

The electrical characteristics listed below are actual tests (unless otherwise stated) performed on each device with an automatic IC tester prior to shipment. Performance of the device in automated test setup is not necessarily optimum. The NE568 is layout-sensitive. Evaluation of performance for correlation to the data sheet should be done with the circuit and layout of Figures 1 – 3 with the evaluation unit soldered in place. (Do not use a socket!)

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$, $f_O = 70MHz$, Test Circuit Figure 1, $f_{IN} = -20dBm$, $R_4 = 0\Omega$ (ground), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{CC}	Supply current			60	75	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{OSC}	Maximum oscillator operating frequency[3]		150			MHz
	Input signal level		50 −20[1]		2000 +10	mV_{P-P} dBm
BW	Demodulated bandwidth			$f_O/7$		MHz
	Non-linearity[5]	Dev = ±10%, Input = −20dBm Dev = ±20%, Input = −20dBm Dev = ±20%, Input = +10dBm		1.5	4.0 5.5 5.5	%
	Lock range[2]	Input = −20dBm	±25	±35		% of f_O
	Capture range[2]	Input = −20dBm	±20	±30		% of f_O
	TC of f_O	Figure 1		100		ppm/°C
R_{IN}	Input resistance[4]		1			kΩ
	Output impedance			6		Ω
	Demodulated V_{OUT}	Dev = ±20% of f_O measured at Pin 4	0.45	0.52		V_{P-P}
	AM rejection	V_{IN} = −20dBm (30% AM) 0dBm (30% AM) referred to ±20% deviation		30 50		dB
f_O	Distribution[6]	Centered at 70MHz, R_2 = 1.2kΩ, C_2 = 17pF, R_4 = 0Ω ($C_2 + C_{STRAY} \approx 20pF$)	−15	0	+15	%
f_O	Drift with supply	4.75V to 5.25V		1		%/V

NOTES:

1. Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.
2. Limits are set symmetrical to f_O. Actual characteristics may have asymmetry beyond the specified limits.
3. Not 100% tested, but guaranteed by design.
4. Input impedance depends on package and layout capacitance. See Figures 4 and 5.
5. Linearity is tested with incremental changes in input frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}). Nonlinearity is then calculated from a straight line over the deviation range specified.
6. Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

150MHz Phase-Locked Loop NE568

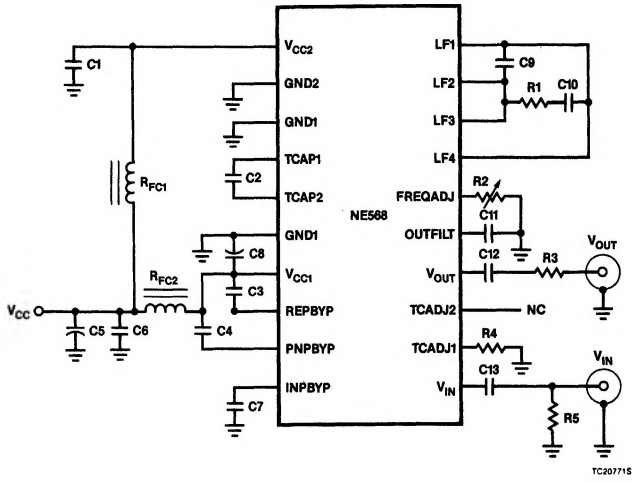


Figure 1. Test and Application Circuit

FUNCTIONAL DESCRIPTION

The NE568 is a high-performance phase-locked loop (PLL). The circuit consists of conventional PLL elements, with special circuitry for linearized demodulated output, and high-frequency performance. The process used has NPN transistors with $f_T > 6GHz$. The high gain and bandwidth of these transistors make careful attention to layout and bypass critical for optimum performance. The performance of the PLL cannot be evaluated independent of the layout. The use of the application layout in this data sheet and surface-mount capacitors are highly recommended as a starting point.

The input to the PLL is through a limiting amplifier with a gain of 200. The input of this amplifier is differential (Pins 10 and 11). For single-ended applications, the input must be coupled through a DC-blocking capacitor with low impedance at the frequency of interest. The single-ended input is normally applied to Pin 11 with Pin 10 AC-bypassed with a low-impedance capacitor. The input impedance is characteristically slightly above 500Ω. Impedance match is not necessary, but loading the signal source should be avoided. When the source is 50 or 75Ω, a DC-blocking capacitor is usually all that is needed.

Input amplification is low enough to assure reasonable response time in the case of large signals, but high enough for good AM rejection. After amplification, the input signal drives one port of a multiplier-cell phase detector. The other port is driven by the current-controlled oscillator (ICO). The output of the phase comparator is a voltage proportional to the phase difference of the input and ICO signals. The error signal is filtered with a low-pass filter to provide a DC-correction voltage, and this voltage is converted to a current which is applied to the ICO, shifting the frequency in the direction which causes the input and ICO to have a 90° phase relationship.

The oscillator is a current-controlled multivibrator. The current control affects the charge/discharge rate of the timing capacitor. It is common for this type of oscillator to be referred to as a voltage-controlled oscillator (VCO), because the output of the phase comparator and the loop filter is a voltage. To control the frequency of an integrated ICO multivibrator, the control signal must be conditioned by a voltage-to-current converter. In the NE568, special circuitry predistorts the control signal to make the change in frequency a linear function over a large control-voltage range.

The free-running frequency of the oscillator depends on the value of the timing capacitor connected between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When $R_2 = 1.2k\Omega$ and $R_4 = 0\Omega$, a very close approximation of the correct capacitor value is:

$$C^* = \frac{0.0014}{f_O} \text{ F}$$

where

$$C^* = C_2 + C_{STRAY}.$$

The temperature-compensation resistor, R_4, affects the actual value of capacitance. This equation is normalized to 70MHz. See Figure 6 for correction factors.

The loop filter determines the dynamic characteristics of the loop. In most PLLs, the phase detector outputs are internally connected to the ICO inputs. The NE568 was designed with filter output to input connections from Pins 20 (ϕ DET) to 17 (ICO), and Pins 19 (ϕ DET) to 18 (ICO) external. This allows the use of both series and shunt loop-filter elements. The loop constants are:

$K_D = 0.127$V/Radian (Phase Detector Constant)

$$K_O = 4.2 \times 10^9 \frac{\text{Radians}}{\text{V-sec}} \text{ (ICO Constant)}$$

The loop filter determines the general characteristics of the loop. Capacitors C_9, C_{10}, and resistor R_1, control the transient output of the phase detector. Capacitor C_9 suppresses 70MHz feedthrough by interaction with 100Ω load resistors internal to the phase detector.

$$C_9 = \frac{1}{2\pi\ (50)(f_O)} \text{ F}$$

At 70MHz, the calculated value is 45pF. Empirical results with the test and application board were improved when a 56pF capacitor was used.

The natural frequency for the loop filter is set by C_{10} and R_1. If the center frequency of the loop is 70MHz and the full demodulated bandwidth is desired, i.e., $f_{BW} = f_O/7 = 10$MHz, and a value for R_1 is chosen, the value of C_{10} can be calculated.

$$C_{10} = \frac{1}{2\pi\ R_1 f_{BW}} \text{ F}$$

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568D

C_1	100nF	±10%	Ceramic chip	1206
C_2[1]	18pF	±2%	Ceramic chip	0805
C_2[2]	34pF	±2%	Ceramic OR chip	
C_3	100nF	±10%	Ceramic chip	1206
C_4	100nF	±10%	Ceramic chip	1206
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	1206
C_7	100nF	±10%	Ceramic chip	1206
C_8	100nF	±10%	Ceramic chip	1206
C_9	56pF	±2%	Ceramic chip	0805 or 1206
C_{10}	560pF	±2%	Ceramic chip	0805 or 1206
C_{11}	47pF	±2%	Ceramic chip	0805 or 1206
C_{12}	100nF	±10%	Ceramic chip	1206
C_{13}	100nF	±10%	Ceramic chip	1206
R_1	27Ω	±10%	Chip	⅛W
R_2	2kΩ		Trim pot	⅛W
R_3[3]	43Ω	±10%	Chip	⅛W
R_4[4]	4.5kΩ	±10%	Chip	⅛W
R_5[3]	50Ω	±10%	Chip	⅛W
RFC_1[5]	10μH	±10%	Surface mount	
RFC_2[5]	10μH	±10%	Surface mount	

NOTES:
1. $C_2 + C_{STRAY} = 20pF$.
2. $C_2 + C_{STRAY} = 36pF$ for temperature-compensated configuration with $R_4 = 4.5k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.
5. 0Ω chip resistors (jumpers) may be substituted with minor degradation of performance.

For the test circuit, R_1 was chosen to be 27Ω. The calculated value of C_{10} is 590pF; 560pF was chosen as a production value. (In actual satellite receiver applications, improved video with low carrier/noise has been observed with a wider loop-filter bandwidth.)

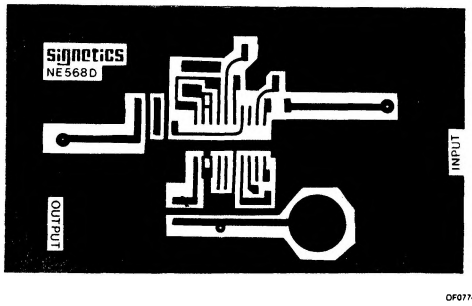
A typical application of the NE568 is demodulation of FM signals. In this mode of operation, a second single-pole filter is available at Pin 15 to minimize high frequency feedthrough to the output. The roll-off frequency is set by an internal resistor of 350Ω ±20%, and an external capacitor from Pin 15 to ground. The value of the capacitor is:

$$C = \frac{1}{2\pi\ (350) f_{BW}}\ F$$

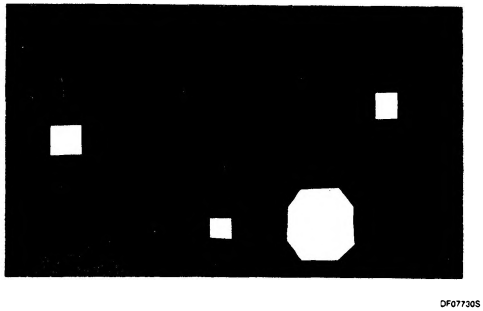
Two final components complete the active part of the circuitry. A resistor from Pin 12 to ground sets the temperature stability of the circuit, and a potentiometer from Pin 16 to ground permits fine tuning of the free-running oscillator frequency. The Pin 16 potentiometer is normally 1.2kΩ. Adjusting this resistance controls current sources which affect the charge and discharge rates of the timing capacitor and, thus, the frequency. The value of the temperature stability resistor is chosen from the graph in Figure 6.

The final consideration is bypass capacitors for the supply lines. The capacitors should be ceramic chips, preferably surface-mount types. They must be kept very close to the device. The capacitors from Pins 8 and 9 return to V_{CC1} before being bypassed with a separate capacitor to ground. This assures that no differential loops are created which might cause instability. The layouts for the test circuits are recommended.

(Shown at 82% of original size.)



DF07740S



DF07730S

a. Component Side Top of Board **b. Back of Board**

NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent. Mount on bottom (back) of board. Add stand-off in each corner.
2. Back and top side ground must be connected at 8 point minimum.

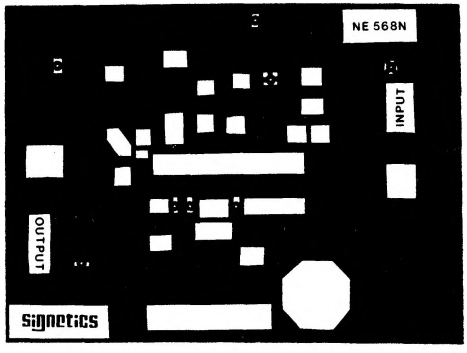
Figure 2

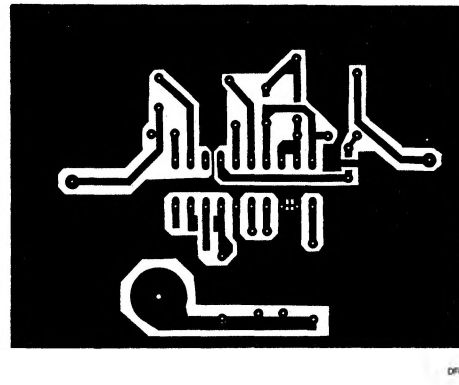
PARTS LIST AND LAYOUT 70MHz APPLICATION NE568N

C_1	100nF	±10%	Ceramic chip	50V
C_2[1]	17pF	±2%	Ceramic OR chip	50V
C_2[2]	34pF	±2%	Ceramic chip	0805
C_3	100nF	±10%	Ceramic chip	50V
C_4	100nF	±10%	Ceramic chip	50V
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic OR chip	50V
C_7	100nF	±10%	Ceramic chip	50V
C_8	100nF	±10%	Ceramic chip	50V
C_9	56pF	±2%	Ceramic chip	50V
C_{10}	560pF	±2%	Ceramic chip	50V
C_{11}	47pF	±2%	Ceramic OR chip	50V
C_{12}	100nF	±10%	Ceramic OR chip	50V
C_{13}	100nF	±10%	Ceramic OR chip	50V
R_1	27Ω	±10%	Carbon	¼W
R_2	2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Carbon	¼W
R_4[4]	4.5kΩ	±10%	Carbon	¼W
R_5[3]	50Ω	±10%	Carbon	¼W
RFC_1	10μH	±10%		
RFC_2	10μH	±10%		

NOTES:
1. $C_2 + C_{STRAY} = 20pF$ for test configuration with $R_4 = 0\Omega$.
2. $C_2 = 34pF$ for temperature-compensated configuration with $R_4 = 4.5k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$; $R_3 = 75\Omega$ for 75Ω applications.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 17pF$.

(Shown at 82% of original size.)





a. Component Side for Leaded Components **b. Solder Side of Board and Chip Capacitors**

NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent mounted on the component side of the board.
2. Component side and solder side ground planes must be connected at 8 points minimum.

Figure 3

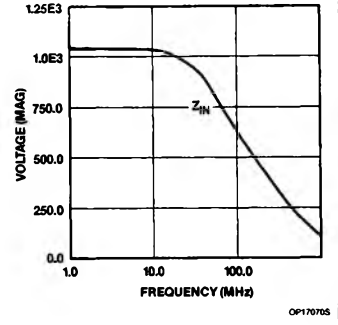


Figure 4. NE568 Input Impedance With CP = 0.5pF 20-Pin SO Package

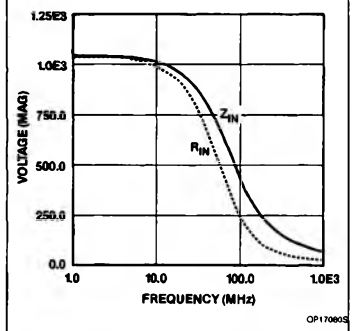


Figure 5. NE568 Input Impedance With CP = 1.49pF 20-Pin Dual In-Line Plastic Package

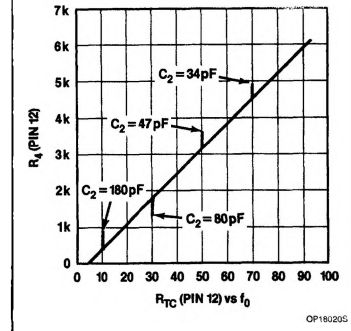


Figure 6

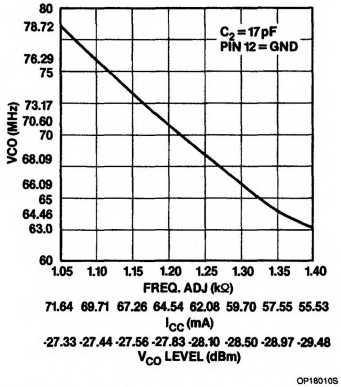


Figure 7. Typical V_{CO} Frequency vs R_2 Adjustment

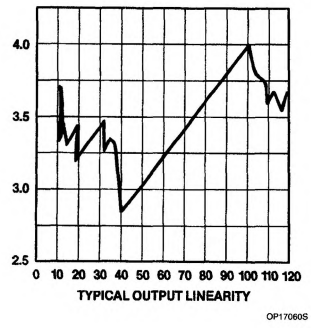


Figure 8. Typical Output Linearity