PHASE LOCKED LOOP

SE/NE564

DESCRIPTION

The NE564 is a versatile, high guaranteed frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

APPLICATIONS

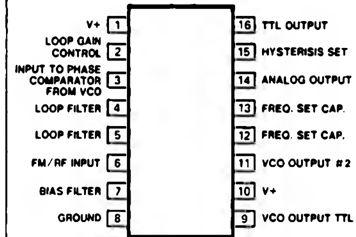
- **High speed modems**
- **FSK receivers and transmitters**
- **Frequency synthesizers**
- **Signal generators**
- **Various satcom/TV systems**

FEATURES

- **Operation with single 5V supply**
- **TTL compatible inputs and outputs**
- **Guaranteed operation to 50MHz**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**
- **Can be used as a modulator**
- **Variable loop gain (Externally Controlled)**

PIN CONFIGURATION

D, I, N PACKAGE



TOP VIEW

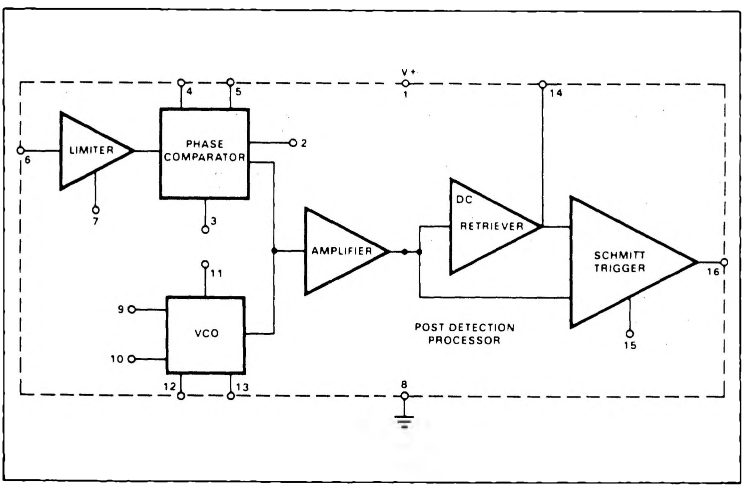
ORDER NUMBERS
NE/SE564I NE/SE564N
NE564D

ABSOLUTE MAXIMUM RATINGS

PARAMETER			RATING	UNIT
V+	Supply voltage			V
	Pin 1		14	
	Pin 10		6	
P_D	Power dissipation		600	mW
T_A	Operating temperature	NE	0 to 70	°C
	Operating temperature	SE	−55 to +125	
t_{stg}	Storage temperature		−65 to 150	°C

NOTE:
Operation above 5 volts will require heatsinking of the case.

BLOCK DIAGRAM



PHASE LOCKED LOOP

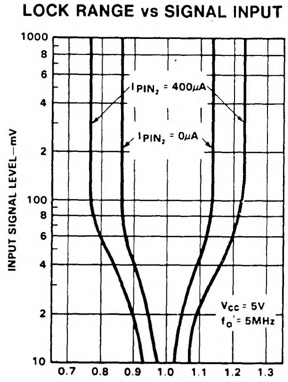
SE/NE564

ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, $f_o = 5MHz$, $I_B = 400\mu A$ unless otherwise specified

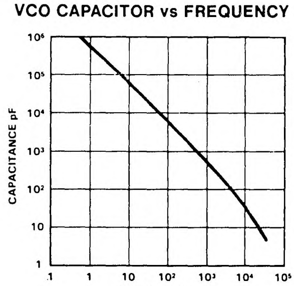
PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
Maximum VCO frequency	$C_1 = 0$ (stray)	50	65		45	60		MHz
Lock range	Input ≥ 200mVrms $T_A = 25°C$	40	70		40	70		% of f_o
	= 125°C	20	30					
	= −55°C	50	80					
	= 0°C					70		
	= 70°C					40		
Capture range	Input ≥ 200mVrms, $R_2 = 27\Omega$	20	30		20	30		% of f_o
VCO frequency drift with temperature	$f_o = 5MHz$, $T_A = -55°C$ to 125°C		400	1000				PPM/°C
	= 0°C to 70°C					400	1250	
	$f_o = 500KHz$, $T_A = -55°C$ to 125°C		250	500				
	= 0°C to 70°C					400	850	
VCO free running frequency	$C_1 = 91pF$ $R_C = 100\Omega$ "Internal"	4	5	6	3.5	5	6.5	MHz
VCO frequency change with supply voltage	$V_{CC} = 4.5V$ to 5.5V		3	8		3	8	% of f_o
Demodulated output voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation:							
	2% T = 25°C	16	28		16	28		mVrms
	1% T = 25°C	8	14		8	14		mVrms
	= 0°C					13		mVrms
	= −55°C	6	10					mVrms
	= 70°C					15		mVrms
	= 125°C	12	16					mVrms
Distortion	Deviation: 1% to 8%		1			1		%
Signal to noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
AM rejection	Std. condition, 30% AM		35			35		dB
Demodulated Output at operating voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation: 1%							
	$V_{CC} = 4.5V$	7	12		7	12		mVrms
	$V_{CC} = 5.5V$	8	14		8	14		mVrms
Supply current	$V_{CC} = 5V$ I_1, I_{10}		45	60		45	60	mA
Output								
"1" output leakage current	$V_{OUT} = 5V$, Pin 16, 9		1	20		1	20	μA
"0" output voltage	$I_{OUT} = 2mA$, Pin 16, 9		0.3	0.6		0.3	0.6	V
	$I_{OUT} = 6mA$, Pin 16, 9		0.4	0.8		0.4	0.8	V

TYPICAL PERFORMANCE CHARACTERISTICS

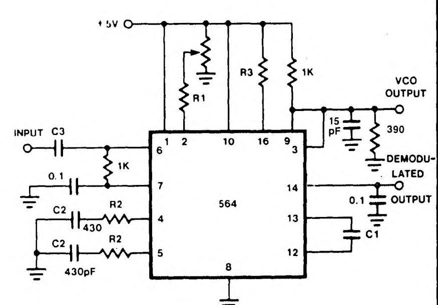
LOCK RANGE vs SIGNAL INPUT



VCO CAPACITOR vs FREQUENCY

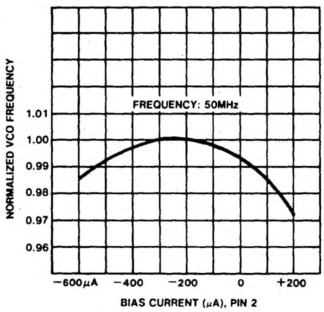


SE/NE 564 TEST CIRCUIT

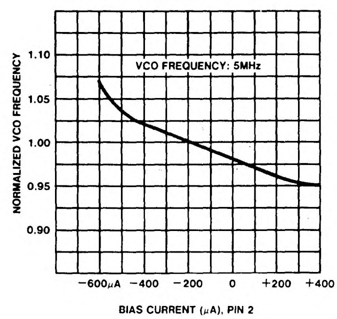


PHASE LOCKED LOOP — SE/NE564

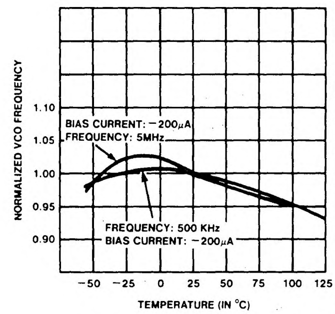
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



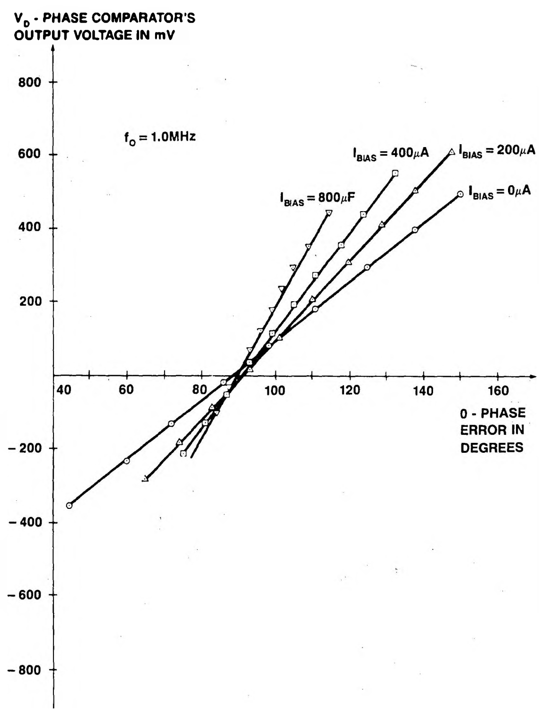
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



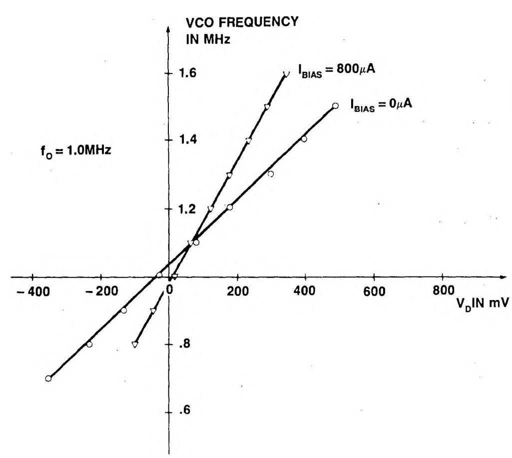
NORMALIZED VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VARIATION OF THE PHASE COMPARATOR'S OUTPUT VOLTAGE VERSUS PHASE ERROR AND BIAS CURRENT (K_D)



VCO OUTPUT FREQUENCY AS A FUNCTION OF INPUT VOLTAGE AND BIAS CURRENT (K_O)



PHASE LOCKED LOOP SE/NE564

FUNCTIONAL DESCRIPTION (figure 1)

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_o)}{K_{VCO}} \qquad \text{Equation 1}$$

K_{VCO} = conversion gain of the VCO
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_O. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources $Q_{25} - Q_{26}$ form the basic oscillator. The approximate free running frequency of the oscillator is shown in the following equation:

$$f_o = \frac{1}{22\, R_C\, (C_1 + C_S)} \qquad \text{Equation 2}$$

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)
C_1 = external frequency setting capacitor
C_S = stray capacitance

Variation of V_d (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative

EQUIVALENT SCHEMATIC

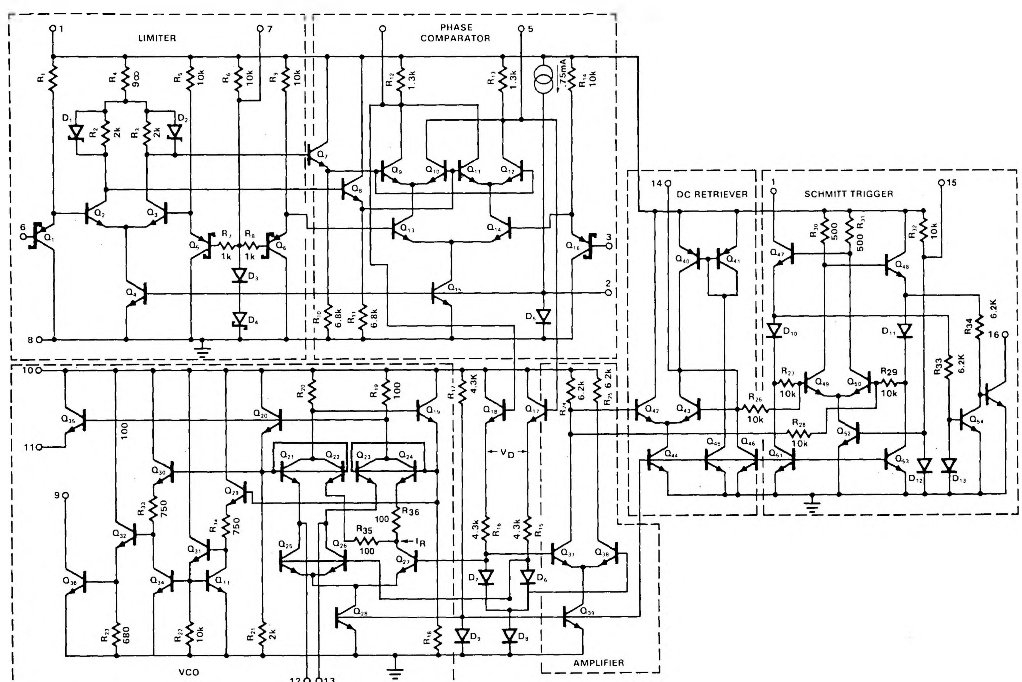


Figure 1

temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transductance amplifier Q_{42}–Q_{43} together with an external capacitor which is connected at the amplifier output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_m}{C_2} V_{in} dt \qquad \text{Equation 3}$$

g_m = transconductance of the amplifier
C_2 = capacitor at the output (pin 14)
V_{in} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q_{49}–Q_{50} with positive feedback being provided by Q_{47}-Q_{48}. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

The free running frequency of the VCO is shown by the following equation:

$$f_o = \frac{1}{25\, R_C\, (C_1 + C_S)} \qquad \text{Equation 4}$$

R_C = 100Ω
C_1 = external cap in farads
C_S = stray capacitance

FM DEMODULATOR AT 5V

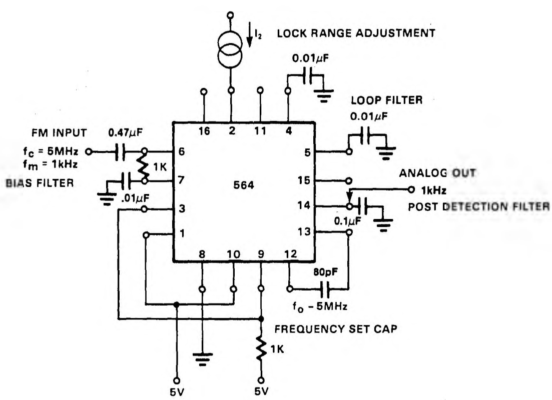


Figure 2

FM DEMODULATOR AT 12V

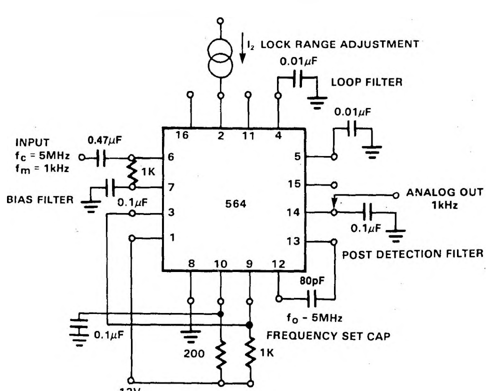


Figure 3

MODULATOR

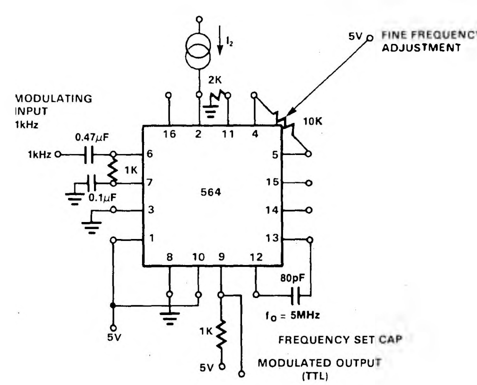


Figure 4

The loop filter diagram shown is explained by the following equation:

$$F(s) = \frac{1}{1 + sRC_3} \text{ (First Order)} \qquad \text{Equation 5}$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (INTERNAL)*

By adding capacitors to pins 4 and 5, a pole is added to the loop transfer function at

$$\omega = \frac{1}{RC_3}.$$

*Refer to Figure 1.

APPLICATIONS

FM DEMODULATOR

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in figures 2 and 3 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in figure 5. This curve will be appropriate for signals injected into pins 4 and 5 as shown in figure 4.

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

The lock range graph indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_o' frequencies.

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in figure 7 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

10.8MHz FSK DECODER USING THE 564

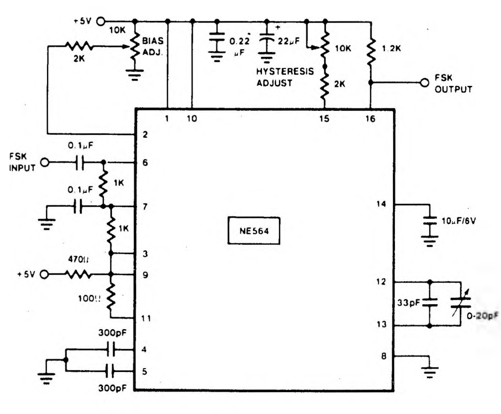
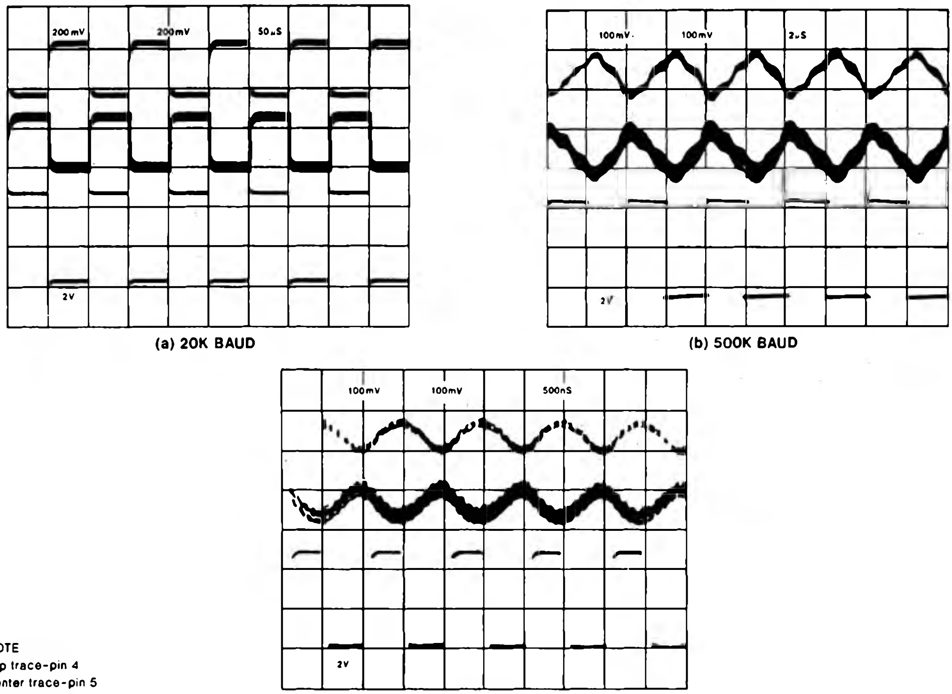


Figure 5

PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF



(a) 20K BAUD

(b) 500K BAUD

(c) 2.0M BAUD

NOTE
Top trace-pin 4
Center trace-pin 5
Bottom trace-pin 16

Figure 6

OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO – .
   If ÷ N in feedback loop, then
   $f_o = N \times f_{in}$.
2. Calculate value of the VCO frequency set capacitor:
   $$C_O \cong \frac{1}{2500\,f_o}$$
3. Set I_2 (current sinking into Pin 2) for $\cong 100\mu A$. After operation is obtained, this value may be adjusted for best dynamic behavior.
4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to ϕ det.). Adjust C_O trim or frequency adj. Pin 4-5 for exact center frequency if needed.
5. Close loop and inject input signal to Pin 6. Monitor Pin 3 and 6 with two channel scope. Lock should occur with $\Delta\phi_{3\text{-}6}$ equal to 90° (phase error).
6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pin 4 and 5. (See PLL application section in Analog Manual.)
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in duty cycle, D.C. offsets will occur in the loop which tend to create an artificial or biased VCO offset.
8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10-50μF on Pin 4, 5. Also careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

NE564 PHASE LOCKED FREQUENCY MULTIPLIER WITH VCXO

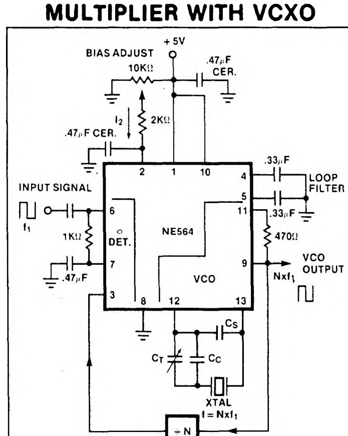


Figure 7

*For additional information, consult the Applications Section.