Signetics

NE/SA5230
Low Voltage Operational Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 125dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 30nV/$\sqrt{Hz}$ noise specification.

FEATURES

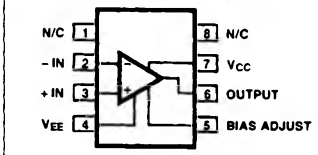
- **Works down to 1.8V supply voltages**
- **Adjustable supply current**
- **Low noise**
- **Common-mode includes both rails**
- **V_{OUT} within 100mV of both rails**

APPLICATIONS

- **Portable precision instruments**
- **Remote transducer amplifier**
- **Portable audio equipment**
- **Rail-to-rail comparators**
- **Half-wave rectification without diodes**
- **Remote temperature transducer with 4 to 20mA output transmission**

PIN CONFIGURATION

N, FE and D Packages



TOP VIEW

CD11071S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5230D
8-Pin Ceramic DIP	0 to +70°C	NE5230FE
8-Pin Plastic DIP	0 to +70°C	NE5230N
8-Pin Plastic SO	-40°C to +85°C	SA5230D
8-Pin Ceramic DIP	-40°C to +85°C	SA5230FE
8-Pin Plastic DIP	-40°C to +85°C	SA5230N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Single supply voltage	18	V
V_S	Dual supply voltage	±9	V
V_{IN}	Input voltage[1]	±9 (18)	V
	Differential input voltage[1]	$\pm V_S$	V
V_{CM}	Common-mode voltage (positive)	V_{CC} + 0.5	V
V_{CM}	Common-mode voltage (negative)	V_{EE} – 0.5	V
P_D	Power dissipation[2]	500	mW
T_J	Operating junction temperature[2]	150	°C
	Output short-circuit duration to either power supply pin[2, 3]	Indefinite	s
T_{STG}	Storage temperature	–65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Can exceed the supply voltages when $V_S \leq \pm 7.5V$ (15V).
2. The maximum operating junction temperature is 150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions.
   Derate above 25°C at the following rates:
   FE package at 6.7mW/°C
   N package at 9.5mW/°C
   D package at 6.25mW/°C
3. Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Single supply voltage	1.8 to 15	V
Dual supply voltage	±0.9 to ±7.5	V
Common-mode voltage (positive)	V_{CC} + 0.25	V
Common-mode voltage (negative)	V_{EE} – 0.25	V
Temperature		
NE grade	0 to 70	°C
SA grade	–40 to 85	°C

Low Voltage Operational Amplifier — NE/SA5230

DC AND AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, $\pm 0.9V \leq V_S \leq \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER		TEST CONDITIONS		BIAS	NE/SA5230			UNIT
						Min	Typ	Max	
V_{OS}	Offset voltage		$T_A = 25°C$		Any		0.4	3	mV
					Any		3	4	mV
V_{OS}	Drift				Any		2	5	µV/°C
I_{OS}	Offset current		$T_A = 25°C$		High		3	50	nA
			$T_A = 25°C$		Low		3	30	nA
					High			100	nA
					Low			60	nA
I_{OS}	Drift				High		0.5	1.4	nA/°C
					Low		0.3	1.4	nA/°C
I_B	Bias current		$T_A = 25°C$		High		40	150	nA
			$T_A = 25°C$		Low		20	60	nA
					High			200	nA
					Low			150	nA
I_B	Drift				High		2	4	nA/°C
					Low		2	4	nA/°C
I_S	Supply current		$V_S = \pm 0.9V$	$T_A = 25°C$	Low		110	160	µA
				$T_A = 25°C$	High		600	750	µA
					Low			250	µA
					High			800	µA
			$V_S = \pm 7.5V$	$T_A = 25°C$	Low		320	550	µA
				$T_A = 25°C$	High		1.1	1.6	mA
					Low			600	µA
					High			1.7	mA
V_{CM}	Common-mode input range		$V_{OS} \leq 6mV$, $T_A = 25°C$		Any	$V^- - 0.25$		$V^+ + 0.25$	V
					Any	V^-		V^+	V
CMRR	Common-mode rejection ratio		$V_S = \pm 7.5V$	$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$, $T_A = 25°C$	Any	85	95		dB
				$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$	Any	80			dB
PSRR	Power supply rejection ratio		$T_A = 25°C$		High	90	105		dB
			$T_A = 25°C$		Low	85	95		dB
					High	75			dB
					Low	80			dB
I_L	Load current	source	$V_S = \pm 7.5V$		Any	4	10		mA
		sink	$V_S = \pm 7.5V$		Any	5	15		mA
		source	$V_S = \pm 0.9V$		Any	1	5		mA
		sink	$V_S = \pm 0.9V$		Any	2	6		mA
		source	$V_S = \pm 0.9V$, $T_A = 25°C$		High	4	6		mA
		sink	$V_S = \pm 0.9V$, $T_A = 25°C$		High	5	7		mA
		source	$V_S = \pm 7.5V$, $T_A = 25°C$		High		16		mA
		sink	$V_S = \pm 7.5V$, $T_A = 25°C$		High		32		mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) Unless otherwise specified, $\pm 0.9V \leq V_S \leq \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS		BIAS	NE/SA5230			UNIT
					Min	Typ	Max	
A_{VOL}	Large-signal open-loop gain	$V_S = \pm 7.5V$	$R_L = 10k\Omega$, $T_A = 25°C$	High	120	2000		V/mV
			$R_L = 10k\Omega$, $T_A = 25°C$	Low	60	750		V/mV
				High	100			V/mV
				Low	50			V/mV
V_{OUT}	Output voltage swing	$V_S = \pm 0.9V$	$T_A = 25°C$, +SW	Any	750	800		mV
			$T_A = 25°C$, −SW	Any	750	800		mV
			+SW	Any	700			mV
			−SW	Any	700			mV
		$V_S = \pm 7.5V$	$T_A = 25°C$, +SW	Any	7.30	7.35		V
			$T_A = 25°C$, −SW	Any	−7.32	−7.35		V
			+SW	Any	7.25	7.30		V
			−SW	Any	−7.30	−7.35		V
SR	Slew rate	$T_A = 25°C$		High		0.25		V/μs
		$T_A = 25°C$		Low		0.09		V/μs
BW	Inverting unity gain bandwidth	$C_L = 100pF$, $T_A = 25°C$		High		0.6		MHz
		$C_L = 100pF$, $T_A = 25°C$		Low		0.25		MHz
θ_M	Phase margin	$C_L = 100pF$, $T_A = 25°C$		Any		70		Deg.
t_S	Settling time	$C_L = 100pF$, 0.1%		High		2		μs
		$C_L = 100pF$, 0.1%		Low		5		μs
V_{INN}	Input noise	$R_S = 0\Omega$, f = 1kHz		High		30		$nV/\sqrt{Hz}$
		$R_S = 0\Omega$, f = 1kHz		Low		60		$nV/\sqrt{Hz}$
THD	Total Harmonic Distortion	$V_S = \pm 7.5V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.003		%
		$V_S = \pm 0.9V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.002		%

THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NE5230 has a common-mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250mV without increasing the input offset voltage by more than 6mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail-to-rail input common-mode range, two emitter-coupled differential pairs are placed in parallel so that the common-mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 1 shows how the complementary emitter-coupler transistors are configured to form the basic input stage cell. Common-mode input signal voltages in the range from 0.8V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common-mode input signal voltages in the range of V_{EE} to 0.8V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail-to-rail capability. As the common-mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common-mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non-conducting. When the common-mode input voltage passes below the reference voltage, V_{B1} = 0.8V at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120mV around the reference voltage V_{B1}. In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common-mode voltage crosses the internal reference voltage, V_{B1}. Careful circuit layout with a cross-coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3mV and a change in the input offset voltage of less than 0.1mV.

Output Stage

Processing output voltage swings that nominally reach to less than 100mV of either supply voltage can only be achieved by a pair of complementary common-emitter connected transistors. Normally, such a configuration causes complex feed-forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NE5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 2, and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

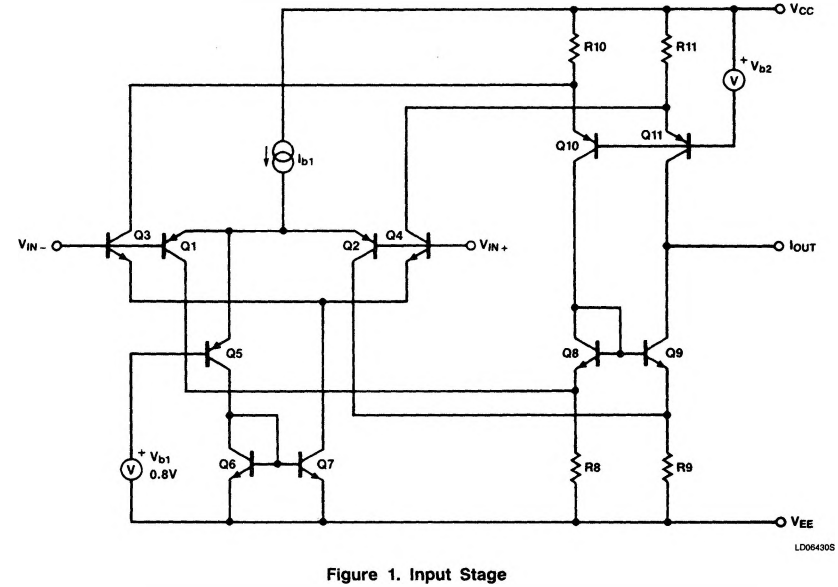


Figure 1. Input Stage

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base-emitter diodes of the output transistors Q1 and Q3. The base-emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base-emitter diode of Q7 and R7. The summed voltage across the base-emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} = I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in-phase driving signals on the bases of Q5 and Q2. This is very important for simple high-frequency compensation. The output transistors can be high-frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general-purpose op amp of this type must have enough open-loop gain for applications when the output is driving a low resistance load. The NE5230 accomplishes this by inserting an intermediate common-emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles — one at the output of each common-emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole-splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole-splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally-compensated op amp with a phase margin of 70 degrees.

THERMAL CONSIDERATIONS

When using the NE5230, the internal power dissipation capabilities of each package should be considered. Signetics does *not* recommend operation at die temperatures above 110°C in the SO package because of its inherently smaller package mass. Die temperatures of 150°C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

Where $T_A \equiv$ Ambient Temperature
T_J = Die Temperature
$P_D \equiv$ Power Dissipation
$= (I_{CC} \times V_{CC})$
$\theta_{JA} \equiv$ Package thermal resistance
$= 270°C/W$ for SO-8 in PC board mounting

See the packaging section for information regarding other methods of mounting.

$\theta_{JA} = 100°C/W$ for the plastic DIP;
$\theta_{JA} = 110°C/W$ for the ceramic DIP.

The maximum supply voltage for the part is 15V and the typical supply current is 1.1mA (1.6mA max). For operation at supply voltages other than the maximum, see the data

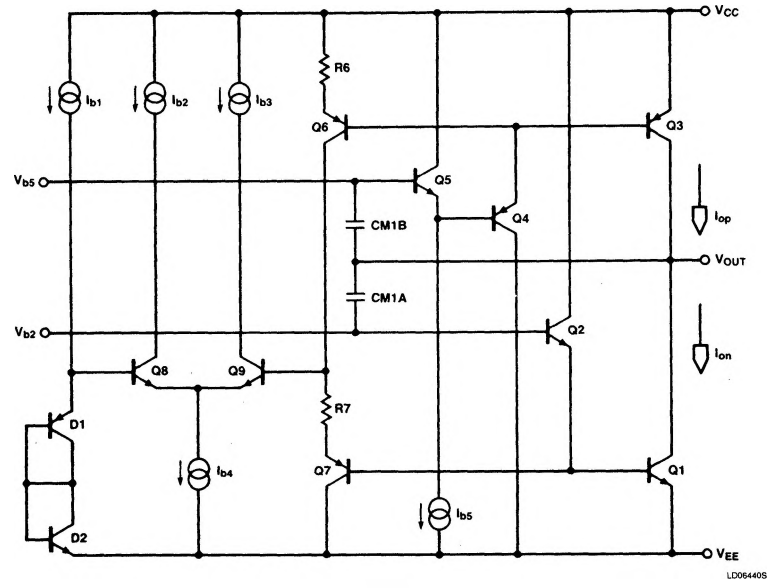


Figure 2. Output Stage

sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100μA between 25°C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower MTBF (Mean Time Between Failures). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

DESIGN TECHNIQUES AND APPLICATIONS

The NE5230 is a very user-friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC}. The programming of the current-control pin depends on the trade-offs which can be made in the designer's application. The graph in Figure 3 will help by showing bandwidth versus I_{CC}. As can be seen, the supply current can be varied anywhere over the range of 100μA to 600μA for a supply voltage of 1.8V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1Ω to 100kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain-bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5μs at low bias to 2μs at high bias. The supply current control can also be utilized for wave-shaping applications such as for pulse or triangular waveforms. The gain-bandwidth can be varied from between 250kHz at low bias to 600kHz at high bias current. The slew rate range is 0.08V/μs at low bias and 0.25V/μs at high bias.

The full output power bandwidth range for V_{CC} equals 2V, is above 40kHz for the maximum bias current setting and greater than 10kHz at the minimum bias current setting.

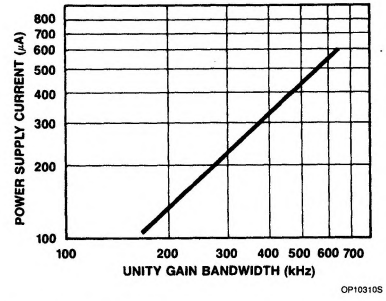
If extremely low signal distortion (< 0.05%) is required at low supply voltages, exclude the common-mode crossover point (V_{B1}) from the common-mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common-mode range of the amplifier. This leads to another helpful and unique property of the NE5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common-mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non-inverting voltage-follower configuration. This is shown in Figure 4 where the input sine wave allows an undistorted output sine wave which will swing less than 100mV of either supply voltage. Many competitive parts will show severe clipping caused by input common-mode limitations. The NE5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

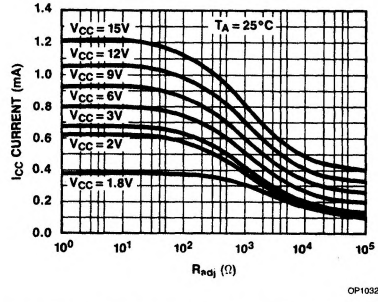
There are not as many considerations when designing with the NE5230 as with other devices. Since the NE5230 is internally-compensated and has a unity gain-bandwidth of 600kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NE5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low-pass RC network as close to the supply pins as possible to eliminate 60Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NE5230 is the same as the standard single op amp pinout with the exception of the bias current adjusting pin.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is



a. Unity Gain Bandwidth vs Power Supply Current for $V_{CC} = \pm 0.9V$



b. I_{CC} Current vs Bias Current Adjusting Resistor for Several Supply Voltages

Figure 3