

# NCP1203

## Advance Information

# PWM Current-Mode Controller for Universal Off-Line Supplies Featuring Standby and Short Circuit Protection

Housed in SO-8 or DIP8 package, the NCP1203 represents a major leap toward ultra-compact Switch-Mode Power Supplies and represents an excellent candidate to replace the UC384X devices. Thanks to its proprietary SmartMOS Very High Voltage Technology, the circuit allows the implementation of complete off-line AC/DC adapters, battery charger and a high-power SMPS with few external components.

With an internal structure operating at a fixed 40 kHz, 60 kHz or 100 kHz switching frequency, the controller features a high-voltage start-up FET which ensures a clean and loss-less start up sequence. Its current-mode control naturally provides good audio-susceptibility and inherent pulse-by-pulse control.

When the current set point falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so-called skip cycle mode and provides improved efficiency at light loads while offering excellent performance in standby conditions. Because this occurs at a user adjustable low peak current, no acoustic noise takes place.

The NCP1203 also includes an efficient protective circuitry which, in presence of an output over load condition, disables the output pulses while the device enters a safe burst mode, trying to restart. Once the default has gone, the device auto-recovers. Finally, a temperature shutdown with hysteresis helps building safe and robust power supplies.

### Features

- High-Voltage Start Up Current Source
- Auto-Recovery Internal Output Short-Circuit Protection
- Extremely Low No-Load Standby Power
- Current-Mode with Adjustable Skip-Cycle Capability
- Internal Leading Edge Blanking
- 250 mA Peak Current Capability
- Internally Fixed Frequency at 40 kHz, 61 kHz and 100 kHz
- Direct Optocoupler Connection
- Undervoltage Lockout at 7.6 V Typical
- SPICE Models Available for TRANSient and AC Analysis
- Pin to Pin Compatible with NCP1200

### Applications

- AC/DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

This document contains information on a new product. Specifications and information herein are subject to change without notice.



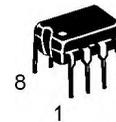
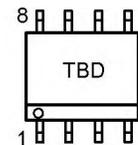
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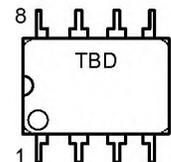
### MARKING DIAGRAMS



SO-8  
D1, D2 SUFFIX  
CASE 751

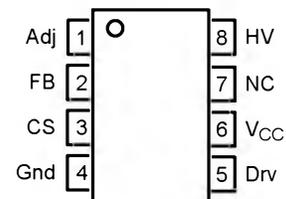


PDIP-8  
N SUFFIX  
CASE 626



xx = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

| Device         | Package | Shipping         |
|----------------|---------|------------------|
| NCP1203P60     | PDIP8   | 50 Units/Tube    |
| NCP1203D60R2   | SO-8    | 2500/Tape & Reel |
| NCP1203P40     | PDIP8   | 50 Units/Tube    |
| NCP1203D40R2   | SO-8    | 2500/Tape & Reel |
| NCP1203P100*   | PDIP8   | 50 Units/Tube    |
| NCP1203D100R2* | SO-8    | 2500/Tape & Reel |

\* Intro Pending Q1, 2002

## NCP1203

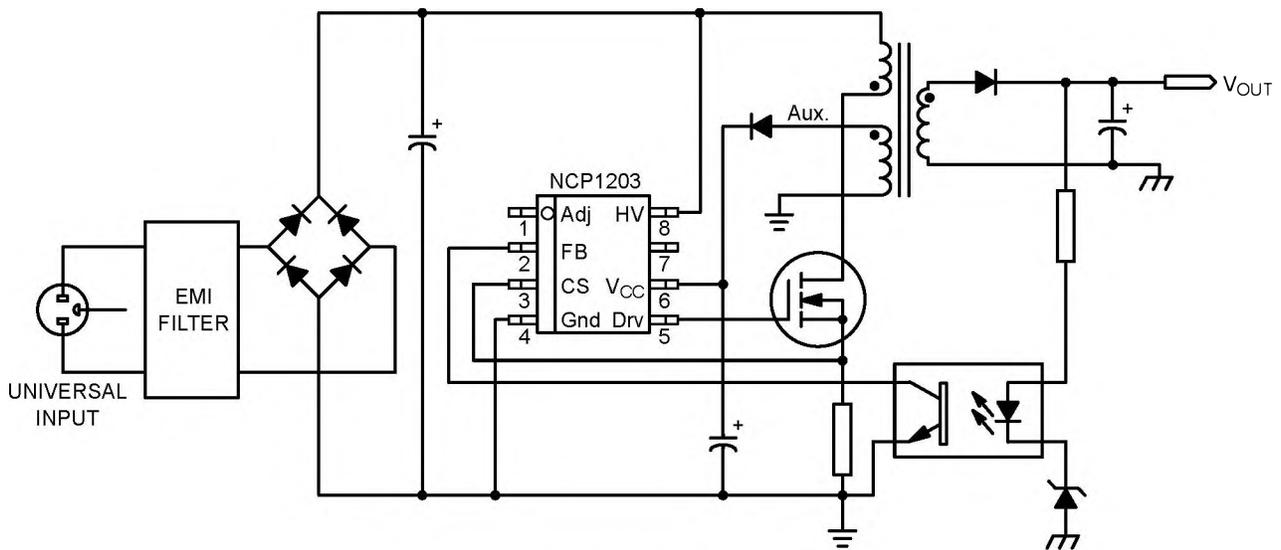


Figure 1. Typical Application Example

### PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Function                                      | Pin Description  |
|---------|----------|---|--|
| 1       | Adj      | Adjust the skipping peak current              | This pin lets you adjust the level at which the cycle skipping process takes place. Shorting this pin to ground, permanently disables the skip cycle feature.              |
| 2       | FB       | Sets the peak current setpoint                | By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand. Skip cycle occurs when FB falls below $V_{pin1}$ . |
| 3       | CS       | Current sense input                           | This pin senses the primary current and routes it to the internal comparator via an L.E.B.   |
| 4       | Gnd      | The IC ground                                 | –  |
| 5       | Drv      | Driving pulses                                | The driver's output to an external MOSFET.   |
| 6       | Vcc      | Supplies the IC                               | This pin is connected to an external bulk capacitor of typically 22 $\mu$ F.   |
| 7       | NC       | –   | This unconnected pin ensures adequate creepage distance.   |
| 8       | HV       | Ensure a clean and lossless start up sequence | Connected to the high-voltage rail, this pin injects a constant current into the Vcc capacitor during the start up sequence.   |

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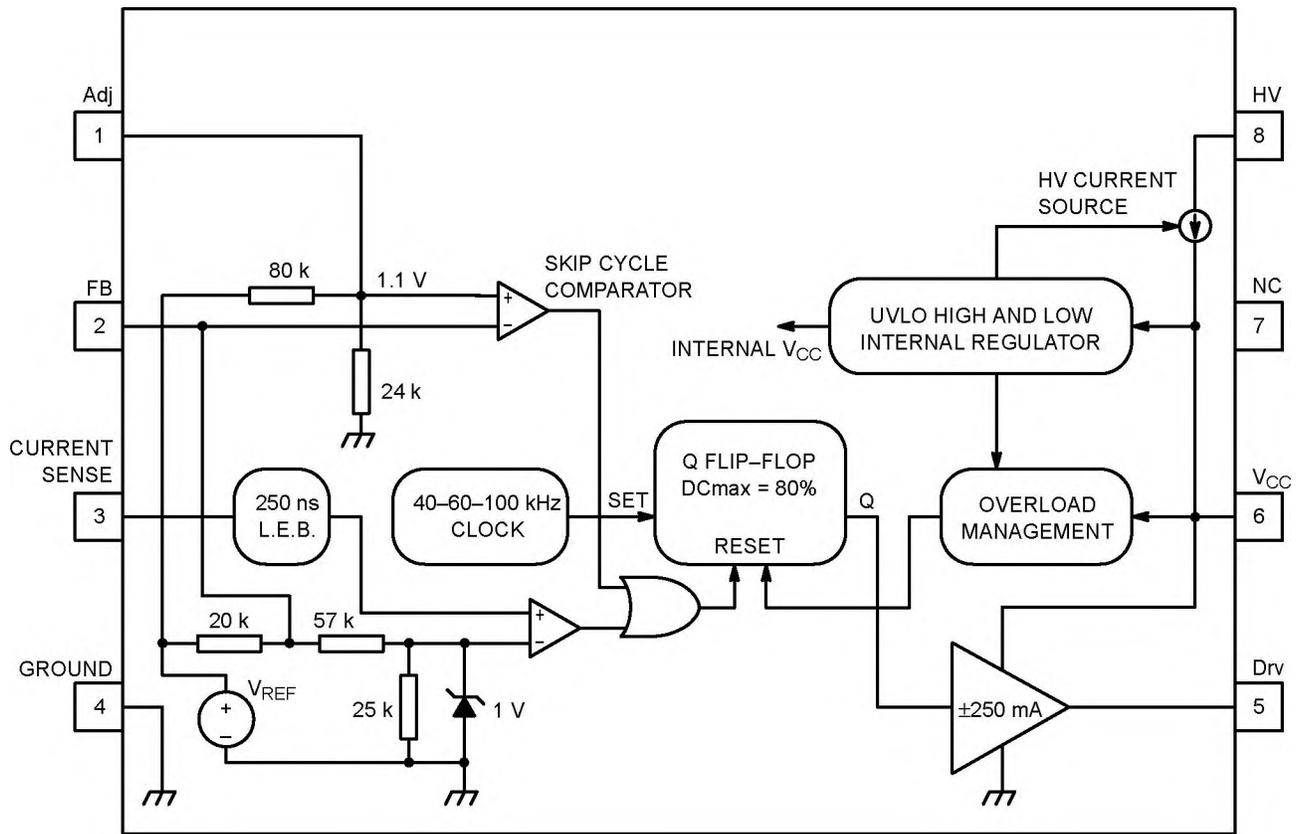


Figure 2. Internal Circuit Architecture

## MAXIMUM RATINGS

| Rating   | Symbol            | Value       | Unit |
|--|-------------------|-------------|------|
| Power Supply Voltage   | V <sub>CC</sub>   | 16          | V    |
| Thermal Resistance Junction-to-Air, PDIP8 Version                                      | R <sub>θJA</sub>  | 100         | °C/W |
| Thermal Resistance Junction-to-Air, SOIC Version                                       | R <sub>θJA</sub>  | 178         | °C/W |
| Maximum Junction Temperature   | T <sub>JMAX</sub> | 150         | °C   |
| Temperature Shutdown (60 kHz)  | -                 | 170         | °C   |
| Hysteresis in Shutdown   | -                 | 30          | °C   |
| Storage Temperature Range  | -                 | -60 to +150 | °C   |
| ESD Capability, HBM Model (All pins except V <sub>CC</sub> and HV)                     | -                 | 2.0         | KV   |
| ESD Capability, Machine Model  | -                 | 200         | V    |
| Maximum Voltage on Pin 8 (HV), Pin 6 (V <sub>CC</sub> ) Grounded                       | -                 | 450         | V    |
| Maximum Voltage on Pin 8 (HV), Pin 6 (V <sub>CC</sub> ) Decoupled to Ground with 10 μF | -                 | 500         | V    |

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**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = 0^\circ\text{C}$  to  $+125^\circ\text{C}$ , Max  $T_J = 150^\circ\text{C}$ ,  $V_{CC} = 11\text{ V}$  unless otherwise noted.)

| Characteristic | Symbol | Pin | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|-----|------|

## Supply Section (All frequency versions, otherwise noted)

|   |               |   |      |      |                 |               |
|---|---------------|---|------|------|-----------------|---------------|
| Turn-on Threshold Level, $V_{CC}$ Going Up                                      | $V_{CCOFF}$   | 6 | 12.2 | 12.8 | 14              | V             |
| Minimum Operating Voltage after Turn-on   | $V_{CC(min)}$ | 6 | 7.2  | 7.8  | 8.4             | V             |
| $V_{CC}$ Decreasing Level at which the Latch-off Phase Ends                     | $V_{CClatch}$ | 6 | –    | 4.9  | –               | V             |
| Internal IC Consumption, No Output Load on Pin 6                                | $ICC1$        | 6 | –    | 750  | 880<br>(Note 1) | $\mu\text{A}$ |
| Internal IC Consumption, 1.0 nF Output Load on Pin 6, $F_{SW} = 40\text{ kHz}$  | $ICC2$        | 6 | –    | 1.2  | 1.4<br>(Note 2) | mA            |
| Internal IC Consumption, 1.0 nF Output Load on Pin 6, $F_{SW} = 60\text{ kHz}$  | $ICC2$        | 6 | –    | 1.4  | 1.6<br>(Note 2) | mA            |
| Internal IC Consumption, 1.0 nF Output Load on Pin 6, $F_{SW} = 100\text{ kHz}$ | $ICC2$        | 6 | –    | 2.0  | 2.2<br>(Note 2) | mA            |
| Internal IC Consumption, Latch-off Phase, $V_{CC} = 6.0\text{ V}$               | $ICC3$        | 6 | –    | 350  | –               | $\mu\text{A}$ |

## Internal Start Up Current Source (Pin 8 biased at 50 V)

|   |       |   |     |     |     |    |
|---|-------|---|-----|-----|-----|----|
| High-Voltage Current Source, $V_{CC} = 10\text{ V}$ | $IC1$ | 8 | 4.5 | 7.0 | 9.0 | mA |
| High-Voltage Current Source, $V_{CC} = 0$           | $IC2$ | 8 | –   | 13  | –   | mA |

## Drive Output

|   |          |   |     |    |    |          |
|---|----------|---|-----|----|----|----------|
| Output Voltage Rise-Time @ $CL = 1.0\text{ nF}$ , 10–90% of Output Signal | $T_r$    | 5 | –   | 67 | –  | ns       |
| Output Voltage Fall-Time @ $CL = 1.0\text{ nF}$ , 10–90% of Output Signal | $T_f$    | 5 | –   | 28 | –  | ns       |
| Source Resistance   | $R_{OH}$ | 5 | 27  | 40 | 61 | $\Omega$ |
| Sink Resistance   | $R_{OL}$ | 5 | 5.0 | 12 | 20 | $\Omega$ |

## Current Comparator (Pin 5 loaded unless otherwise noted)

|  |             |   |      |      |     |               |
|--|-------------|---|------|------|-----|---------------|
| Input Bias Current @ 1.0 V Input Level on Pin 3            | $I_{IB}$    | 3 | –    | 0.02 | –   | $\mu\text{A}$ |
| Maximum Internal Current Setpoint (Note 3)                 | $I_{Limit}$ | 3 | 0.85 | 0.92 | 1.0 | V             |
| Default Internal Current Setpoint for Skip Cycle Operation | $I_{Lskip}$ | 3 | –    | 360  | –   | mV            |
| Propagation Delay from Current Detection to Gate OFF State | $T_{DEL}$   | 3 | –    | 90   | 160 | ns            |
| Leading Edge Blanking Duration (Note 3)                    | $T_{LEB}$   | 3 | –    | 230  | –   | ns            |

## Internal Oscillator ( $V_{CC} = 11\text{ V}$ , pin 5 loaded by 1 nF)

|  |           |   |    |     |     |     |
|--|-----------|---|----|-----|-----|-----|
| Oscillation Frequency, 40 kHz Version  | $f_{OSC}$ | – | 37 | 42  | 47  | kHz |
| Oscillation Frequency, 60 kHz Version  | $f_{OSC}$ | – | 57 | 65  | 73  | kHz |
| Oscillation Frequency, 100 kHz Version | $f_{OSC}$ | – | 90 | 103 | 115 | kHz |
| Maximum Duty-Cycle                     | $D_{max}$ | – | 74 | 80  | 87  | %   |

## Feedback Section ( $V_{CC} = 11\text{ V}$ , pin 5 unloaded)

|  |             |   |   |     |   |            |
|--|-------------|---|---|-----|---|------------|
| Internal Pull-up Resistor                | $R_{up}$    | 2 | – | 20  | – | k $\Omega$ |
| Pin 3 to Current Setpoint Division Ratio | $I_{ratio}$ | – | – | 3.3 | – | –          |

## Skip Cycle Generation

|                                 |            |   |     |     |     |            |
|---------------------------------|------------|---|-----|-----|-----|------------|
| Default Skip Mode Level         | $V_{skip}$ | 1 | 1.0 | 1.2 | 1.4 | V          |
| Pin 1 Internal Output Impedance | $Z_{out}$  | 1 | –   | 22  | –   | k $\Omega$ |

1. Max value at  $T_J = 0^\circ\text{C}$ .
2. Maximum value @  $T_J = 25^\circ\text{C}$ , please see characterization curves.
3. Pin 5 loaded by 1 nF.

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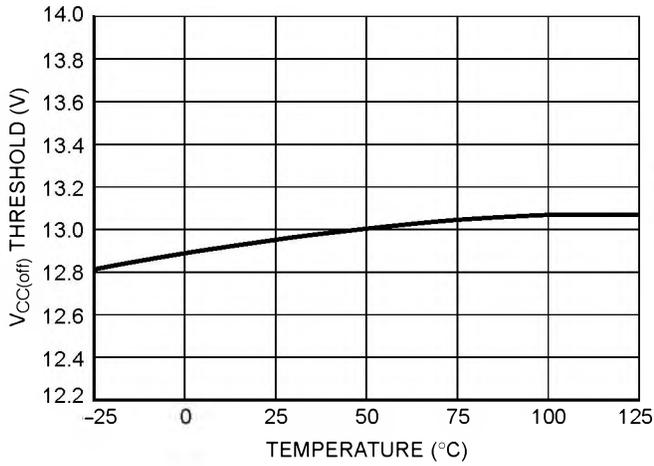


Figure 3.  $V_{CC(off)}$  Threshold versus Temperature

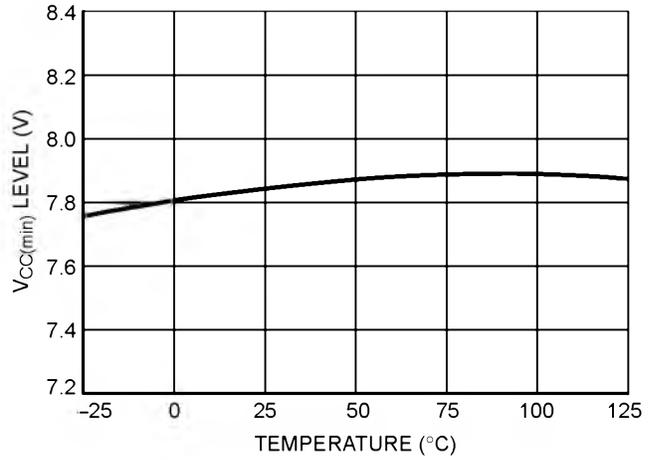


Figure 4.  $V_{CC(min)}$  Level versus Temperature

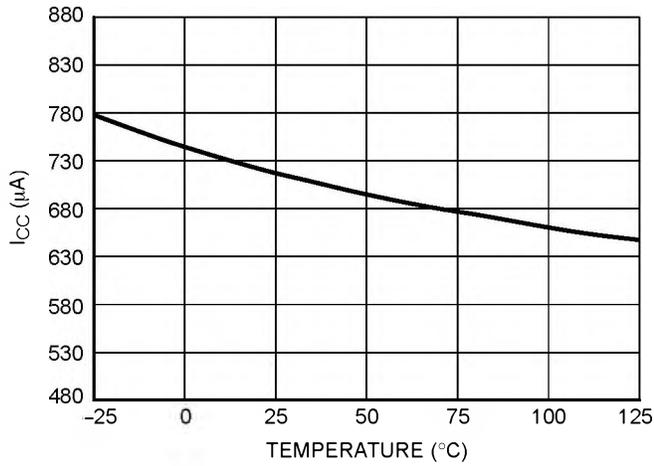


Figure 5.  $I_{CC}$  Current Consumption (No Load) versus Temperature

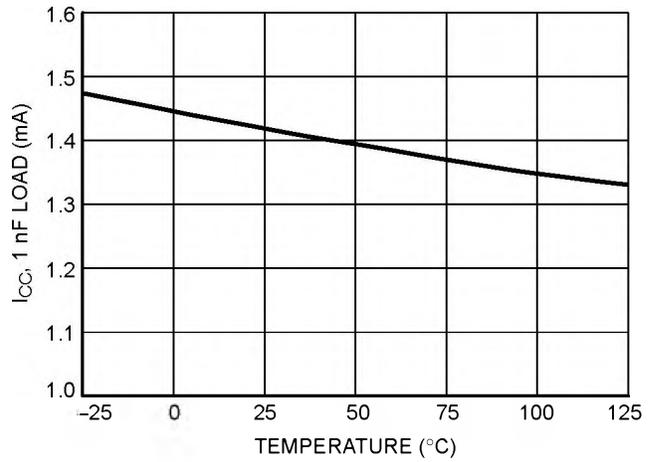


Figure 6.  $I_{CC}$  Consumption (Loaded by 1 nF) versus Temperature

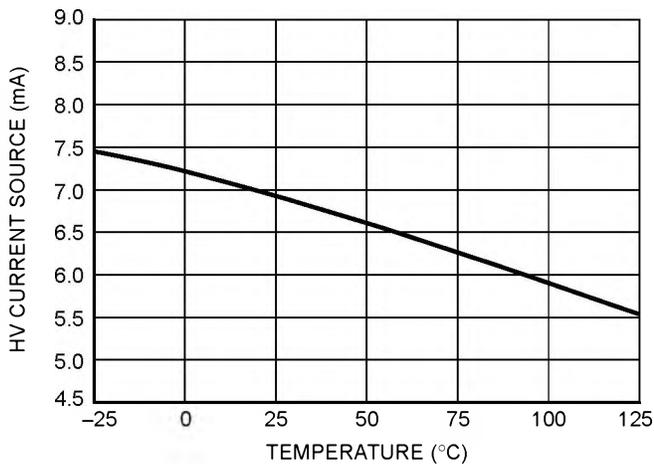


Figure 7. HV Current Source at  $V_{CC} = 10$  V versus Temperature

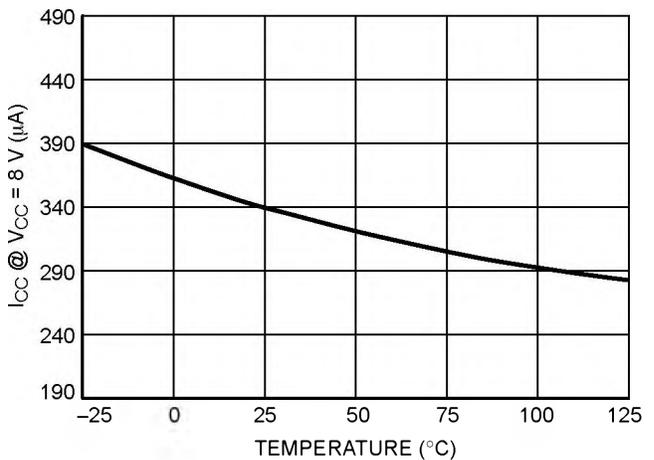


Figure 8.  $I_{CC}$  Consumption at  $V_{CC} = 8$  V versus Temperature

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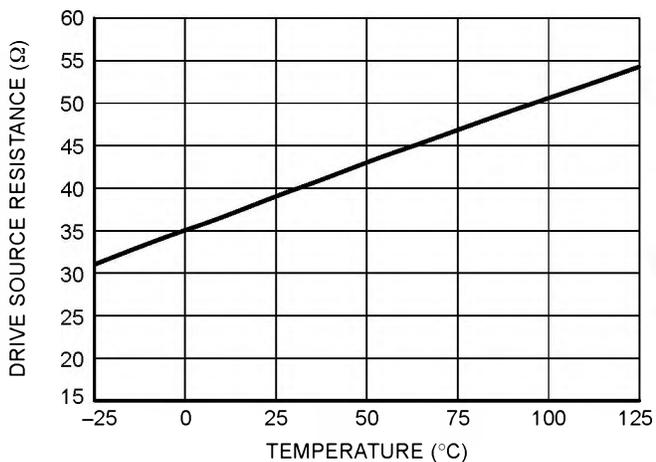


Figure 9. Drive Source Resistance versus Temperature

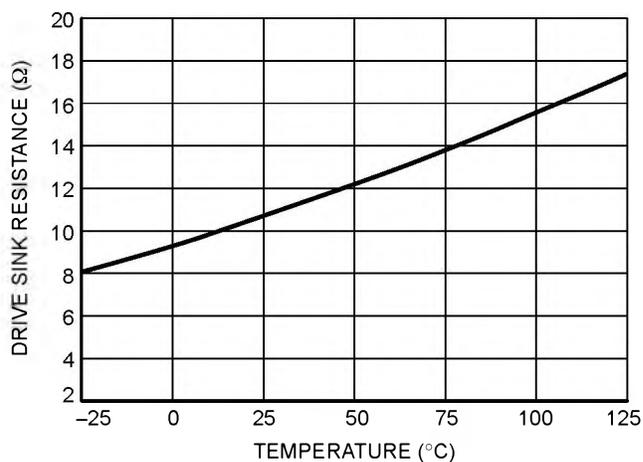


Figure 10. Drive Sink Resistance versus Temperature

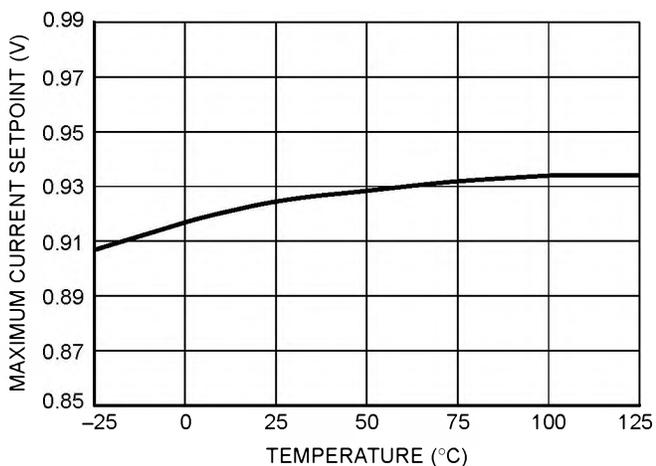


Figure 11. Maximum Current Setpoint versus Temperature

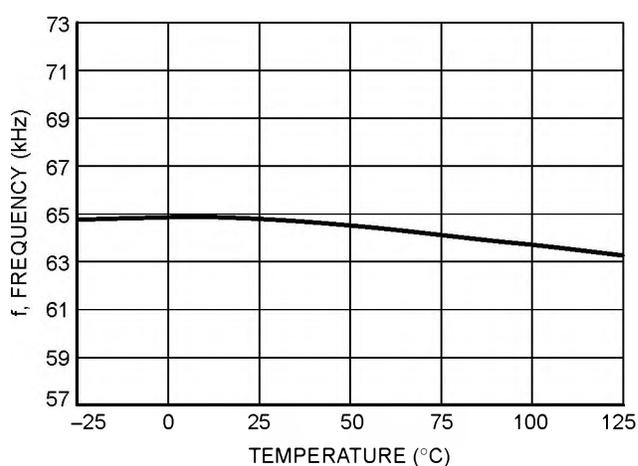


Figure 12. Frequency versus Temperature

APPLICATION INFORMATION

Introduction

The NCP1203 implements a standard current mode architecture where the switch-off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part-count is the key parameter, particularly in low-cost AC/DC adapters, auxiliary supplies etc. Thanks to its high-performance SmartMOS High-Voltage technology, the NCP1203 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low-pass filter and start up device. This later point emphasizes the fact that ON Semiconductor's NCP1203 does not need an external start up resistance but supplies the start up current directly from the high-voltage rail. On the other hand, more and more applications are requiring low no-load standby power, e.g. for AC/DC adapters, VCRs etc. UC384X series have a lot of difficulty to reduce the switching losses at low power levels. NCP1203 elegantly solves this problem by

skipping unwanted switching cycles at a user-adjustable power level. By ensuring that skip cycles take place at low peak current, the device ensures quiet, noise free operation. Finally, an auto-recovery output short-circuit protection (OCP) prevents from any lethal thermal runaway in overload conditions.

Start-Up Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 4.0 mA) is biased and charges up the V<sub>CC</sub> capacitor. When the voltage on this V<sub>CC</sub> capacitor reaches the V<sub>CC</sub>OFF level (typically 12.8 V), the current source turns off and no longer wastes any power. At this time, the V<sub>CC</sub> capacitor only supplies the controller and the auxiliary supply is supposed to take over before V<sub>CC</sub> collapses below V<sub>CC</sub>(min). Figure 13 shows the internal arrangement of this structure:

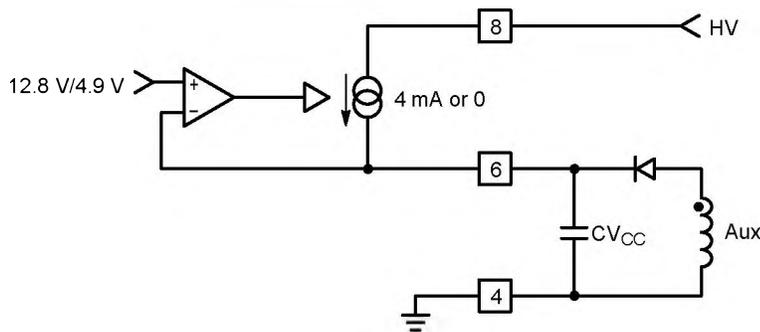


Figure 13. The Current Source Brings V<sub>CC</sub> Above 12.8 V and then Turns Off

Once the power supply has started, the V<sub>CC</sub> shall be constrained below 16 V, which is the maximum rating on pin 6. Figure 14 portrays a typical start up sequence with a V<sub>CC</sub> regulated at 12.5 V:

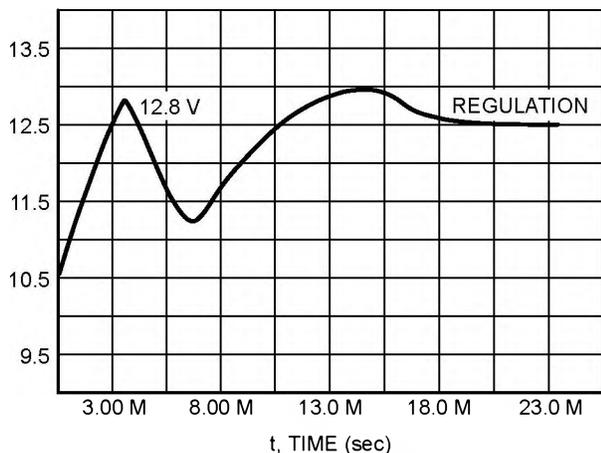


Figure 14. A Typical Start Up Sequence for the NCP1203

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short-circuit protection. A short-circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the auxiliary voltage also decreases because it also operates in Flyback and thus duplicates the output voltage, providing the leakage inductance between windings is kept low. To account for this situation and properly protect the power supply, NCP1203 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty-cycle. The system auto-recovers when the fault condition disappears.

During the start-up phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. The auxiliary voltage takes place after a few switching cycles and self-supplies the IC. In presence of a short circuit on the output, the auxiliary voltage will go down until it crosses the undervoltage

lockout level of typically 7.6 V. When this happens, NCP1203 immediately stops the switching pulses and unbiases all unnecessary logical blocks. The overall consumption drops, while keeping the gate grounded, and the Vcc slowly falls down. As soon as Vcc reaches typically 4.6 V, the start up source turns-on again and a new start up

sequence occurs, bringing Vcc toward 12.8 V as an attempt to restart. If the default has gone, then the power supply normally restarts. If not, a new protective burst is initiated, shielding the SMPS from any runaway. Figure 15 portrays the typical operating signals in short circuit:

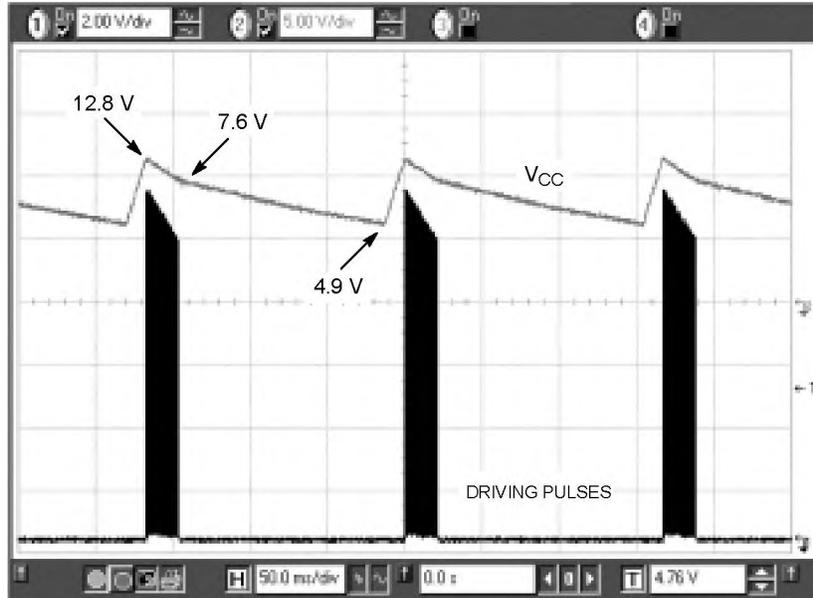


Figure 15. Typical Waveforms in Short Circuit Conditions

**Calculating the Vcc Capacitor**

The Vcc capacitor can be calculated knowing the IC consumption as soon as Vcc reaches 12.8 V. Suppose that a NCP1203P60 is used and drives a MOSFET with a 30 nC total gate charge (Qg). The total average current is thus made of Icc1 (700 μA) plus the driver current, Fsw x Qg or 1.8 mA. The total current is therefore 2.5 mA. The ΔV available to fully start up the circuit (e.g. never reach the 7.6 V UVLO during power on) is 12.8–7.6 = 5.2 V. We have a capacitor who then needs to supply the NCP1203 with 2.5 mA during a given time until the auxiliary supply takes over. Suppose that this time was measured at around 15 ms.

CVcc is calculated using the equation  $C = \frac{\Delta t \cdot i}{\Delta V}$  or  $C \geq 7.2 \mu F$ . Select a 10 μF/16 V and this will fit.

**Skipping Cycle Mode**

The NCP1203 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level (Vpin 1), the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so-called skip cycle mode, also named controlled burst operation. The power transfer now

depends upon the width of the pulse bunches (Figure 17). Suppose we have the following component values:

- Lp, primary inductance = 350 μH
- Fsw, switching frequency = 61 kHz
- Ip skip = 600 mA (or 333 mV/Rsense)

The theoretical power transfer is therefore:

$$\frac{1}{2} \cdot L_p \cdot I_p^2 \cdot F_{sw} = 3.8 W$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: 3.8 . 0.1 = 380 mW.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:

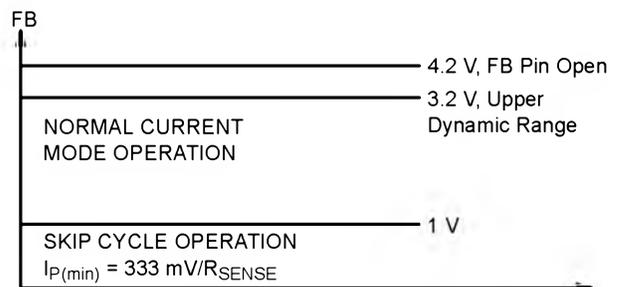


Figure 16.

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When FB is above the skip cycle threshold (1.0 V by default), the peak current cannot exceed 1.0 V/R<sub>sense</sub>. When the IC enters the skip cycle mode, the peak current cannot go below V<sub>pin1</sub>/3.3. The user still has the flexibility

to alter this 1.0 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level. Grounding pin 1 permanently invalidates the skip cycle operation.

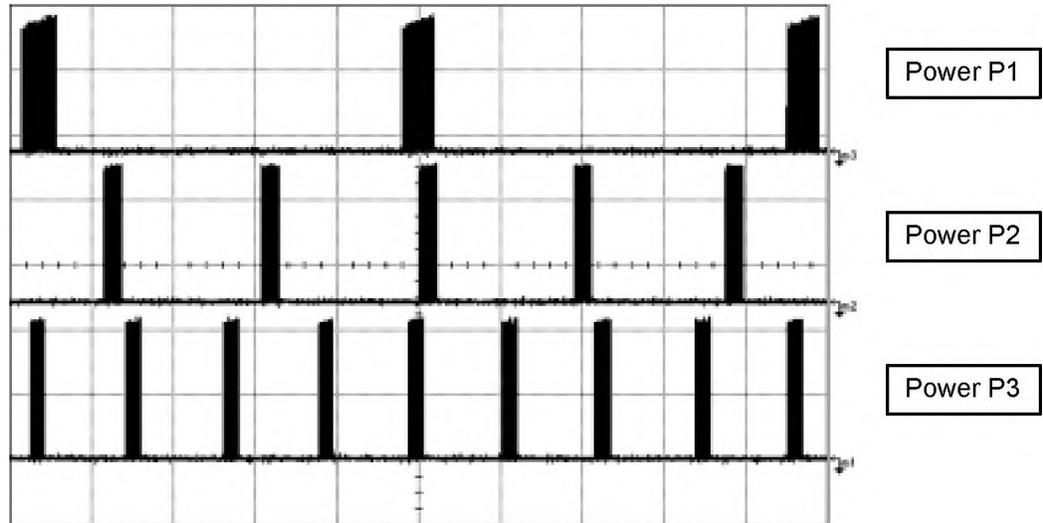


Figure 17. Output Pulses at Various Power Levels (X = 5.0  $\mu$ s/div) P1 < P2 < P3

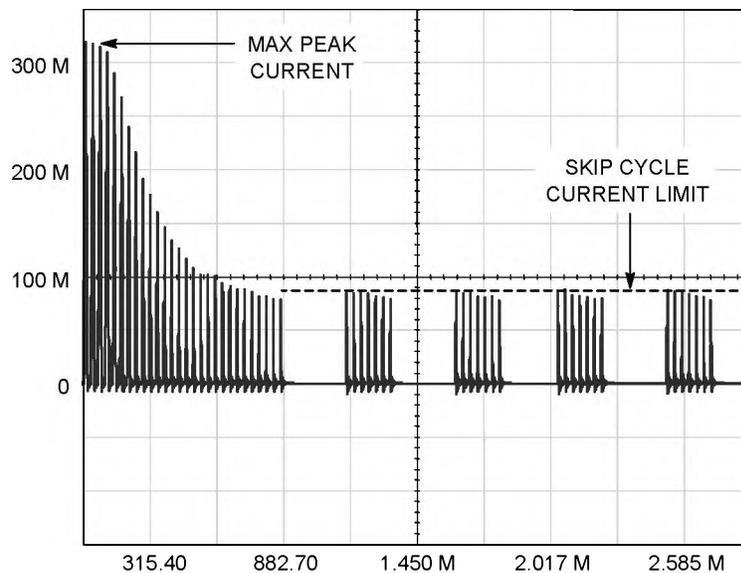


Figure 18. The Skip Cycle Takes Place at Low Peak Currents which Guaranties Noise-Free Operation

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We recommend a pin1 operation between 400 mV and 1.3 V that will fix the skip peak current level between 120 mV/Rsense and 390 mV/Rsense.

### Non-Latching Shutdown

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has

disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the Adj pin 1 level, the output pulses are disabled as long as FB is pulled below pin 1. As soon as FB is relaxed, the IC resumes its operation. Figure 9 depicts the application example:

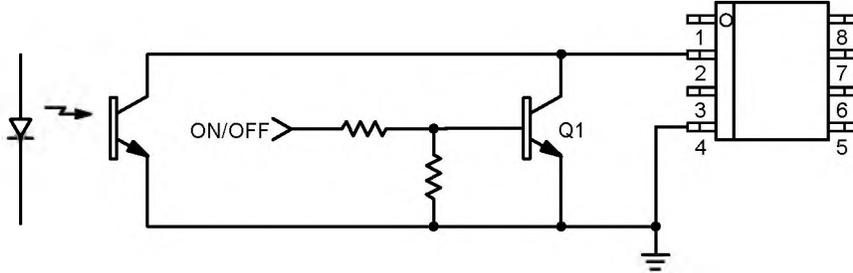


Figure 19. Another Way of Shutting Down the IC without a Definitive Latch-Off State

### Full Latching Shutdown

Other applications require a full latching shutdown, e.g. when an abnormal situation is detected (over temp or overvoltage). This feature can easily be implemented through two external transistors wired as a discrete SCR.

When the Vcc level exceeds the zener breakdown voltage, the NPN biases the PNP and fires the equivalent SCR, permanently bringing down the FB pin. The switching pulses are disabled until the user unplugs the power supply.

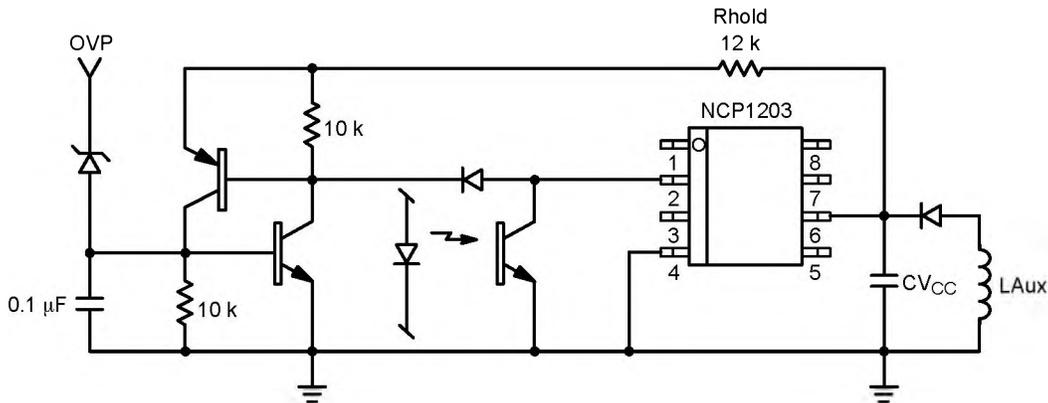


Figure 20. Two Bipolars Ensure a Total Latch-Off of the SMPS in Presence of an OVP

Rhold ensures that the SCR stays on when fired. The bias current flowing through Rhold should be small enough to let the Vcc ramp up (12.8 V) and down (4.6 V) when the SCR is fired. The NPN base can also receive a signal from a

temperature sensor. Typical bipolars can be MMBT2222 and MMBT2907 for the discrete latch. The MMBT3946 features two bipolars NPN+PNP in the same package and could also be used.