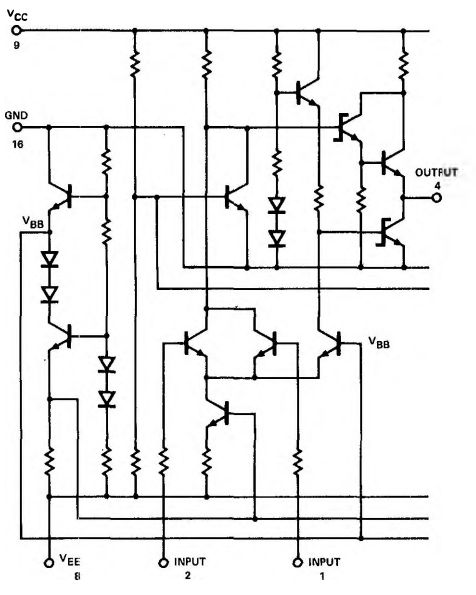
DESCRIPTION

Four level translators for converting ECL signal levels to TTL or DTL logic levels. The 1068 incorporates familiar Schottky "totem pole" outputs to provide high speed operation.

FEATURES

- FAST PROPAGATION DELAY = 5.0 ns TYP
- POWER DISSIPATION = 360 mW/PACKAGE TYP
- SCHOTTKY TTL TOTEM POLE OUTPUTS
- RECOMMENDED POWER SUPPLIES:
  - V_{CC} = +5.0 V DC ±5%
  - V_{EE} = −5.2 V DC ±5%
- FOUR TRANSLATORS PER PACKAGE

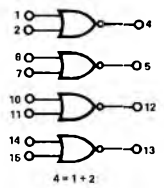
CIRCUIT SCHEMATIC



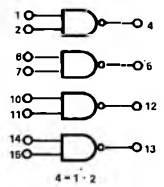
(ONE OF FOUR TRANSLATOR CIRCUITS SHOWN)

LOGIC DIAGRAM AND PIN CONFIGURATION

POSITIVE LOGIC



NEGATIVE LOGIC



Gnd = 16
V_{CC} (+5.0 Vdc) = 9
V_{EE} (−5.2 Vdc) = 8

DC Input Loading Factor = 2.5 (ECL)
DC Output Loading Factor = 10 (TTL)

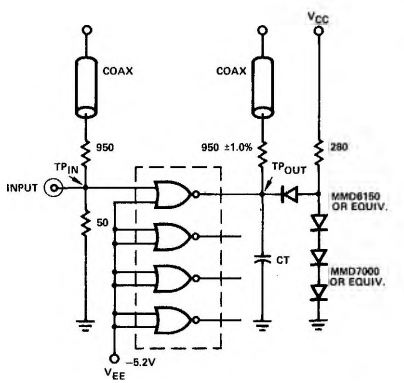
ELECTRICAL CHARACTERISTICS

Test procedures are shown for one translator. The other translators are tested in the same manner.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES						
	Volts					mAdc	
	V_{IL} min to V_{IL} max	V_{IH} min to V_{IH} max	V_{IH} max	V_{CC}	V_{EE}	I_{OL}	I_{OH}
0°C	−5.2 to −1.378	−1.046 to −0.740	–	+5.0	−5.2	2-	−2.0
1068 +25°C	−5.2 to −1.350	−1.000 to −0.700	−0.700	+5.0	−5.2	20	2.0
75°C	−5.2 to −1.285	−0.925 to −0.625	–	+5.0	−5.2	20	−2.0

Characteristic	Symbol	Pin Under Test	N1068 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IL} min to V_{IL} max	V_{IH} min to V_{IH} max	V_{IH} max	V_{CC}	V_{EE}	I_{OL}	I_{OH}	Gnd
Positive Supply Drain Current	I_{CCH}	9	–	–	–	60	–	–	mAdc	–	–	1,2,6,7,10,14,15	9	8	–	–	16
	I_{CCL}	9	–	–	–	45	–	–	mAdc	–	–	–	9	1,2,6,7,8,10,11,14,15	–	–	16
Negative Supply Drain Current	I_E	8	–	–	–	60	–	–	mAdc	–	–	–	–	1,2,6,7,8,10,11,14,15	–	–	16
Input Current	I_{in}	1	–	–	–	250	–	–	µAdc	–	1	–	9	2,6,7,8,10,11,14,15	–	–	16
		2	–	–	–	250	–	–	µAdc	–	2	–	9	1,6,7,8,10,11,14,15	–	–	16
Input Leakage Current	I_R	1	–	–	–	0.5	–	1.0	µAdc	–	–	–	9	1,8	–	–	16
		2	–	–	–	0.5	–	1.0	µAdc	–	–	–	9	2,8	–	–	16
Output Voltage High	V_{OH}	4	2.4	–	2.4	–	2.4	–	Vdc	2	–	–	9	8	–	3	16
		4	2.4	–	2.4	–	2.4	–	Vdc	1	–	–	9	8	–	3	16
Output Voltage Low	V_{OL}	4	–	0.6	–	0.6	–	0.6	Vdc	–	1	–	9	2,6,7,8,10,11,14,15	3	–	16
		4	–	0.6	–	0.5	–	0.5	Vdc	–	2	–	9	1,6,7,8,10,11,14,15	3	–	16
Output Short Circuit Current	I_{SC}	4	-30	-90	-30	-90	-30	90	mAdc	–	–	–	9	1,2,6,7,8,10,11,14,15	–	–	3,16
			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out						
Switching Times	t_{1-4+}	4			5.0				ns	1	4	–	9	2,6,7,8,10,11,14,15	–	–	16
	t_{1+4-}	↓	–	–	↓	–	–	–	↓	1	↓	–	↓	2,6,7,8,10,11,14,15	–	–	↓
	t_{2-4+}		–	–		–	–	–		2		–		1,6,7,8,10,11,14,15	–	–	
	t_{2+4-}		–	–		–	–	–		2		–		1,6,7,8,10,11,14,15	–	–	

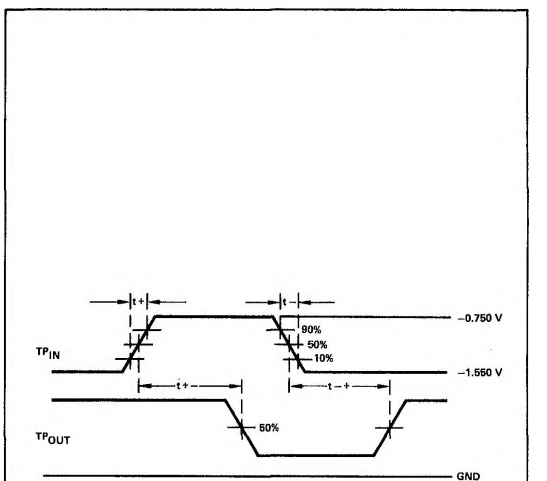
SWITCHING TIME TEST CIRCUIT



INPUT PULSE

t^+, t^- = 2.0 ± 0.2ns

WAVEFORM@ 25°C



The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

ECL 1,000/10,000 SERIES PRODUCT INFORMATION

10,000 SERIES ADVANTAGES

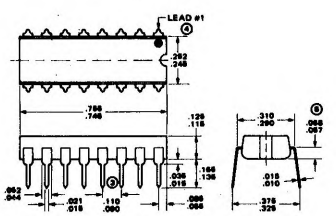
- Best system cost — Performance available in a standard integrated circuit family.
- Factor of 2-or-more — higher system performance than Schottky TTL.
- Complete family of SS1, interface elements, and high performance MS1, with memories coming soon.
- ECL 10,000 Series includes MECL 10,000 equivalents and Signetics-originated 10,000 Series designs.
- Offers designers the logic power of ECL — Open emitter logic, simultaneous complementary outputs, transmission line capability.
- Offers designers system-optimized circuit characteristics — Excellent speed power product, excellent propagation delay/rise time ratio, excellent noise immunity/noise generation ratio, transmission line capability, differential interface capability, and high immunity from power supply variations (±5% recommended, ±10% results in minimal change in system characteristics).
- Compatible with transmission line environment, two-sided printed circuit boards, standard fan cooling techniques. Less support hardware required than Schottky TTL for many system designs.
- Low noise generation capability — Complementary balanced-load outputs, optimized propagation delay/rise time ratio, minimum "1"/"0" power imbalance.
- Directly compatible with MECL III family. Also compatible with ECL II/MECL II family with some reduction in noise immunity at the interface.
- These products contain a temperature compensated internal bias which ensures that the threshold point tracks with the center of the transition region over temperature.

10,000 SERIES TECHNOLOGY

- Signetics thin-epitaxial high performance, high volume production process.
- Advanced circuit design techniques used:
  - Internal Emitter-Dot 'OR' Logic
  - Internal Collector-Dot 'AND' Logic
  - Internal Stacked Series Gating
  - Single Stage Delay Exclusive OR Gates

PACKAGE INFORMATION

B PACKAGE



NOTES:

1. Lead Material: Nickel, tin plated
2. Body Material: Silicone molded
3. Tolerances non-cumulative
4. Signetics symbol denotes Lead No. 1
5. Lead spacing shall be measured within this zone
6. Body dimensions do not include molding flash

PACKAGE TYPES

- SSI, MSI and memories will be available in cerdip packages. Signetics new designation F specifies cerdip packages or any number of leads. (Previously E specified 16 lead cerdip).
- Presently SSI, and later some MSI and memories will be available in Signetics' double-encapsulated silicone dip with nickel lead frame. This provides minimum thermal resistance and hence maximum thermal compatibility with cerdip packages.

MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Supply Voltage (V_{CC} = 0)	Note 1	V_{EE}	-8	Vdc
Input Voltage (V_{CC} = 0)	Note 1	V_{IN}	0 to V_{EE}	Vdc
Output Source Current	Note 1	I_o		
Continuous			50	mAdc
Surge			100	mAdc
Storage Temperature Range	Note 1	T_{stg}	-65 to +125	°C
Operating Junction Temperature	Note 1	T_J	125	°C
Operating Temperature Range	Note 2	T_A	-30 to +85	°C
DC Fan-Out (Gates and Flip-Flops)	Notes 2,3	—	70	—
Power Supply Regulation Required	Note 2	—	±10%	—

NOTES:

1. Ratings above which device life may be impaired.
2. Recommended maximum rating above which performance may be degraded.
3. AC fan-out is defined by desired system performance.

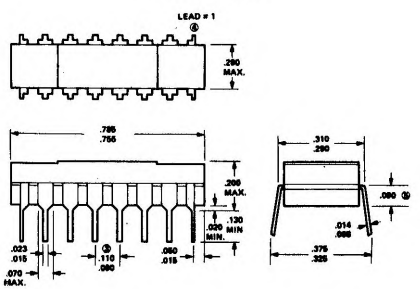
ORDERING INFORMATION

101XX F — Specifies a 10,000 Series product in Cerdip Dual-in-Line package, operating temperature range -30°C to +85°C (intermediate Range). (F is Signetics' new designation for Cerdip).

101XX B — Specifies a 10,000 Series product in 16 pin Silicone Dual-in-Line package, operating temperature range -30°C to +85°C (intermediate Range).

Availability of a device in a particular package is indicated on the appropriate product Data Sheet.

F PACKAGE

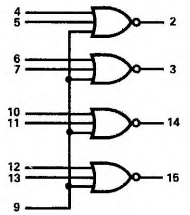


NOTES:

1. Lead Material: Alloy 42 or equivalent, tin plated
2. Body Material: Ceramic with glass seal
3. Tolerances non-cumulative
4. Signetics symbol denotes lead No. 1
5. Lead spacing shall be measured within this zone

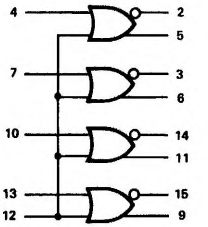
LOGIC DIAGRAMS: BASIC GATES

10100
QUAD 3-INPUT NOR



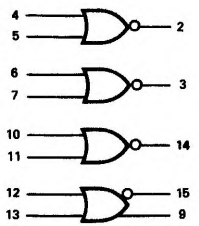
t_{pd} = 2.0 ns TYP.

10101
QUAD OR/NOR



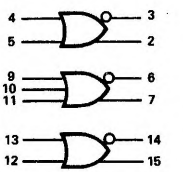
t_{pd} = 2.0 ns TYP.

10102
QUAD 2-INPUT NOR



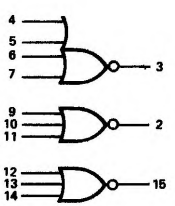
t_{pd} = 2.0 ns TYP.

10105
TRIPLE 2, 3, 2-INPUT OR/NOR



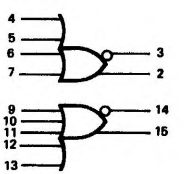
t_{pd} = 2.0 ns TYP.

10106
TRIPLE 4, 3, 3-INPUT NOR



t_{pd} = 2.0 ns TYP.

10109
DUAL 4, 5-INPUT OR/NOR



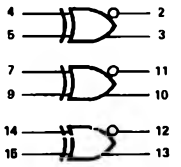
t_{pd} = 2.0 ns TYP.

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

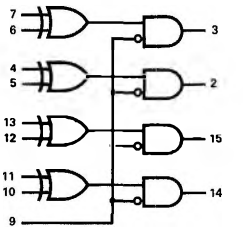
LOGIC DIAGRAMS: COMPLEX GATES

10107
TRIPLE EXCLUSIVE OR/NOR



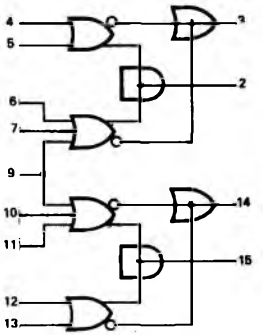
t_{pd} = 2.0, 2.8 ns TYP.

10113
QUAD EXCLUSIVE OR (WITH ENABLE)



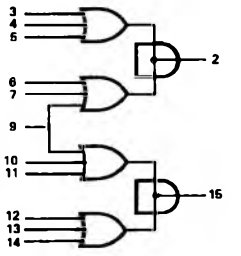
t_{pd} = 2.5 ns TYP.

10117
DUAL 2-WIDE 2, 3-INPUT OA/OAI GATE



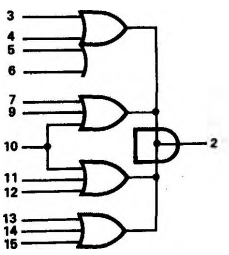
t_{pd} = 2.3 ns TYP.

10118
DUAL 2-WIDE 3-INPUT OR-AND



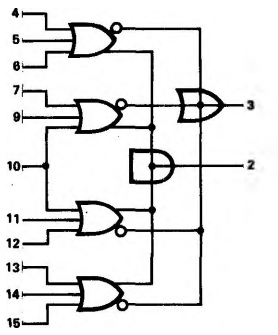
t_{pd} = 2.3 ns TYP.

10119
4-WIDE 4, 3, 3, 3-INPUT OR-AND



t_{pd} = 2.3 ns TYP.

10121
4-WIDE 3, 3, 3, 3-INPUT OA/OAI



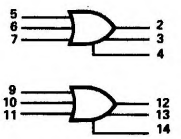
t_{pd} = 2.3 ns TYP.

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

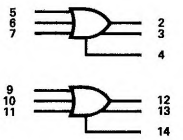
LOGIC DIAGRAMS: MULTIPLE OUTPUT GATES

10110
DUAL 3-INPUT 3-OUTPUT OR



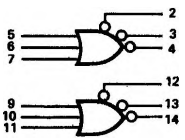
t_{pd} = 2.4 ns TYP. (ALL OUTPUTS LOADED)

10210
DUAL 3-INPUT 3-OUTPUT OR



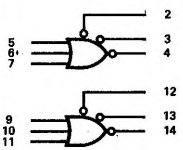
t_{pd} = 1.7 ns TYP. (ALL OUTPUTS LOADED)

10111
DUAL 3-INPUT 3-OUTPUT NOR



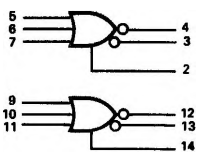
t_{pd} = 2.4 ns TYP. (ALL OUTPUTS LOADED)

10211
DUAL 3-INPUT 3-OUTPUT NOR



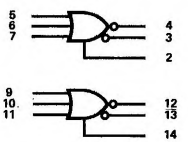
t_{pd} = 1.7 ns TYP. (ALL OUTPUTS LOADED)

10112
DUAL 3-INPUT 2-NOR/1-OR



t_{pd} = 2.4 ns TYP. (ALL OUTPUTS LOADED)

10212
DUAL 3-INPUT 2-NOR/1-OR



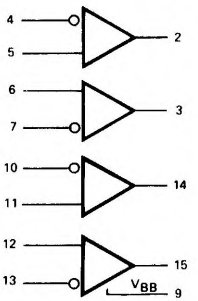
t_{pd} = 1.7 ns TYP. (ALL OUTPUTS LOADED)

NOTES: V_{CC1} = 1, 15, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

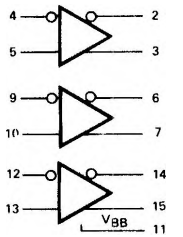
LOGIC DIAGRAMS: INTERFACE CIRCUITS

10115
QUAD DIFFERENTIAL LINE RECEIVER



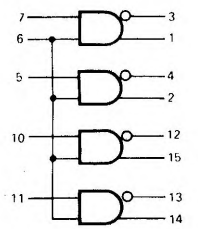
t_{pd} = 2.0 ns TYP.
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10116
TRIPLE DIFFERENTIAL LINE RECEIVER (OR/NOR)



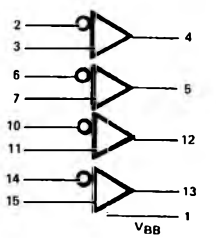
t_{pd} = 2.0 ns TYP.
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10124
QUAD TTL TO-ECL TRANSLATOR



t_{pd} = 5.0 ns TYP.
V_{CC} = 9 GND = 16 V_{EE} = 8

10125
QUAD ECL TO TTL TRANSLATOR (TOTEM-POLE OUTPUTS)

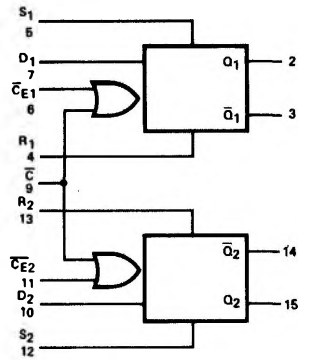


t_{pd} = 5.0 ns TYP.
V_{CC} = 9 GND = 16 V_{EE} = 8

NOTE: POSITIVE LOGIC: HIGH LEVEL = '1'

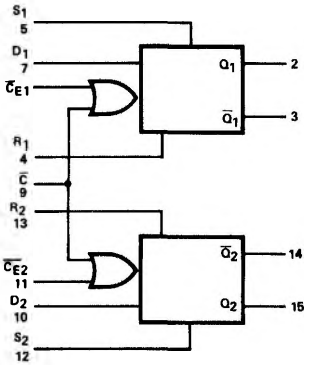
LOGIC DIAGRAMS: DUAL LATCHES AND FLIP-FLOPS

10130
DUAL D-TYPE LATCH



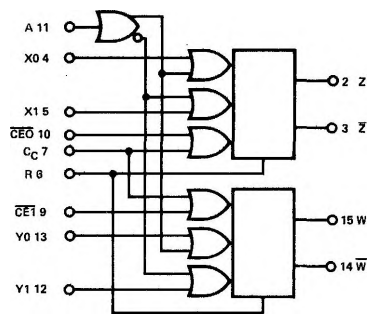
t_{pd} (DATA) = 2.5 ns TYP.
t_{pd} (CLOCK) = 3.0 ns TYP.

10131
DUAL TYPE D MASTER-SLAVE FLIP FLOP



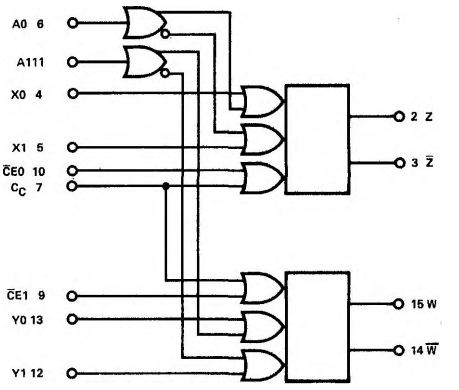
f = 170 MHz TYP.

10132
DUAL MULTIPLEXER-LATCH (WITH RESET)



t_{pd} (DATA) = 2.5 ns TYP.
t_{pd} (CLOCK) = 4.0 ns TYP.

10134
DUAL MULTIPLEXER-LATCH



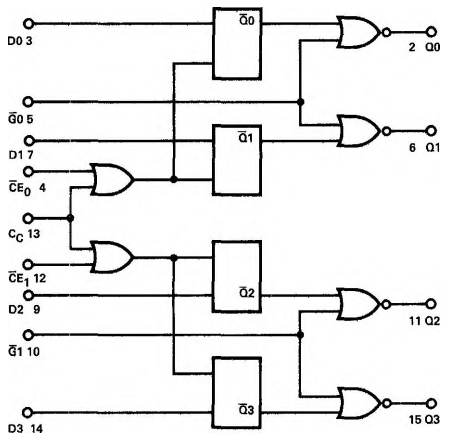
t_{pd} (DATA) = 2.5 ns TYP.
t_{pd} (CLOCK) = 4.0 ns TYP.

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

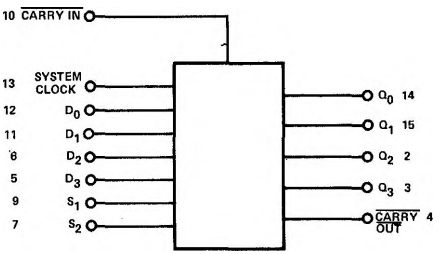
LOGIC DIAGRAMS: MSI: QUAD LATCH, COUNTERS, SHIFT REGISTER

10133
QUAD LATCH
(WITH OUTPUT GATING)

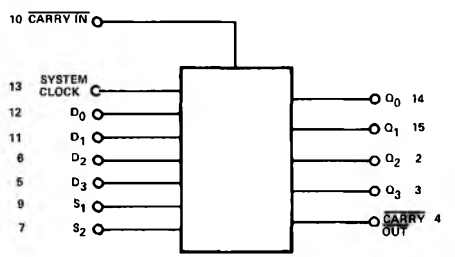


t_{pd} = 4.0 ns TYP.

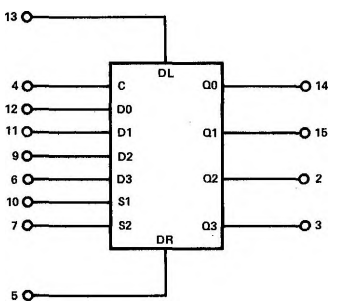
10136
UNIVERSAL HEXADECIMAL COUNTER



10137
UNIVERSAL DECADE COUNTER



10141
FOUR-BIT SHIFT REGISTER



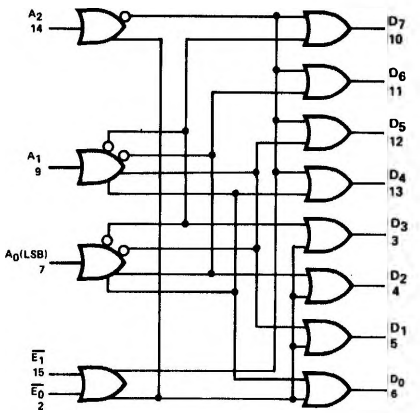
f_{TOG} = 200 MHz TYP.

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

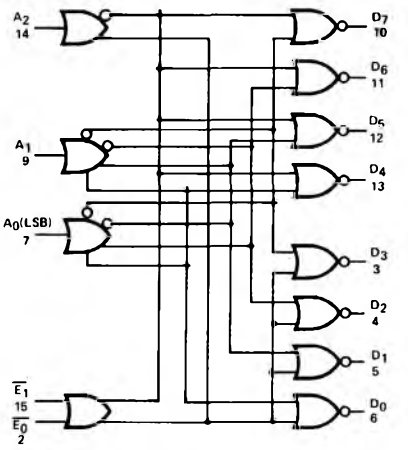
LOGIC DIAGRAMS: MSI DECODERS

10161
1 OF 8 DEMULTIPLEXER/DECODER
(SELECTED OUTPUT IS LOW)



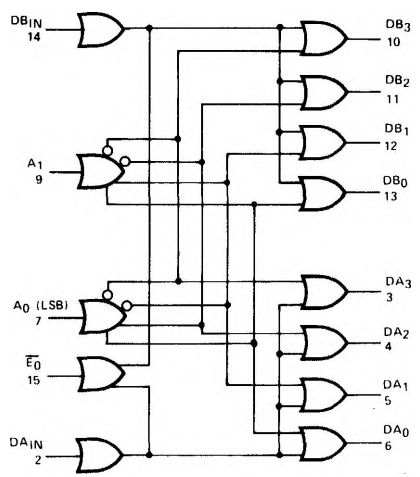
t_{pd} = 4.0 ns TYP.
(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

10162
1 OF 8 DEMULTIPLEXER/DECODER
(SELECTED OUTPUT IS HIGH)



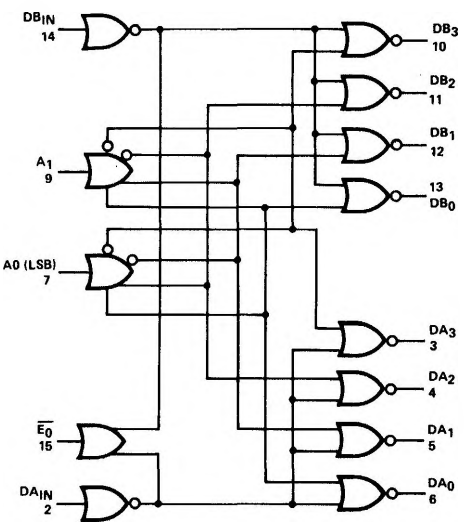
t_{pd} = 4.0 ns TYP.
(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

10171
DUAL 1 OF 4 DEMULTIPLEXER/DECODER
(SELECTED OUTPUTS LOW)



t_{pd} = 4.0 ns TYP.
(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

10172
DUAL 1 OF 4 DEMULTIPLEXER/DECODER
(SELECTED OUTPUTS HIGH)



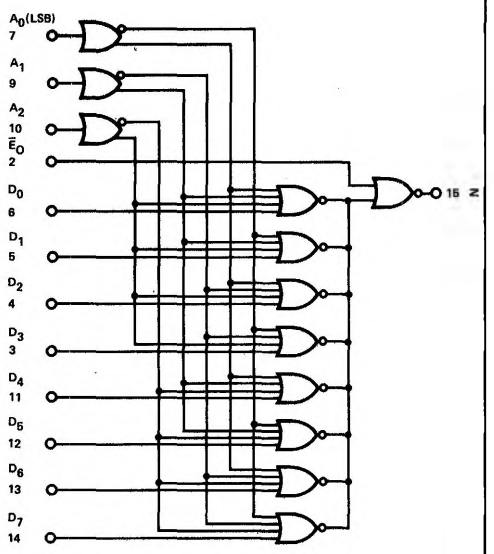
t_{pd} = 4.0 ns TYP.
(INTERNAL CONNECTIONS ARE EMITTER-DOT OR)

NOTES: V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

POSITIVE LOGIC: HIGH LEVEL = '1'

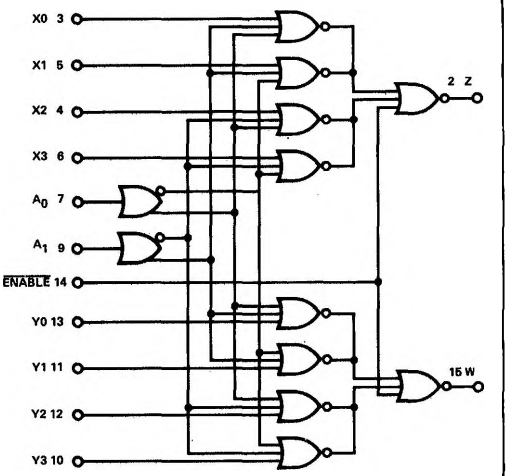
LOGIC DIAGRAMS: MSI: MULTIPLEXERS, QUAD MULTIPLEXER-LATCH

10164
8 TO 1 MULTIPLEXER



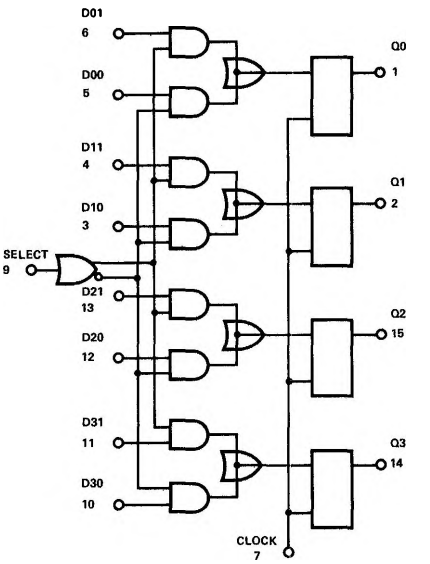
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10174
DUAL 4 TO 1 MULTIPLEXER



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10173
QUAD MULTIPLEXER-LATCH



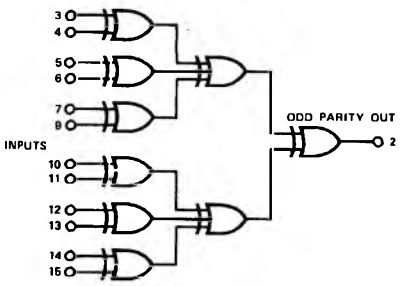
V_{CC1} = V_{CC2} = 16, V_{EE} = 8

NOTE: POSITIVE LOGIC: HIGH LEVEL = '1'

LOGIC DIAGRAMS: MSI: PARITY AND ALU FUNCTIONS

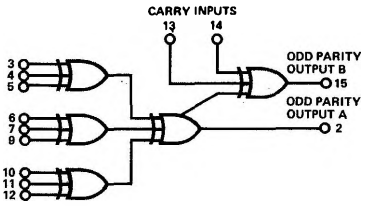
TO BE ANNOUNCED

10160
12-BIT PARITY CIRCUIT



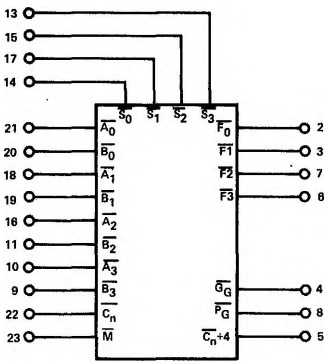
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10170
9 + 2 PARITY CIRCUIT



t_{pd} (OUTPUT A) = 4.0 ns TYP.
t_{pd} (OUTPUT B) = 6.0 ns TYP.
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

10181
4-BIT ARITHMETIC UNIT (16 ARITHMETIC FUNCTIONS AND 16 LOGICAL OPERATIONS)



t_{pd} = 7.0nS ($\overline{A1}$ TO $\overline{F}$)
t_{pd} = 5.0 ns ($\overline{A1}$ TO $\overline{Cn}$ + 4)
V_{CC1} = 1, V_{CC2} = 24, V_{EE} = 12

NOTE: POSITIVE LOGIC: HIGH LEVEL = '1'