

LMH6533 Four-Channel Laser Diode Driver with Dual Output, LVDS Interface and HFM Oscillator

Check for Samples: LMH6533

FEATURES

- Fast switching: Rise and fall times <0.8 ns
- Low voltage differential signaling (LVDS) channels enable interface for the fast switching lines
- Low output current noise: <0.5nA/√Hz
- Dual output: Selectable by SELB pin (active HIGH)
- Four independent current channels
- Gain of 300, 300 mA write channel
- Gain of 150, 150 mA low-noise read channel
- Two gain of 150, 150 mA write channels
- 500 mA minimum combined output current
- Integrated AC Coupled HFM Oscillator
- Selectable frequency and amplitude setting by

external resistors

- 200 MHz to 600 MHz frequency range
- Amplitude to 100 mA peak-to-peak modulation
- Complete shutdown by ENABLE pin
- 5V single-supply operation
- Logic inputs TTL and CMOS compatible
- Space saving Leadless Leadframe Package LLP[®]-28

APPLICATIONS

- Combination DVD/CD recordable and rewritable drives
- DVD camcorders
- DVD video recorders

DESCRIPTION

The LMH[™] 6533 is a laser diode driver for use in combination DVD/CD recordable and rewritable systems. The part contains two high-current outputs for reading and writing the DVD (650 nm) and CD (780 nm) lasers. Functionality includes read, write and erase through four separate switched current channels. The channel currents are summed together at the selected output to generate multilevel waveforms for reading, writing and erasing of optical discs. The LVDS interface delivers DVD write speeds of 12x and higher while minimizing noise and crosstalk. The LMH6533 is optimized for both speed and power consumption to meet the demands of next generation systems. The part features a 150 mA read channel plus one 300 mA and two 150 mA write channels, which can be summed to allow a total output current of 500 mA or greater. The channel currents are set through four independent current inputs.

The part is manufactured in National Semiconductor's VIP10[™] process, which features bonded wafer technology and trench isolation for very high switching speeds at low power levels. An on-board High-Frequency Modulator (HFM) oscillator helps reduce low-frequency noise of the laser and is enabled with the ENOSC pin. The fully differential oscillator circuit minimizes supply line noise, easing FCC approval of the overall system. The SELB pin (active HIGH) selects the output channel and oscillator settings. External resistors determine oscillator frequency and amplitude for each setting. The write and erase channels can be switched on and off through dedicated LVDS interface pins.

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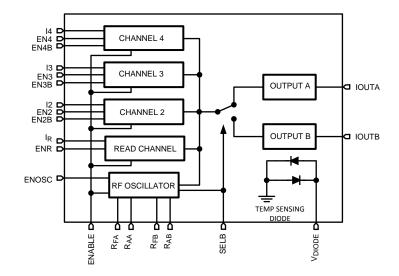
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LMH6533

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EXAS

Block Diagram





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance	
Human Body Model	2KV ⁽²⁾
Machine Model	200V ⁽³⁾
Supply Voltage ($V^+ - V^-$)	5.5V
Differential Input Voltage	±5.5V
Output Short Circuit to Ground ⁽⁴⁾	Continuous
Input Common Mode Voltage	V ⁻ to V ⁺
Storage Temperature Range	−65°C to +150°C
Junction Temperature ⁽⁵⁾	+150°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

(2) For testing purposes, ESD was applied using 'Human body model'; 1.5 k Ω in series with 100 pF

(3) Machine Model, 0Ω in series with 200 pF.

(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C

(5) The maximum power dissipation is a function of $T_{J(MAX}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)} - T_A$) / θ_{JA} . All numbers apply for packages soldered directly onto a PC board.

Operating Ratings ⁽¹⁾

Supply Voltage (V ⁺ - V ⁻)	$4.5 V \le V_S \ge 5.5 V$
Operating Temp. Range (T _A) ⁽²⁾	$-40^{\circ}C \le T_{A} \le 85^{\circ}C$
Thermal Resistance ⁽³⁾ , ⁽²⁾	LLP Package
θ _{JC}	3°C/W
θ_{JA} (no heatsink)	42°C/W

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

(2) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. There is no guarantee of parametric performance as indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information on temperature de-rating of this device.

(3) The maximum power dissipation is a function of $T_{J(MAX}, \theta_{JA}$, and T_A . The maximum allowable power dissipation at any ambient temperature is PD = $(T_{J(MAX)}, T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.



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Operating Ratings⁽¹⁾ (continued)

θ_{JA} (with heatsink) see $^{(4)}$	30.8°C/W
I _{INR} /3/4	1.5 mA (max)
I _{IN2}	1.0 mA (max)
R _{FREQ}	1000Ω (min)
R _{AMP}	300Ω
Fosc	100-600 MHz
A _{OSC}	10-100 mA _{PP}

(4) V_{GPD} = ground potential difference voltage between driver and receiver



+5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^{\circ}$ C, $R_L = 10\Omega$. Boldface limits apply at the temperature extremes. (1)

Symbol	Parameter	Conditions	Min (2)	Тур (3)	Max (2)	Units
LVDS					I	I
VI	Input Voltage Range	V _{GPD} < 50 mV (2), (4), (5)	825	1550	1575	mV
V _{IDTH}	Input Diff. Threshold	V _{GPD} < 50 mV (2), (4), (5)	-100	0	100	mV
V _{HYST}	Input Diff. Hysteresis	VIDTHH - VIDTH1 (2), (4), (5)	25	0		mV
R _{IN}	Input Diff. Impedance	(2), (4),(5)	80	104	120	Ω
I _{IN}	Input Current	Excluding R _{IN} Current V _{CM} = 1.25V		5	50	μA
Current Ch	annels					
R _{IN}	Input Resistance all Channels	R _{IN} to Ground	425	556	675	Ω
l _{OS}	Current Offset	All Channels Off ⁽⁶⁾	-7.5	4.75	7.5	mA
A _{IW}	Current Gain	Channel 2 ⁽⁷⁾	270	303	330	A/A
A _{IR}	Current Gain	Channels 3,4 and Read ⁽⁷⁾	135	152	165	A/A
I _{LIN-R,3,4}	Output Current Linearity	500 $\mu A < L_{IN} <$ 1000 $\mu A;$ R_{LOAD} = 10 Ω Channels Read, 3 and 4	-3.5	2.5	+3.5	%
I _{LIN-2}	Output Current Linearity	500 $\mu A < L_{IN} <$ 1000 $\mu A;~R_{LOAD}$ = 10 Ω Channels 2	-8	5	+8	%
IOUT _W	Output Current	Channel 2 ⁽⁶⁾ @ 1mA Input Current	250	263		mA
IOUT _{R,3,4}	Output Current	Channel 3, 4 and Read ⁽⁶⁾ @ 1 mA Input Current	135	150		mA
IOUT _{TOTAL}	Total Output Current	All Channels ⁽⁸⁾ ; $R_{LOAD} = 5\Omega$	500			mA
V _{TLO}	TTL Low Voltage	ENR, ENOSC Input (H to L)		1.51	0.8	V
V _{ELO}	Enable Low Voltage	Enable Input (H to L)		2.41	0.8	V
V _{THI}	TTL High Voltage	ENR, ENOSC Inputs (L to H)	2.0	1.54		V
V _{EHI}	Enable High Voltage	Enable Input (L to H)	2.8	2.4		V
I _{SPD}	Supply Current, Power Down	Enable = Low ⁽⁶⁾		0.003	0.5	mA
I _{Sr1}	Supply Current, Read Mode, Oscillator Disabled	ENOSC = Low; ⁽⁶⁾ I2 = I3 = I4 = I _R = 125 μA		98.5	120	mA
I _{Sr2}	Supply Current, Read Mode, Oscillator Enabled	ENOSC = High; ⁽⁶⁾ I2 = I3 = I4 = I _R = 125 μA		98.5	120	mA
I _{Swr}	Supply Current, Write Mode	EN2 = EN3 = EN4 = High; ⁽⁶⁾ I2 = I3 = I4 = I _R = 125 μA		182.5	210	mA
I _S	Supply Current	All Channels Disable, No Input Current. SELB = 0; R _{AA} , R _{AB} , R _{FA} , R _{FB} = ∞		45		mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. There is no guarantee of parametric performance as indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information on temperature de-rating of this device. (2)

All limits are guaranteed by testing or statistical analysis. Typical values represent the most likely parametric norm. V_{GPD} = ground potential difference voltage between driver and receiver (3) (4)

(5) Reference IEEE Reduced Range Link (RRL) specifications.

Positive current corresponds to current flowing into the device. (6)

(7) Input currents are set to 0.3 mA

Total input current is 4.4 mA (all 4 channels equal) and output currents are summed together (see typical performance characteristics). (8)



+5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^{\circ}C$, $R_L = 10\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Тур (3)	Max (2)	Units
t _r	Write Rise Time	I_{OUT} = 40 mA (Read) + 40 mA (10% to 90%) R_{LOAD} = 5 Ω	0.50		ns	
t _f	Write Fall Time	I_{OUT} = 40 mA (Read) + 40 mA (90% to 10%) R_{LOAD} = 5 Ω		0.76		ns
t _r	Write Rise Time	I_{OUT} = 100 mA (Read) + 100 mA (10% to 90%) R _{LOAD} = 5Ω		0.65		ns
t _f	Write Fall Time	I_{OUT} = 100 mA (Read) + 100 mA (90% to 10%) R_{LOAD} = 5 Ω		0.75		ns
t _r	Write Rise Time	I_{OUT} = 150 mA (Read) + 150 mA (10% to 90%) R_{LOAD} = 5 Ω		0.78		ns
t _f	Write Fall Time	I_{OUT} = 150 mA (Read) + 150 mA (90% to 10%) R_{LOAD} = 5 Ω	0.77		ns	
OS	Output Current Overshoot	I _{OUT} = 40 mA (Read) + 40 mA	16		%	
IN ₀	Output Current Noise	$I_{OUT} = 40 \text{ mA}; R_{LOAD} = 50\Omega;$ f = 10 MHz; ENOSC = Low		0.47		nA/√Hz
t _{ON}	I _{OUT} ON Prop. Delay	Switched on EN2 and EN2B		0.45		ns
t _{OFF}	I _{OUT} OFF Prop. Delay	Switched on EN2 and EN2B		0.40		ns
t _{disr}	Disable Time, Read Channel	Switch on ENR		1.1		ns
t _{enr}	Enable Time, Read Channel	Switch on ENR		1.1		ns
t _{dis}	Disable Time, (Shutdown)			3		μs
t _{en}	Enable Time, (Shutdown)		3			μs
BW _C	Channel Bandwidth, -3 dB	I _{OUT} = 50 mA, All Channels		2.5		MHz
f _{OSC}	Oscillator Frequency	$R_F = 3 k\Omega$ Range 200 MHz to 600 MHz	270	330	390	MHz
T _{DO}	Disable Time Oscillator			5.2		ns
T _{EO}	Enable Time Oscillator			5.4		ns

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(2) All limits are guaranteed by testing or statistical analysis.

(3) Typical values represent the most likely parametric norm.

Connection Diagram

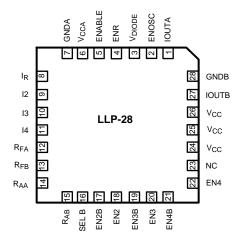


Figure 1. 28-Pin LLP (Top View)



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Table 1. Pin Descriptions

Pin #	Description	Remark
1	Laser driver output channel A	
2	Internal Oscillator Enable pin	Oscillator activated if pin is high
3	Temp Sensing Diode	See application note on using this pin
4	Read Channel Enable pin	Read Channel Enabled if pin is high
5	Chip Enable pin	Chip Enabled if pin is high
6	Supply Voltage A	
7	Ground Connection A	
8	Read Channel current setting	
9	Channel 2 current setting	
10	Channel 3 current setting	
11	Channel 4 current setting	
12	Oscillator Frequency setting Channel A	Set by external resistor to ground
13	Oscillator Frequency setting Channel B	Set by external resistor to ground
14	Oscillator Amplitude setting Channel A	Set by external resistor to ground
15	Oscillator Amplitude setting Channel B	Set by external resistor to ground
16	Channel select B	Channel B selected if pin is high
17	LVDS input Channel 2B	Channel 2 active if logical input is low
18	LVDS input Channel 2	Channel 2 active if logical input is high
19	LVDS input Channel 3B	Channel 3 active if logical input is low
20	LVDS input Channel 3	Channel 3 active if logical input is high
21	LVDS input Channel 4B	Channel 4 active if logical input is low
22	LVDS input Channel 4	Channel 4 active if logical input is high
23	NC	
24	Supply Voltage	
25	Supply Voltage	
26	Supply Voltage	
27	Laser driver output channel B	
28	Ground Connection B	

Truth Tables

Table 2. IOUT CONTROL

Enable	ENR	EN2	EN3	EN4	IOUT
0	Х	Х	Х	Х	OFF
1	0	0	0	0	OFF
1	1	0	0	0	A _R *I _{INR}
1	1	1	0	0	$A_{R}^{*I}_{INR} + A_{2}^{*I}_{IN2}$
1	1	0	1	0	A _R *I _{INR} +A ₃ *I _{IN3}
1	1	0	0	1	$A_{R}^{*I}_{INR} + A_{4}^{*I}_{IN4}$

Table 3. OSCILLATOR CONTROL

Enable	ENOSC	ENR	EN2	EN3	EN4	Oscillator
0	х	x	x	x	x	OFF
1	0	x	x	x	x	OFF
1	1	x	x	x	x	on



Waveforms

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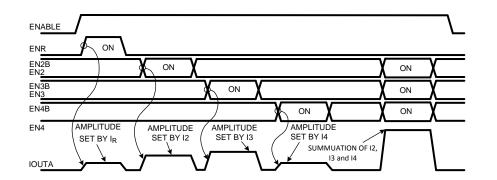


Figure 2. Functional Timing Diagram

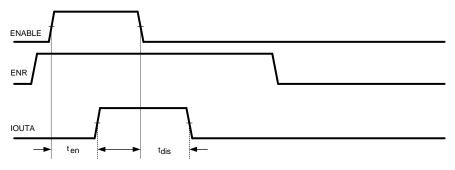


Figure 3. Enable Timing

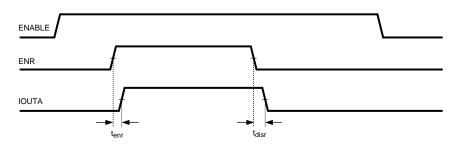


Figure 4. Read Timing

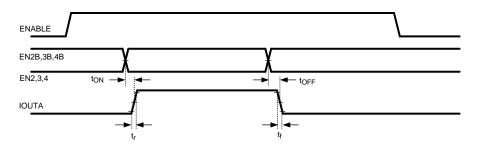
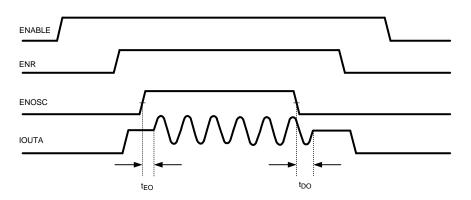


Figure 5. Write Timing









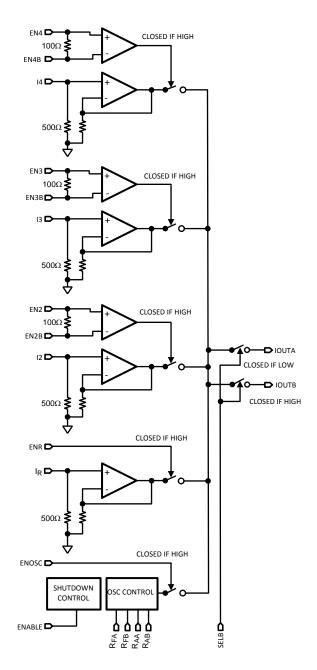


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Detailed Block Diagram

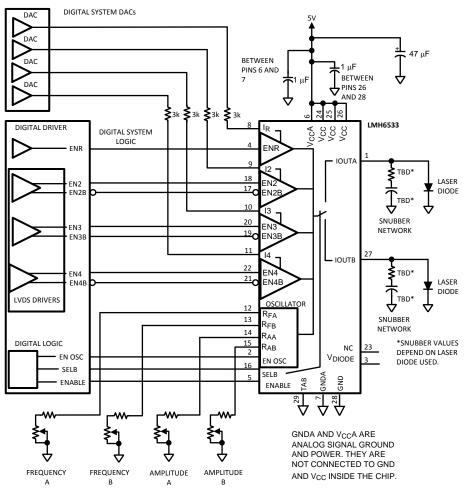




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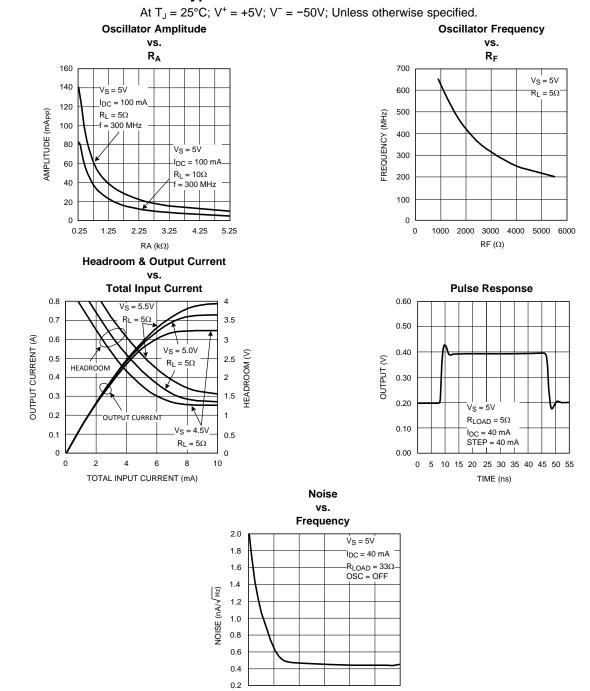
Application Schematic



LOWER RESISTANCE = HIGHER FREQUENCY AND AMPLITUDE

10 Submit Documentation Feedback





Typical Performance Characteristics

FREQUENCY (MHz)

26 30

1 6 11 16 21

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