## INTRODUCTION

The KS0040 is an LCD driver and controller LSI for liquid crystal dot matrix character display systems. It can display 1 to 4 lines of 8 characters in the 16 × 16 dots format. It is particularly suitable for displaying Asian characters such as Korean, Chinese and Japanese. 8 ×16 dot half-size alpha-numeric characters can be displayed as well. It can also be used for a 64 ×128 dot graphic LCD with an internal CGRAM.
A voltage converter (2 to 4 times), voltage regulator, and voltage follower and bias circuit are built-in to the IC.

## FEATURES

- **Driver outputs**
  - — Common outputs: 64 common + 1 common for icon
  - — Segment outputs: 128 segment + 4 segment for icon
- **Applicable Panel Size**

| Display Size | Duty | Contents of Outputs |
|---|---|---|
| 1 line × 8 char. | 1/17 | 1× 8 characters + 16 × 4 vertical icons + 128 horizontal icons |
| 2 line × 8 char. | 1/33 | 2 × 8 characters + 32 × 4 vertical icons + 128 horizontal icons |
| 3 line × 8 char. | 1/49 | 3 × 8 characters + 48 × 4 vertical icons + 128 horizontal icons |
| 4 line × 8 char. | 1/65 | 3 × 8 characters + 48 × 4 vertical icons + 128 horizontal icons |

- **Internal memory**
  - — Full-size character generator ROM (FCGROM): 2,097,152 bits (8,192 characters × 16 × 16 dot)
  - — Half-size character generator ROM (HCGROM): 16,384 bits (128 characters × 8 × 16 dot)
  - — Character generator RAM (CGRAM): 8,192 bits (32 characters × 16 × 16 dot)
  - — Display data RAM (DDRAM): 1,024 bits (64 characters × 2 byte)
  - — Icon RAM (ICONRAM): 384 bits (128 horizontal icons + 64 × 4 vertical icons)
- **MPU interface**
  - — 8-bit/4-bit parallel interface mode: 68-series, 80-series selectable
  - — Serial interface mode: 4-pin clock synchronous serial interface
- **Function set**
  - — Various instruction sets: Vertical / horizontal dot-by-dot display shift, B / W inversion, power control ... etc.
  - — COM / SEG bidirectional
  - — H/W Reset
- **Built-in analog circuit**
  - — Programmable oscillator circuit
  - — Electrical volume for contrast control (64 stages)
  - — Voltage converter (2 to 4 times) / voltage regulator / voltage follower & bias circuit

- **Low power operation**
  - — Sleep mode (5μA)
  - — Normal mode (TBD)
- **Operating voltage range**
  - — Supply voltage (VDD): 2.4V to 5.5V
  - — LCD driving voltage (VLCD = V0 – VSS): 13.0V
- **Package type**
  - — Bumped chip / TCP

## BLOCK DIAGRAM

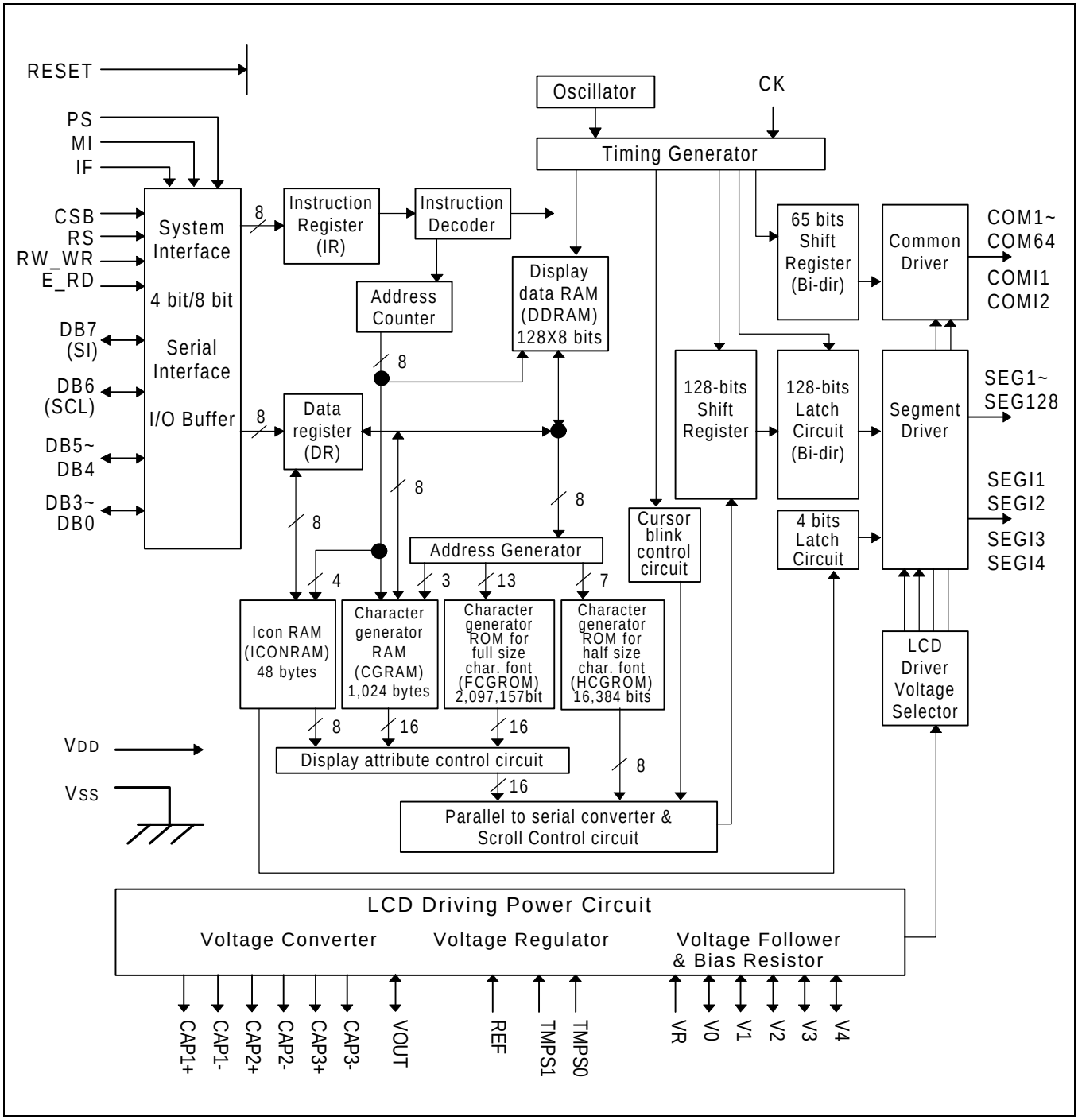



**Figure 1. Block Diagram**

## PAD CONFIGURATION

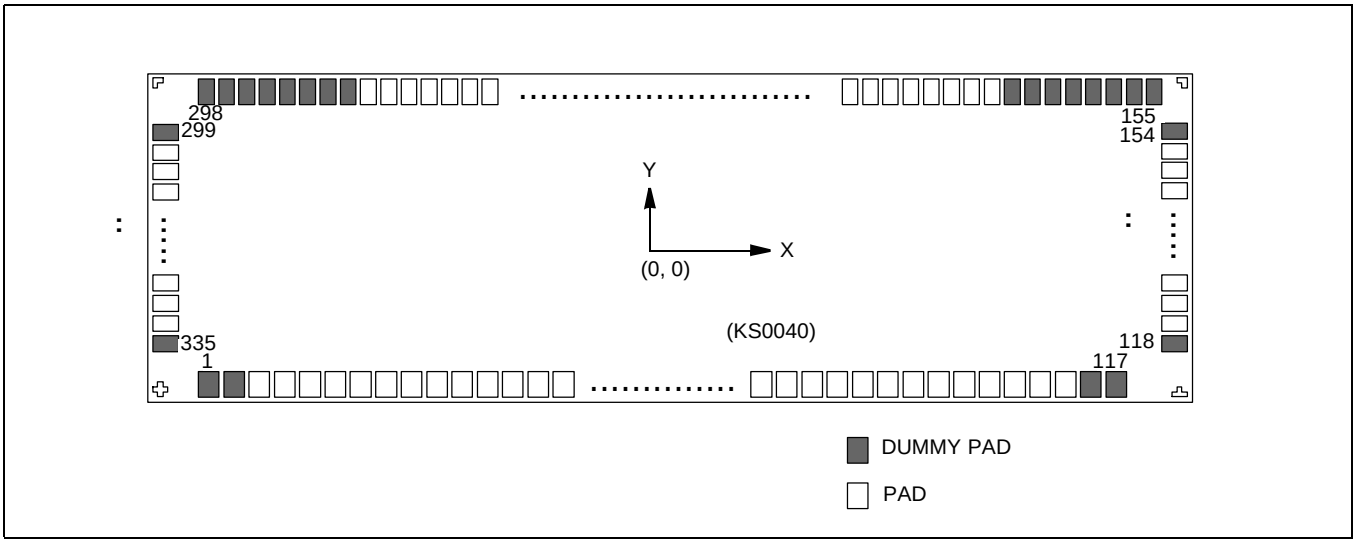



**Figure 2. Pad Configuration**

| Item | Pad No. | Size | | Unit |
|---|---|---|---|---|
| | | X | Y | |
| Chip size | – | 12160 | 3860 | μm |
| Pad pitch | 1 to 117 | 90 | | |
| | 118 to 335 | 70 | | |
| Bumped pad size | 1 to 117 | 56 | 114 | |
| | 118 to 154 | 108 | 50 | |
| | 155 to 298 | 50 | 108 | |
| | 229 to 335 | 108 | 50 | |
| Bumped pad height | All pads | 17 (Typ) | | |

## PAD LOCATION

**Table 1. Pad Location**

[unit: μm]

| Pad No | Pad Name | Coordinate | | Pad No | Pad Name | Coordinate | | Pad No | Pad Name | Coordinate | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | X | Y | | | X | Y | | | X | Y |
| 1 | DUMMY | -5220 | -1806 | 46 | $V_{DD}$ | -1170 | -1806 | 91 | V0 | 2880 | -1806 |
| 2 | DUMMY | -5130 | -1806 | 47 | $V_{DD}$ | -1080 | -1806 | 92 | V0 | 2970 | -1806 |
| 3 | $V_{SS}$ | -5040 | -1806 | 48 | $V_{DD}$ | -990 | -1806 | 93 | V0 | 3060 | -1806 |
| 4 | TEST1 | -4950 | -1806 | 49 | $V_{DD}$ | -900 | -1806 | 94 | V0 | 3150 | -1806 |
| 5 | $V_{DD}$ | -4860 | -1806 | 50 | $V_{DD}$ | -810 | -1806 | 95 | DUMMY | 3240 | -1806 |
| 6 | DUMMY | -4770 | -1806 | 51 | $V_{DD}$ | -720 | -1806 | 96 | V1 | 3330 | -1806 |
| 7 | $V_{SS}$ | -4680 | -1806 | 52 | $V_{DD}$ | -630 | -1806 | 97 | V1 | 3420 | -1806 |
| 8 | REF | -4590 | -1806 | 53 | $V_{DD}$ | -540 | -1806 | 98 | V2 | 3510 | -1806 |
| 9 | $V_{DD}$ | -4500 | -1806 | 54 | DUMMY | -450 | -1806 | 99 | V2 | 3600 | -1806 |
| 10 | MI | -4410 | -1806 | 55 | VOUT | -360 | -1806 | 100 | V3 | 3690 | -1806 |
| 11 | $V_{SS}$ | -4320 | -1806 | 56 | VOUT | -270 | -1806 | 101 | V3 | 3780 | -1806 |
| 12 | IF | -4230 | -1806 | 57 | VOUT | -180 | -1806 | 102 | V4 | 3870 | -1806 |
| 13 | $V_{DD}$ | -4140 | -1806 | 58 | VOUT | -90 | -1806 | 103 | V4 | 3960 | -1806 |
| 14 | PS | -4050 | -1806 | 59 | DUMMY | 0 | -1806 | 104 | DUMMY | 4050 | -1806 |
| 15 | $V_{SS}$ | -3960 | -1806 | 60 | CAP3+ | 90 | -1806 | 105 | $V_{SS}$ | 4140 | -1806 |
| 16 | CSB | -3870 | -1806 | 61 | CAP3+ | 180 | -1806 | 106 | TEST3 | 4230 | -1806 |
| 17 | $V_{DD}$ | -3780 | -1806 | 62 | CAP3+ | 270 | -1806 | 107 | $V_{DD}$ | 4320 | -1806 |
| 18 | RESET | -3690 | -1806 | 63 | CAP3+ | 360 | -1806 | 108 | TMPS1 | 4410 | -1806 |
| 19 | RS | -3600 | -1806 | 64 | CAP3- | 450 | -1806 | 109 | $V_{SS}$ | 4500 | -1806 |
| 20 | RW_WR | -3510 | -1806 | 65 | CAP3- | 540 | -1806 | 110 | TMPS0 | 4590 | -1806 |
| 21 | E_RD | -3420 | -1806 | 66 | CAP3- | 630 | -1806 | 111 | $V_{DD}$ | 4680 | -1806 |
| 22 | DB7 | -3330 | -1806 | 67 | CAP3- | 720 | -1806 | 112 | TEST2 | 4770 | -1806 |
| 23 | DB6 | -3240 | -1806 | 68 | CAP1+ | 810 | -1806 | 113 | $V_{SS}$ | 4860 | -1806 |
| 24 | DB5 | -3150 | -1806 | 69 | CAP1+ | 900 | -1806 | 114 | CK | 4950 | -1806 |
| 25 | DB4 | -3060 | -1806 | 70 | CAP1+ | 990 | -1806 | 115 | $V_{DD}$ | 5040 | -1806 |
| 26 | DB3 | -2970 | -1806 | 71 | CAP1+ | 1080 | -1806 | 116 | DUMMY | 5130 | -1806 |
| 27 | DB2 | -2880 | -1806 | 72 | CAP1- | 1170 | -1806 | 117 | DUMMY | 5220 | -1806 |
| 28 | DB1 | -2790 | -1806 | 73 | CAP1- | 1260 | -1806 | 118 | DUMMY | 5920 | -1326 |
| 29 | DB0 | -2700 | -1806 | 74 | CAP1- | 1350 | -1806 | 119 | COMI1 | 5920 | -1256 |
| 30 | DUMMY | -2610 | -1806 | 75 | CAP1- | 1440 | -1806 | 120 | COM1 | 5920 | -1186 |
| 31 | DUMMY | -2520 | -1806 | 76 | CAP2+ | 1530 | -1806 | 121 | COM2 | 5920 | -1116 |
| 32 | DUMMY | -2430 | -1806 | 77 | CAP2+ | 1620 | -1806 | 122 | COM3 | 5920 | -1046 |
| 33 | $V_{SS}$ | -2340 | -1806 | 78 | CAP2+ | 1710 | -1806 | 123 | COM4 | 5920 | -976 |
| 34 | $V_{SS}$ | -2250 | -1806 | 79 | CAP2+ | 1800 | -1806 | 124 | COM5 | 5920 | -906 |
| 35 | $V_{SS}$ | -2160 | -1806 | 80 | CAP2- | 1890 | -1806 | 125 | COM6 | 5920 | -836 |
| 36 | $V_{SS}$ | -2070 | -1806 | 81 | CAP2- | 1980 | -1806 | 126 | COM7 | 5920 | -766 |
| 37 | $V_{SS}$ | -1980 | -1806 | 82 | CAP2- | 2070 | -1806 | 127 | COM8 | 5920 | -696 |
| 38 | $V_{SS}$ | -1890 | -1806 | 83 | CAP2- | 2160 | -1806 | 128 | COM17 | 5920 | -626 |
| 39 | $V_{SS}$ | -1800 | -1806 | 84 | DUMMY | 2250 | -1806 | 129 | COM18 | 5920 | -556 |
| 40 | $V_{SS}$ | -1710 | -1806 | 85 | DUMMY | 2340 | -1806 | 130 | COM19 | 5920 | -486 |
| 41 | $V_{SS}$ | -1620 | -1806 | 86 | VR | 2430 | -1806 | 131 | COM20 | 5920 | -416 |
| 42 | $V_{SS}$ | -1530 | -1806 | 87 | VR | 2520 | -1806 | 132 | COM21 | 5920 | -346 |
| 43 | DUMMY | -1440 | -1806 | 88 | VR | 2610 | -1806 | 133 | COM22 | 5920 | -276 |
| 44 | $V_{DD}$ | -1350 | -1806 | 89 | VR | 2700 | -1806 | 134 | COM23 | 5920 | -206 |
| 45 | $V_{DD}$ | -1260 | -1806 | 90 | DUMMY | 2790 | -1806 | 135 | COM24 | 5920 | -136 |

**Table 1. Pad Location (Continued)**

[unit: μm]

| Pad No | Pad Name | Coordinate | | Pad No | Pad Name | Coordinate | | Pad No | Pad Name | Coordinate | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | X | Y | | | X | Y | | | X | Y |
| 136 | COM33 | 5920 | -66 | 186 | SEG24 | 2835 | 1770 | 236 | SEG74 | -665 | 1770 |
| 137 | COM34 | 5920 | 4 | 187 | SEG25 | 2765 | 1770 | 237 | SEG75 | -735 | 1770 |
| 138 | COM35 | 5920 | 74 | 188 | SEG26 | 2695 | 1770 | 238 | SEG76 | -805 | 1770 |
| 139 | COM36 | 5920 | 144 | 189 | SEG27 | 2625 | 1770 | 239 | SEG77 | -875 | 1770 |
| 140 | COM37 | 5920 | 214 | 190 | SEG28 | 2555 | 1770 | 240 | SEG78 | -945 | 1770 |
| 141 | COM38 | 5920 | 284 | 191 | SEG29 | 2485 | 1770 | 241 | SEG79 | -1015 | 1770 |
| 142 | COM39 | 5920 | 354 | 192 | SEG30 | 2415 | 1770 | 242 | SEG80 | -1085 | 1770 |
| 143 | COM40 | 5920 | 424 | 193 | SEG31 | 2345 | 1770 | 243 | SEG81 | -1155 | 1770 |
| 144 | COM49 | 5920 | 494 | 194 | SEG32 | 2275 | 1770 | 244 | SEG82 | -1225 | 1770 |
| 145 | COM50 | 5920 | 564 | 195 | SEG33 | 2205 | 1770 | 245 | SEG83 | -1295 | 1770 |
| 146 | COM51 | 5920 | 634 | 196 | SEG34 | 2135 | 1770 | 246 | SEG84 | -1365 | 1770 |
| 147 | COM52 | 5920 | 704 | 197 | SEG35 | 2065 | 1770 | 247 | SEG85 | -1435 | 1770 |
| 148 | COM53 | 5920 | 774 | 198 | SEG36 | 1995 | 1770 | 248 | SEG86 | -1505 | 1770 |
| 149 | COM54 | 5920 | 844 | 199 | SEG37 | 1925 | 1770 | 249 | SEG87 | -1575 | 1770 |
| 150 | COM55 | 5920 | 914 | 200 | SEG38 | 1855 | 1770 | 250 | SEG88 | -1645 | 1770 |
| 151 | COM56 | 5920 | 984 | 201 | SEG39 | 1785 | 1770 | 251 | SEG89 | -1715 | 1770 |
| 152 | SEGI1 | 5920 | 1054 | 202 | SEG40 | 1715 | 1770 | 252 | SEG90 | -1785 | 1770 |
| 153 | SEGI2 | 5920 | 1124 | 203 | SEG41 | 1645 | 1770 | 253 | SEG91 | -1855 | 1770 |
| 154 | DUMMY | 5920 | 1194 | 204 | SEG42 | 1575 | 1770 | 254 | SEG92 | -1925 | 1770 |
| 155 | DUMMY | 5005 | 1770 | 205 | SEG43 | 1505 | 1770 | 255 | SEG93 | -1995 | 1770 |
| 156 | DUMMY | 4935 | 1770 | 206 | SEG44 | 1435 | 1770 | 256 | SEG94 | -2065 | 1770 |
| 157 | DUMMY | 4865 | 1770 | 207 | SEG45 | 1365 | 1770 | 257 | SEG95 | -2135 | 1770 |
| 158 | DUMMY | 4795 | 1770 | 208 | SEG46 | 1295 | 1770 | 258 | SEG96 | -2205 | 1770 |
| 159 | DUMMY | 4725 | 1770 | 209 | SEG47 | 1225 | 1770 | 259 | SEG97 | -2275 | 1770 |
| 160 | DUMMY | 4655 | 1770 | 210 | SEG48 | 1155 | 1770 | 260 | SEG98 | -2345 | 1770 |
| 161 | DUMMY | 4585 | 1770 | 211 | SEG49 | 1085 | 1770 | 261 | SEG99 | -2415 | 1770 |
| 162 | DUMMY | 4515 | 1770 | 212 | SEG50 | 1015 | 1770 | 262 | SEG100 | -2485 | 1770 |
| 163 | SEG1 | 4445 | 1770 | 213 | SEG51 | 945 | 1770 | 263 | SEG101 | -2555 | 1770 |
| 164 | SEG2 | 4375 | 1770 | 214 | SEG52 | 875 | 1770 | 264 | SEG102 | -2625 | 1770 |
| 165 | SEG3 | 4305 | 1770 | 215 | SEG53 | 805 | 1770 | 265 | SEG103 | -2695 | 1770 |
| 166 | SEG4 | 4235 | 1770 | 216 | SEG54 | 735 | 1770 | 266 | SEG104 | -2765 | 1770 |
| 167 | SEG5 | 4165 | 1770 | 217 | SEG55 | 665 | 1770 | 267 | SEG105 | -2835 | 1770 |
| 168 | SEG6 | 4095 | 1770 | 218 | SEG56 | 595 | 1770 | 268 | SEG106 | -2905 | 1770 |
| 169 | SEG7 | 4025 | 1770 | 219 | SEG57 | 525 | 1770 | 269 | SEG107 | -2975 | 1770 |
| 170 | SEG8 | 3955 | 1770 | 220 | SEG58 | 455 | 1770 | 270 | SEG108 | -3045 | 1770 |
| 171 | SEG9 | 3885 | 1770 | 221 | SEG59 | 385 | 1770 | 271 | SEG109 | -3115 | 1770 |
| 172 | SEG10 | 3815 | 1770 | 222 | SEG60 | 315 | 1770 | 272 | SEG110 | -3185 | 1770 |
| 173 | SEG11 | 3745 | 1770 | 223 | SEG61 | 245 | 1770 | 273 | SEG111 | -3255 | 1770 |
| 174 | SEG12 | 3675 | 1770 | 224 | SEG62 | 175 | 1770 | 274 | SEG112 | -3325 | 1770 |
| 175 | SEG13 | 3605 | 1770 | 225 | SEG63 | 105 | 1770 | 275 | SEG113 | -3395 | 1770 |
| 176 | SEG14 | 3535 | 1770 | 226 | SEG64 | 35 | 1770 | 276 | SEG114 | -3465 | 1770 |
| 177 | SEG15 | 3465 | 1770 | 227 | SEG65 | -35 | 1770 | 277 | SEG115 | -3535 | 1770 |
| 178 | SEG16 | 3395 | 1770 | 228 | SEG66 | -105 | 1770 | 278 | SEG116 | -3605 | 1770 |
| 179 | SEG17 | 3325 | 1770 | 229 | SEG67 | -175 | 1770 | 279 | SEG117 | -3675 | 1770 |
| 180 | SEG18 | 3255 | 1770 | 230 | SEG68 | -245 | 1770 | 280 | SEG118 | -3745 | 1770 |
| 181 | SEG19 | 3185 | 1770 | 231 | SEG69 | -315 | 1770 | 281 | SEG119 | -3815 | 1770 |
| 182 | SEG20 | 3115 | 1770 | 232 | SEG70 | -385 | 1770 | 282 | SEG120 | -3885 | 1770 |
| 183 | SEG21 | 3045 | 1770 | 233 | SEG71 | -455 | 1770 | 283 | SEG121 | -3955 | 1770 |
| 184 | SEG22 | 2975 | 1770 | 234 | SEG72 | -525 | 1770 | 284 | SEG122 | -4025 | 1770 |
| 185 | SEG23 | 2905 | 1770 | 235 | SEG73 | -595 | 1770 | 285 | SEG123 | -4095 | 1770 |

**Table 1. Pad Location (Continued)**

[unit: μm]

| Pad No | Pad Name | Coordinate | | Pad No | Pad Name | Coordinate | | Pad No | Pad Name | Coordinate | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | X | Y | | | X | Y | | | X | Y |
| 286 | SEG124 | -4165 | 1770 | 303 | COM64 | -5920 | 914 | 320 | COM31 | -5920 | -276 |
| 287 | SEG125 | -4235 | 1770 | 304 | COM63 | -5920 | 844 | 321 | COM30 | -5920 | -346 |
| 288 | SEG126 | -4305 | 1770 | 305 | COM62 | -5920 | 774 | 322 | COM29 | -5920 | -416 |
| 289 | SEG127 | -4375 | 1770 | 306 | COM61 | -5920 | 704 | 323 | COM28 | -5920 | -486 |
| 290 | SEG128 | -4445 | 1770 | 307 | COM60 | -5920 | 634 | 324 | COM27 | -5920 | -556 |
| 291 | DUMMY | -4515 | 1770 | 308 | COM59 | -5920 | 564 | 325 | COM26 | -5920 | -626 |
| 292 | DUMMY | -4585 | 1770 | 309 | COM58 | -5920 | 494 | 326 | COM25 | -5920 | -696 |
| 293 | DUMMY | -4655 | 1770 | 310 | COM57 | -5920 | 424 | 327 | COM16 | -5920 | -766 |
| 294 | DUMMY | -4725 | 1770 | 311 | COM48 | -5920 | 354 | 328 | COM15 | -5920 | -836 |
| 295 | DUMMY | -4795 | 1770 | 312 | COM47 | -5920 | 284 | 329 | COM14 | -5920 | -906 |
| 296 | DUMMY | -4865 | 1770 | 313 | COM46 | -5920 | 214 | 330 | COM13 | -5920 | -976 |
| 297 | DUMMY | -4935 | 1770 | 314 | COM45 | -5920 | 144 | 331 | COM12 | -5920 | -1046 |
| 298 | DUMMY | -5005 | 1770 | 315 | COM44 | 5920 | 74 | 332 | COM11 | -5920 | -1116 |
| 299 | DUMMY | -5920 | 1194 | 316 | COM43 | -5920 | 4 | 333 | COM10 | -5920 | -1186 |
| 300 | SEGI3 | -5920 | 1124 | 317 | COM42 | -5920 | -66 | 334 | COM9 | -5920 | -1256 |
| 301 | SEGI4 | -5920 | 1054 | 318 | COM41 | -5920 | -136 | 335 | DUMMY | -5920 | -1326 |
| 302 | COMI2 | -5920 | 984 | 319 | COM32 | -5920 | -206 | | | | |

## PIN DESCRIPTIONS

**Table 2. Pin Description**

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Power Supply</td></tr>
<tr><td>VDD</td><td>Power</td><td>Power supply<br>Connect to MPU power supply pin.</td></tr>
<tr><td>VSS</td><td></td><td>0 V (GND)</td></tr>
<tr><td>V0<br>V1<br>V2<br>V3<br>V4</td><td>I/O</td><td>Bias voltage level for LCD driving.<br>Voltages have the following relationship:<br><br>V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS<br><br>When the on-chip power circuit is active, these voltages are generated according to the state of LCD bias, as shown in the table below.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/9 Bias</td><td>(8/9) V0</td><td>(7/9) V0</td><td>(2/9) V0</td><td>(1/9) V0</td></tr>
<tr><td>1/8 Bias</td><td>(7/8) V0</td><td>(6/8) V0</td><td>(2/8) V0</td><td>(1/8) V0</td></tr>
<tr><td>1/7 Bias</td><td>(6/7) V0</td><td>(5/7) V0</td><td>(2/7) V0</td><td>(1/7) V0</td></tr>
<tr><td>1/5 Bias</td><td>(4/5) V0</td><td>(3/5) V0</td><td>(2/5) V0</td><td>(1/5) V0</td></tr>
</table></td></tr>
<tr><td colspan="3">LCD Driver Supply</td></tr>
<tr><td>CAP1+</td><td>O</td><td>Capacitor1+ connect for the internal voltage converter</td></tr>
<tr><td>CAP1–</td><td></td><td>Capacitor1– connect for the internal voltage converter</td></tr>
<tr><td>CAP2+</td><td></td><td>Capacitor2+ connect for the internal voltage converter</td></tr>
<tr><td>CAP2–</td><td></td><td>Capacitor2– connect for the internal voltage converter</td></tr>
<tr><td>CAP3+</td><td></td><td>Capacitor3+ connect for the internal voltage converter</td></tr>
<tr><td>CAP3–</td><td></td><td>Capacitor3– connect for the internal voltage converter</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>Voltage Converter output</td></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjustment pin which is valid only when using external resistors</td></tr>
<tr><td>REF</td><td>I</td><td>Select the reference voltage of the internal voltage regulator.<br>REF = “High”: The reference voltage of the internal voltage regulator is the voltage of VDD.<br>REF = “Low”: The reference voltage of the internal voltage regulator is the internal $V_{REF}$(2.0V).</td></tr>
</table>

**Table 2. Pin Description (Continued)**

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">System Control</td></tr>
<tr><td>CK</td><td>I</td><td>External clock input. It must be fixed to either “High” or “Low” when the internal oscillation circuit is used.<br>In the external clock mode, CK is used as the clock input and the OSC bit should be off.</td></tr>
<tr><td>TMPS1<br>TMPS0</td><td>I</td><td>Select temperature coefficient of the reference voltage.
<table>
<tr><th>TMPS1</th><th>TMPS0</th><th>Temperature Coefficient</th></tr>
<tr><td>0</td><td>0</td><td>– 0.0%/°C</td></tr>
<tr><td>0</td><td>1</td><td>– 0.1%/°C</td></tr>
<tr><td>1</td><td>0</td><td>– 0.2%/°C</td></tr>
<tr><td>1</td><td>1</td><td>– 0.3%/°C</td></tr>
</table></td></tr>
<tr><td>MI</td><td>I</td><td>Select the kinds of the MPU to interface.<br>When MI = “High”: 6800-series MPU interface mode<br>When MI = “Low”: 8080-series MPU interface</td></tr>
<tr><td>IF</td><td>I</td><td>Select the interface bit length when parallel interfacing (PS = “High”).<br>When IF = “High”: 8-bit interface mode<br>When IF = “Low”: 4-bit interface mode</td></tr>
<tr><td>PS</td><td>I</td><td>Select Interface mode with the MPU.<br>When PS = “High”: Parallel interface mode.<br>When PS = “Low”: Serial interface mode.</td></tr>
<tr><td colspan="3">MPU Interface</td></tr>
<tr><td>RESET</td><td>I</td><td>Hardware reset input.<br>Initialization is performed by edge sensing (rising or falling) of the RESET signal.</td></tr>
<tr><td>CSB</td><td>I</td><td>Used as chip selection input.<br>When CSB = “High”, not selected.<br>When CSB = “Low”, selected.</td></tr>
<tr><td>RS</td><td>I</td><td>Used as register selection input.<br>When RS = “High”, Data register.<br>When RS = “Low”, Instruction register.</td></tr>
<tr><td>RW_WR</td><td>I</td><td>When MI = “High” (6800-series MPU interfacing), used as read (RW_WR = “High”) / write (RW_WR = “Low”) selection input (R/$\overline{W}$).<br>When MI = “Low” (8080-series MPU interfacing), used as write enable input ($\overline{WR}$).</td></tr>
<tr><td>E_RD</td><td>I</td><td>When MI = “High” (6800-series MPU interfacing), used as read / write enable input (E).<br>When MI = “Low”(8080-series MPU interfacing), used as read enable input ($\overline{RD}$).</td></tr>
<tr><td>DB0 to<br>DB7</td><td>I/O</td><td>When in 8-bit interface mode, DB0 to DB7 are used as bidirectional data bus pin.<br>When in 4-bit interface mode, only DB4 to DB7 are used as data input pin and DB0 to DB3 are not used.<br>When in serial mode, DB6 (SCL) is used as a serial clock input pin, DB7 (SI) is used as a serial data input pin and the others are not used.</td></tr>
</table>

**Table 2. Pin Description (Continued)**

| Name | I/O | Description |
|---|---|---|
| **LCD Driver Output** | | |
| COM1 to COM64 | O | Common signal output for character display |
| COMI1, COMI2 | O | Common signal output for horizontal icon display.<br>Each signal is the same, but the name is different. |
| SEG1 to SEG128 | O | Segment signal output for character display |
| SEGI1 to SEGI4 | O | Segment signal output for vertical icon display |
| **Test Pin** | | |
| TEST1<br>TEST2<br>TEST3 | I | Test pin.<br>**Connect these to "low".** |

# FUNCTION DESCRIPTION

## SYSTEM INTERFACE

KS0040 has two different MPU interface types: bus mode (8-bit/4-bit length) and serial mode. Whether to use Serial or bus mode is decided by the PS pin.

**Table 3. Various Kinds of MPU Interface**

| PS | MI | IF | CSB | RS | RW_WR | E_RD | DB0 to 3 | DB4 to 5 | DB6 | DB7 |
|---|---|---|---|---|---|---|---|---|---|---|
| Bus mode (H) | 6800-series (H) | 8-bits (H) | CSB | RS | R/$\overline{W}$ | E | DB0 to 3 | DB4 t o5 | DB6 | DB7 |
| | | 4-bits (L) | CSB | RS | (L) | E | * (1) | DB4 to 5 | DB6 | DB7 |
| | 8080-series (L) | 8-bits (H) | CSB | RS | $\overline{WR}$ | $\overline{RD}$ | DB0 to 3 | DB4 to 5 | DB6 | DB7 |
| | | 4-bits (L) | CSB | RS | $\overline{WR}$ | (H)/(L) | * | DB4 to 5 | DB6 | DB7 |
| Serial mode (L) | (H)/(L) (2) | (H)/(L) | CSB | RS | (H)/(L) | (H)/(L) | * | * | SCL | SI |

**NOTES:**
1. Dont care (high, low or open)
2. Fixed high ($V_{DD}$) or low ($V_{SS}$)

**PS**

| | |
|---|---|
| H | Parallel interface mode |
| L | Serial interface mode |

**MI**

| | |
|---|---|
| H | 6800-Series MPU interface |
| L | 8080-Series MPU interface mode |

**IF**

| | |
|---|---|
| H | 8-Bit interface mode |
| L | 4-Bit interface mode |

**CSB**

| | |
|---|---|
| H | Chip not selected |
| L | Chip selected |

**RS**

| | |
|---|---|
| H | Data register select |
| L | Instruction register select |

**RW_WR**

| | |
|---|---|
| MI=H | 6800-series read/write select |
| MI=L | 8080-series “High” write enable |

**E_RD**

| | |
|---|---|
| MI=H | 6800-series active “Low” enable |
| MI=L | 8080-series “Low” read enable |

**SCL(DB6)**

| | |
|---|---|
| PS=L | Serial clock input |

**SI(DB7)**

| | |
|---|---|
| PS=L | Serial data input |

### Interface with MPU in Parallel Bus Mode (PS = "High")

In parallel interface mode, whether to use the 6800-series or 8080-series MPU is decided by the MI pin, and the interface bit length (8-bit / 4-bit) is selected by the IF pin.
During write operation, the 16-bit data register (DR) and 8-bit instruction register (IR) are used.
The data register (DR) is used as a temporary storage place for data from MPU, being written into DDRAM / CGRAM / ICONRAM. The target RAM is selected by RAM select instruction.
The Instruction register (IR) is used only to store instruction code transferred from MPU.
To select either DR or IR, use the RS input pin in parallel mode or serial mode.

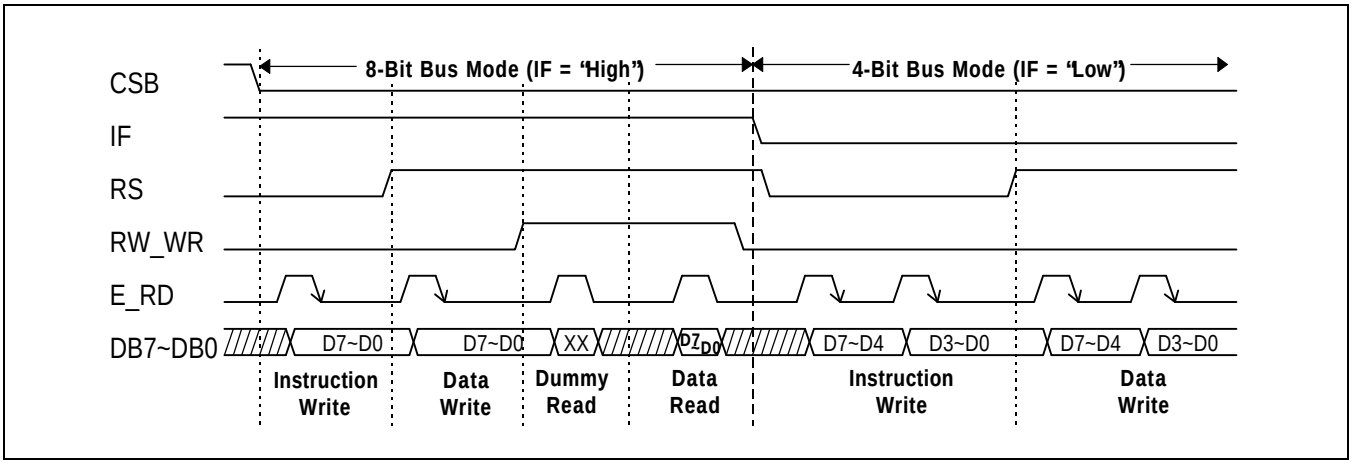



**Figure 3. Timing Diagram of 6800-series Bus Mode Data Transfer (MI = "High")**

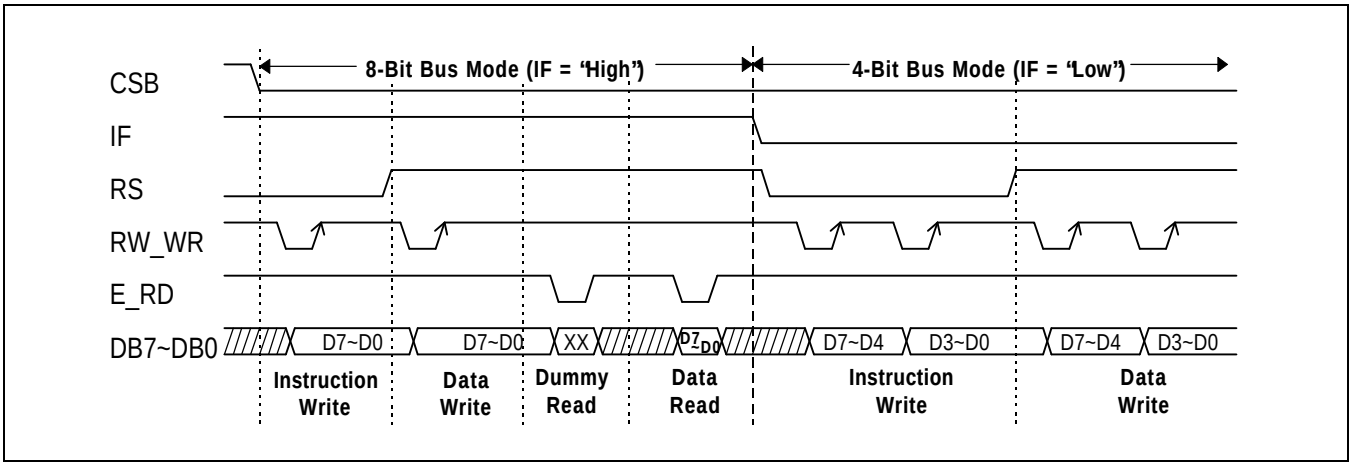



**Figure 4. Timing Diagram of 8080-series Bus Mode Data Transfer (MI = "Low")**

### Interface With MPU in Serial Bus Mode (PS = "Low")

When PS input pin is "Low", clock synchronized serial interface mode is selected.
At this time, the following four ports are used: SCL (DB6, synchronizing transfer clock input), SI (DB7, serial data input), RS (register selection input), and CSB (chip selection input).
By setting CSB to "Low", KS0040 can receive SCL input. If CSB is set to "High", KS0040 initializes the interface circuit (8-bit shift register and 3-bit counter).
Serial data is input in the order of "D7, D6, D5, D4, D3, D2, D1, D0" from the serial data input pin (SI = DB7) at the rising edge of the serial clock (SCL = DB6).
At the rising edge of the 8th serial clock, the serial data (D7–D0) is converted into 8-bit bus data. The RS input of the DR/IR selection is latched at the rising edge of the 8th serial clock (SCL).

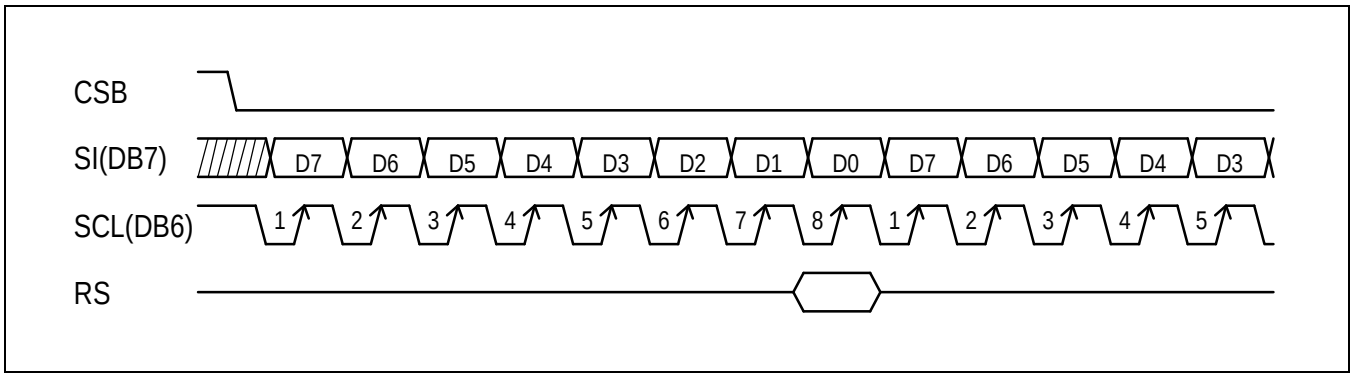



**Figure 5. Timing Diagram of Serial Data Transfer**

## RAM MAP

Internal RAM has a total of 1,200 bytes, consisting of the following components: DDRAM (128 bytes), ICONRAM (48 bytes) and CGRAM (1,024 bytes).

**Table 4. RAM Map**

| R3 | R2 | R1 | R0 | Address (Hex) | RAM Data Usage (D7 to D0) | RAM Sizes |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 00 – 0F<br>10 – 1F<br>20 – 2F<br>30 – 3F<br>40 – 4F<br>50 – 5F<br>60 – 6F<br>70 – 7F | DDRAM (1st Line) [EXT = 0]<br>DDRAM (2st Line) [EXT = 0]<br>DDRAM (3rd Line) [EXT = 0]<br>DDRAM (4th Line) [EXT = 1]<br>DDRAM (5th Line) [EXT = 1]<br>DDRAM (6th Line) [EXT = 1]<br>DDRAM (7th Line) [EXT = 1]<br>DDRAM (8th Line) [EXT = 1] | 128 bytes |
| 0 | 0 | 0 | 1 | 00 – 0F<br>10 – 1F<br>20 – 2F | ICONRAM Upper 128 Icons (C1 to C128)<br>ICONRAM Lower 128 Icons (C129 to C252)<br>ICONRAM COMS Data (S1 to S128) | 48 bytes |
| 1 | 0 | 0 | 0 | 00 – 1F<br>20 – 3F<br>40 – 5F<br>60 – 7F | CGRAM 1st 16 × 16 pattern<br>CGRAM 2nd 16 × 16 pattern<br>CGRAM 3rd 16 × 16 pattern<br>CGRAM 4th 16 × 16 pattern | 128 bytes<br>(page 0) |
| 1 | 0 | 0 | 1 | 00 – 1F<br>20 – 3F<br>40 – 5F<br>60 – 7F | CGRAM 5th 16 × 16 pattern<br>CGRAM 6th 16 × 16 pattern<br>CGRAM 7th 16 × 16 pattern<br>CGRAM 8th 16 × 16 pattern | 128 bytes<br>(page 1) |
| 1 | 0 | 1 | 0 | 00 – 1F<br>20 – 3F<br>40 – 5F<br>60 – 7F | CGRAM 9th 16 × 16 pattern<br>CGRAM 10th 16 × 16 pattern<br>CGRAM 11th 16 × 16 pattern<br>CGRAM 12th 16 × 16 pattern | 128 bytes<br>(page 2) |
| 1 | 0 | 1 | 1 | 00 – 1F<br>20 – 3F<br>40 – 5F<br>60 – 7F | CGRAM 13th 16 × 16 pattern<br>CGRAM 14th 16 × 16 pattern<br>CGRAM 15th 16 × 16 pattern<br>CGRAM 16th 16 × 16 pattern | 128 bytes<br>(page 3) |
| 1 | 1 | 0 | 0 | 00 – 1F<br>20 – 3F<br>40 – 5F<br>60 – 7F | CGRAM 17th 16 × 16 pattern<br>CGRAM 18th 16 × 16 pattern<br>CGRAM 19th 16 × 16 pattern<br>CGRAM 20th 16 × 16 pattern | 128 bytes<br>(page 4) |
| 1 | 1 | 0 | 1 | 00 – 1F<br>20 – 3F<br>40 – 5F<br>60 - 7F | CGRAM 21th 16 × 16 pattern<br>CGRAM 22th 16 × 16 pattern<br>CGRAM 23th 16 × 16 pattern<br>CGRAM 24th 16 × 16 pattern | 128 bytes<br>(page 5) |

**Table 4. RAM Map (Continued)**

| R3 | R2 | R1 | R0 | Address (Hex) | RAM Data Usage (D7 to D0) | RAM Sizes |
|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 00 – 1F<br>20 – 3F<br>40 – 5F<br>60 – 7F | CGRAM 25th 16 x 16 pattern<br>CGRAM 26th 16 x 16 pattern<br>CGRAM 27th 16 x 16 pattern<br>CGRAM 28th 16 x 16 pattern | 128 bytes<br>(page 6) |
| 1 | 1 | 1 | 1 | 00 – 1F<br>20 – 3F<br>40 – 5F<br>60 – 7F | CGRAM 29th 16 × 16 pattern<br>CGRAM 30th 16 × 16 pattern<br>CGRAM 31th 16 × 16 pattern<br>CGRAM 32th 16 × 16 pattern | 128 bytes<br>(page 7) |

**NOTE:** R3 to R0: RAM/System select register

### Display Data RAM (DDRAM)

DDRAM stores 16-bit character code in FCGROM/CGRAM and 8-bit character code in HCGROM. Its maximum capacity is 128-bytes (64-words: 64 characters of a full-size font or 128 characters of a half-size font). The displayable area is 64 bytes and the other is extended data area. To display extended DDRAM data, set the EXT bit “high” in system register set instruction.
DDRAM address is set by the address counter (AC) as a hexadecimal number.

| MSB | | | | | | LSB |
|---|---|---|---|---|---|---|
| **AC6** | **AC5** | **AC4** | **AC3** | **AC2** | **AC1** | **AC0** |

### The relations of DDRAM address and display position

### When DDRAM is set to normal mode (EXT = Low)

| | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th |
|---|---|---|---|---|---|---|---|---|
| COM1 – COM16 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| COM17 – COM32 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| COM33 – COM48 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
| COM49 – COM64 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |

(a) Display shift is not performed

| | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th |
|---|---|---|---|---|---|---|---|---|
| COM1 – COM16 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| COM17 – COM32 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
| COM33 – COM48 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |
| COM49 – COM64 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |

(b) Display shift up is performed

| | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th |
|---|---|---|---|---|---|---|---|---|
| COM1 – COM16 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |
| COM17 – COM32 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| COM33 – COM48 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| COM49 – COM64 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |

(c) Display shift down is performed

**When DDRAM is set to extended mode (EXT = High)**

| | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th |
|---|---|---|---|---|---|---|---|---|
| COM1 – COM16 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| COM17 – COM32 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| COM33 – COM48 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
| COM49 – COM64 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F |
| | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 5A | 5B | 5C | 5D | 5E | 5F |
| | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 6A | 6B | 6C | 6D | 6E | 6F |
| | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 7A | 7B | 7C | 7D | 7E | 7F |

(a) Display shift is not performed

| | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th |
|---|---|---|---|---|---|---|---|---|
| COM1 – COM16 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| COM17 – COM32 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
| COM33 – COM48 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |
| COM49 – COM64 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F |
| | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 5A | 5B | 5C | 5D | 5E | 5F |
| | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 6A | 6B | 6C | 6D | 6E | 6F |
| | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 7A | 7B | 7C | 7D | 7E | 7F |
| | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |

(b) Display shift up is performed

| | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th |
|---|---|---|---|---|---|---|---|---|
| COM1 – COM16 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 7A | 7B | 7C | 7D | 7E | 7F |
| COM17 – COM32 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| COM33 – COM48 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| COM49 – COM64 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
| | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F |
| | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 5A | 5B | 5C | 5D | 5E | 5F |
| | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 6A | 6B | 6C | 6D | 6E | 6F |

(c) Display shift down is performed

### Character Generator RAM (CGRAM)

CGRAM is used for user defined character patterns. It can generate 32 full-size fonts (16 x 16 bits) including the cursor position. The CGRAM capacity is large enough to support bitmap graphics 128 × 64 dot.
To use the character pattern in CGRAM, write the character code into DDRAM as shown in Table 5.

**Table 5. Relationship Between Character Code(DDRAM) and Character Pattern(CGRAM)**

| Character Code (DDRAM DATA) | CGRAM ADDRESS | | | | | | | | | | CGRAM DATA (A0 = 0) | | | | | | | | CGRAM DATA (A0 = 1) | | | | | | | | Pattern Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | R3 | R2 | R1 | R0 | A6 | A5 | A4 | A3 | A2 | A1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0000h | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | Pattern1 |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 001Fh | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | □ | □ | Pattern32 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | □ | □ | □ | ■ | □ | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | □ | □ | □ | ■ | □ | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | □ | □ | ■ | □ | □ | □ | □ | ■ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | □ | □ | ■ | □ | □ | □ | □ | ■ | □ | □ | □ | □ | ■ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | □ | ■ | □ | □ | □ | □ | □ | ■ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | ■ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | □ | □ | □ | ■ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |

**Table 6. Example for Bitmap Graphic by CGRAM**

| Character Code (DDRAM DATA) | CGRAM ADDRESS | | | | | | | | | | CGRAM DATA (A0 = 0) | | | | | | | | CGRAM DATA (A0 = 1) | | | | | | | | Pattern Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | R3 | R2 | R1 | R0 | A6 | A5 | A4 | A3 | A2 | A1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0000h | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | Pattern1 |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | □ | □ | □ | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | □ | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | □ | ■ | ■ | ■ | ■ | ■ | ■ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | ■ | □ | □ | □ | ■ | ■ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | ■ | □ | □ | □ | ■ | □ | □ | □ | □ | ■ | ■ | ■ | ■ | □ | □ | □ | |
| 0001h | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | Pattern2 |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | ■ | ■ | ■ | ■ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | ■ | ■ | ■ | □ | □ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | ■ | □ | □ | □ | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | □ | □ | □ | □ | □ | □ | □ | □ | ■ | ■ | ■ | ■ | ■ | □ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | □ | □ | □ | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | ■ | □ | □ | |
| | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | □ | □ | ■ | ■ | ■ | ■ | □ | □ | □ | □ | □ | □ | □ | ■ | □ | □ | |
| : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |

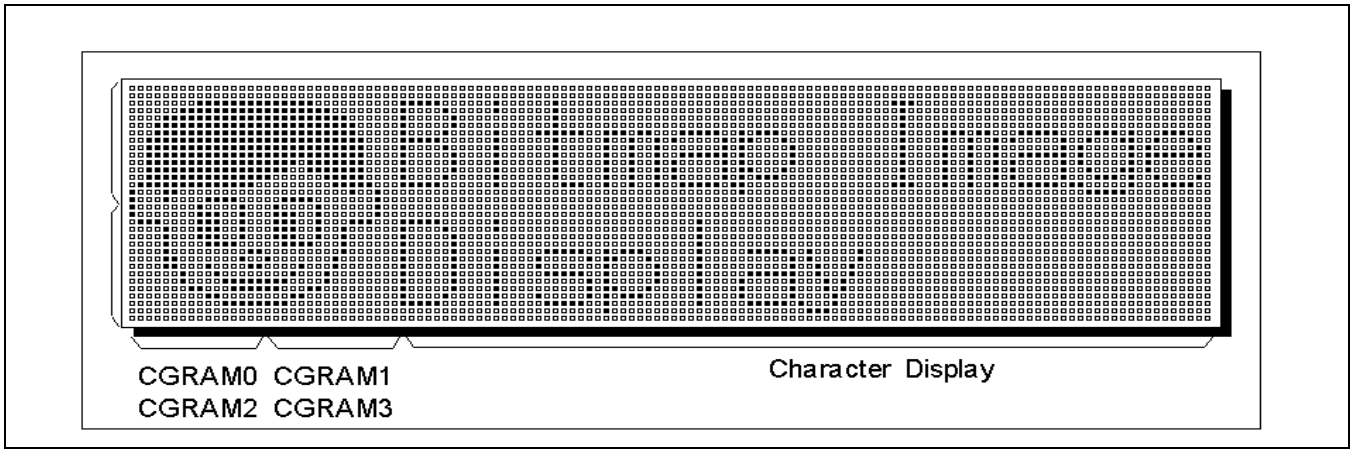



**Figure 6. Example for Bitmap Display with Character**

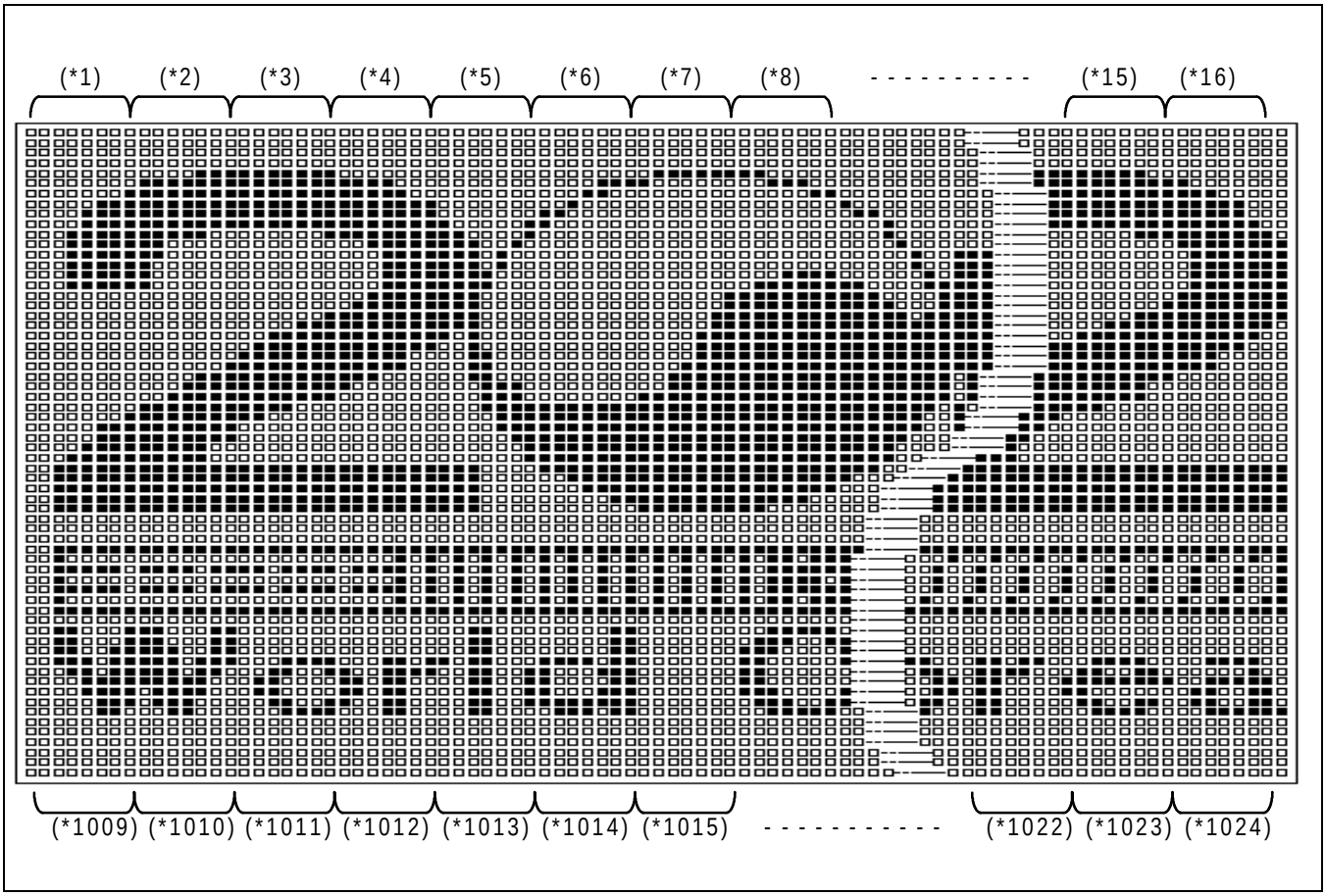



**Figure 7. Relationship Between CGRAM Full Graphic Mode Data Writing and Display Pattern (FG = "high")**

During CGROM full graphic mode, CGRAM data is written from (*1) to (*1024) by 8-bit length

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| (*1) | (*2) | (*3) | (*4) | (*5) | (*6) | (*7) | (*8) | .... | .... | (*15) | (*16) |
| (*17) | (*18) | (*19) | (*20) | (*21) | (*22) | (*23) | (*24) | .... | .... | (*31) | (*32) |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| (*1009) | (*1010) | (*1011) | (*1012) | (*1013) | (*1014) | (*1015) | .... | .... | (*1022) | (*1023) | (*1024) |

### Segment & Common Icon RAM (ICONRAM)

ICONRAM has segment/common icon pattern data.
COMI1 or COMI2 and SEGI1 to 4 enable the data of ICONRAM to display icons.

**Table 7. Relationship Between ICONRAM Address and Display Pattern**

| ICONRAM Address | | | | | | ICONRAM Bits | | | | | | | | Icons |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A5 | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | VL1 | VL2 | VR1 | VR2 | VL3 | VL4 | VR3 | VR4 | Upper 128 SEGI Icons Data (*1) |
| | | 0 | 0 | 0 | 1 | VL5 | VL6 | VR5 | VR6 | VL7 | VL8 | VR7 | VR8 | |
| | | | | . | | | | | | . | | | | |
| | | | | . | | | | | | . | | | | |
| | | 1 | 1 | 1 | 0 | VL57 | VL58 | VR57 | VR58 | VL59 | VL60 | VR59 | VR60 | |
| | | 1 | 1 | 1 | 1 | VL61 | VL62 | VR61 | VR62 | VL63 | VL64 | VR63 | VR64 | |
| 0 | 1 | 0 | 0 | 0 | 0 | VL65 | VL66 | VR65 | VR66 | VL67 | VL68 | VR67 | VR68 | Lower 128 SEGI Icons Data (*2) |
| | | 0 | 0 | 0 | 1 | VL69 | VL70 | VR69 | VR70 | VL71 | VL72 | VR71 | VR72 | |
| | | | | . | | | | | | . | | | | |
| | | | | . | | | | | | . | | | | |
| | | 1 | 1 | 1 | 0 | VL121 | VL122 | VR121 | VR122 | VL123 | VL124 | VR123 | VR124 | |
| | | 1 | 1 | 1 | 1 | VL125 | VL126 | VR125 | VR126 | VL127 | VL128 | VR127 | VR128 | |
| 1 | 0 | 0 | 0 | 0 | 0 | H1 | H2 | H3 | H4 | H5 | H6 | H7 | H8 | COMI Icons Data (*3) |
| | | 0 | 0 | 0 | 1 | H9 | H10 | H11 | H12 | H13 | H14 | H15 | H16 | |
| | | | | . | | | | | | . | | | | |
| | | | | . | | | | | | . | | | | |
| | | 1 | 1 | 1 | 0 | H113 | H114 | H115 | H116 | H117 | H118 | H119 | H120 | |
| | | 1 | 1 | 1 | 1 | H121 | H122 | H123 | H124 | H125 | H126 | H127 | H128 | |

**NOTES:**
1. VLn: Vertical Left n-th icon, VRn: Vertical Right n-th icon
2. Hn: Horizontal n-th icon (where n = 1 to 128)

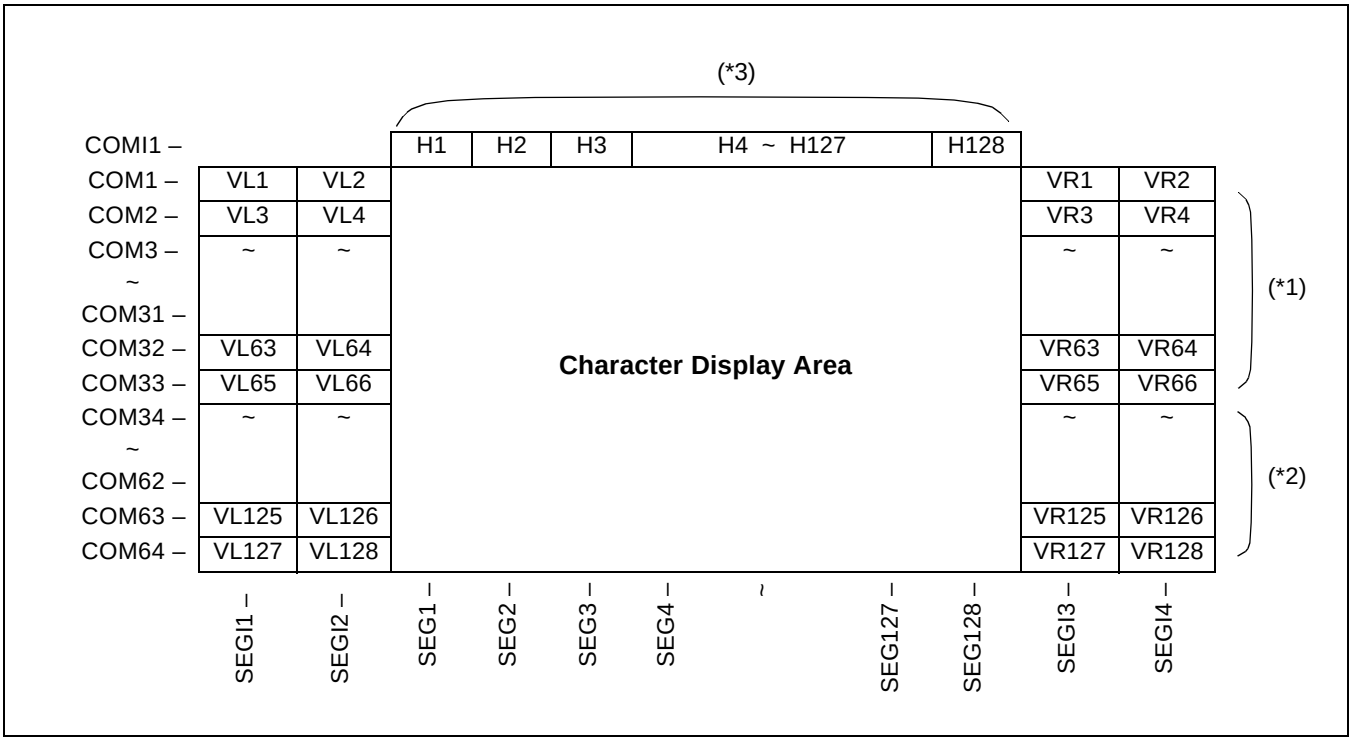



**Figure 8. Relationship Between Icon Pattern Data and COM/SEG Line (When DIRC = 0, DIRS = 0)**

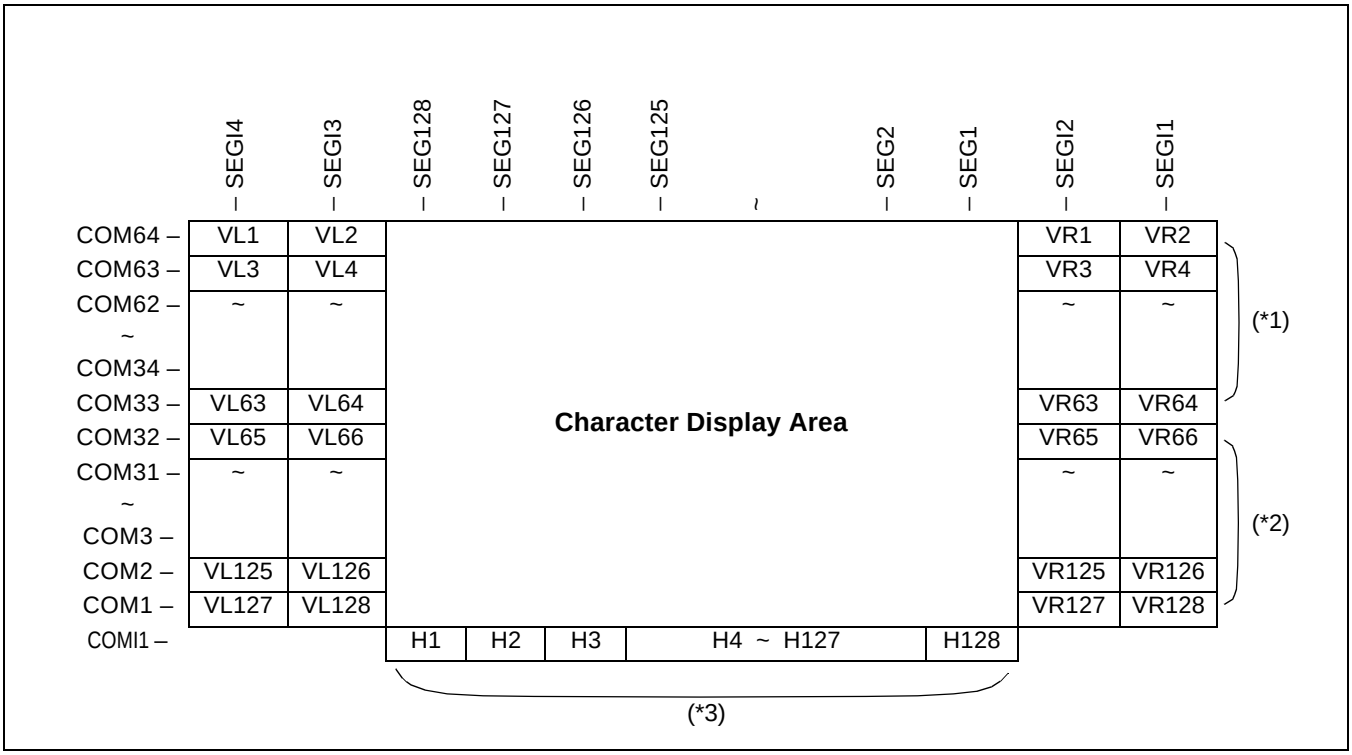



**Figure 9. Relationship Between Icon Pattern Data and COM/SEG Line (When DIRC = 1, DIRS = 1)**

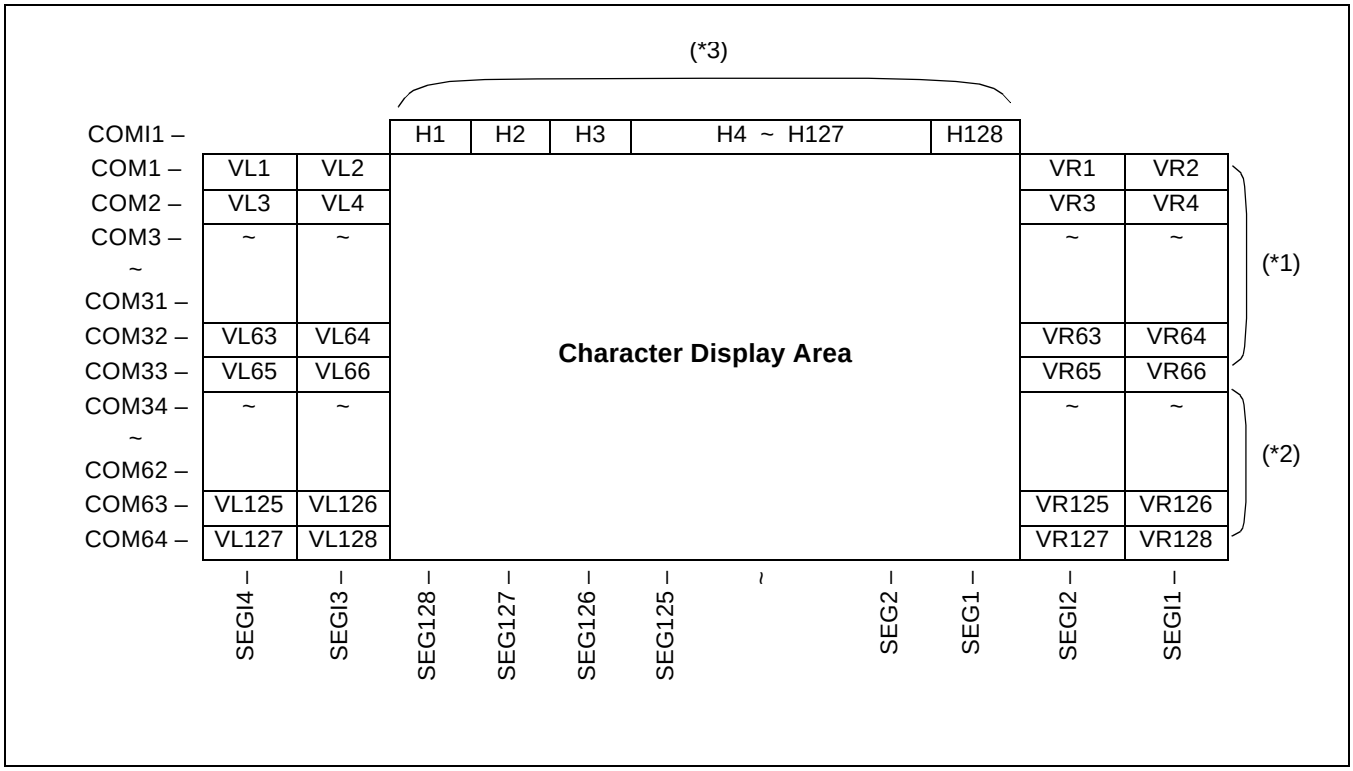



**Figure 10. Relationship Between Icon Pattern Data and COM/SEG Line (When DIRC = 0, DIRS = 1)**

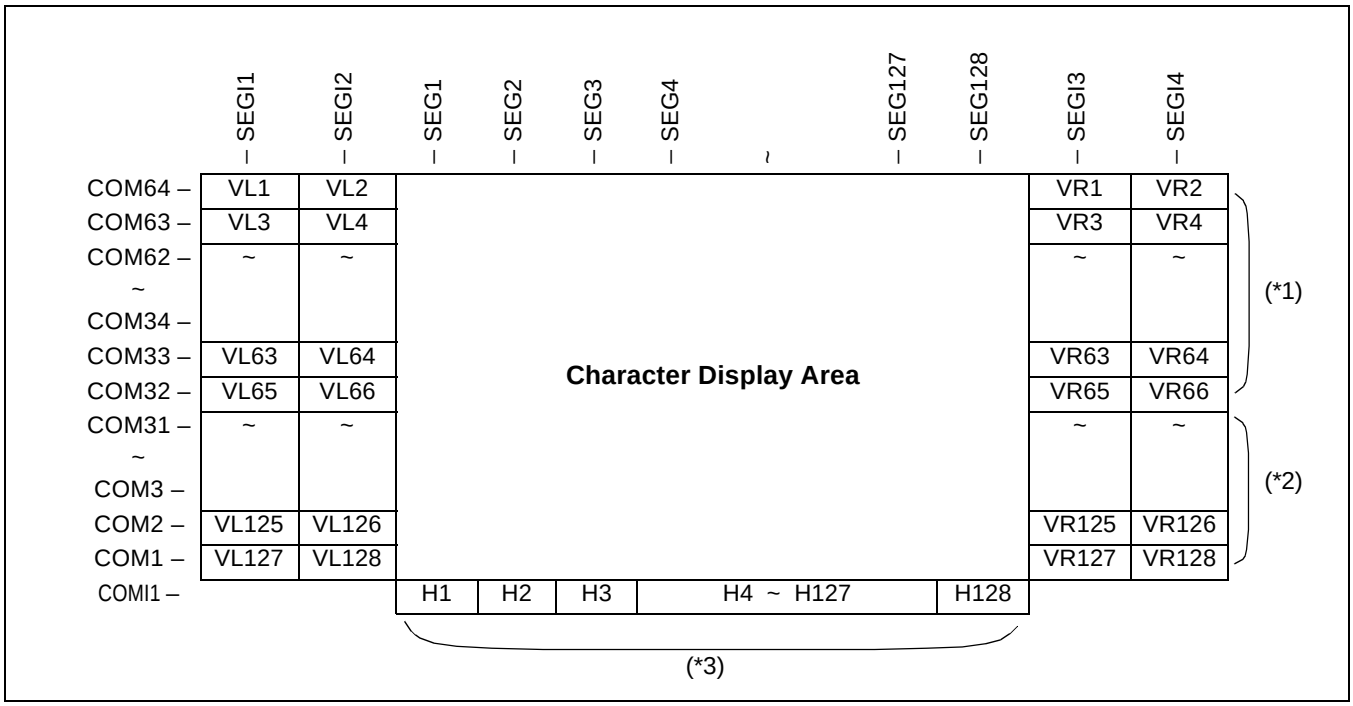
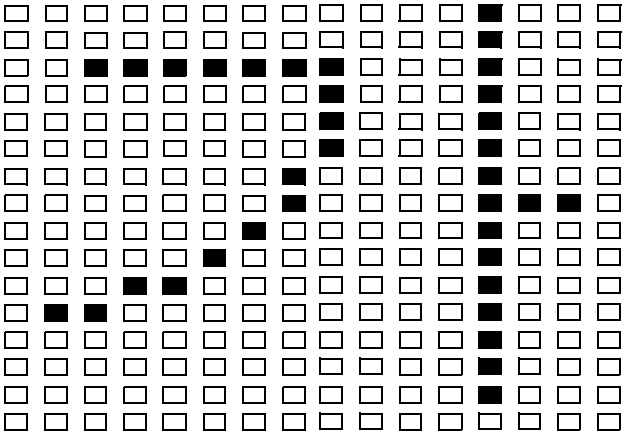



**Figure 11. Relationship Between Icon Pattern Data and COM/SEG Line (When DIRC = 1, DIRS = 0)**

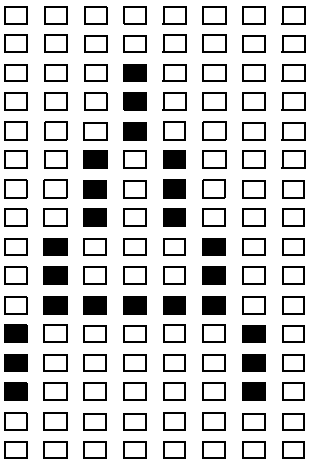
### CHARACTER GENERATOR ROM FOR A FULL-SIZE FONT (FCGROM)

FCGROM generates 16 × 16 character patterns from the character generate code in DDRAM. FCGROM has 8,192 character patterns (16×16-dot), including the cursor position for Asian language character fonts (like Chinese, Japanese Kanji, and Korean). If the data in the cursor position bit are high, they are included in the character pattern. So, the selected positions are always ON without regard to cursor position.

| FCGROM Address | FONT Data (D15 ~ D0) |
|---|---|
| A13 ~ A0 | F E D C B A 9 8 7 6 5 4 3 2 1 0 |
| 0380(h) |  |

### CHARACTER GENERATOR ROM FOR A HALF-SIZE FONT (HCGROM)

HCGROM generates 8 × 16 character patterns from the character generate code in DDRAM. HCGROM has 128 character patterns (8 × 16-dot), including the cursor position for half-size fonts (like alphanumeric characters and symbols). If the data in the cursor position bit are high, they are included in the character pattern. So, the selected positions are always ON without regard to cursor position.

| HCGROM Address | FONT Data (D7 ~ D0) |
|---|---|
| A6 ~ A0 | 7 6 5 4 3 2 1 0 |
| 41(h) |  |

### KSC5601 CODE MAP

| KSC5601 Code (Hex) | KS0040 FCGROM Code (Hex) | Font Data |
|---|---|---|
| – | 0000 – 001F | CGRAM Font Area |
| A1A1 – ACFE | 0020 – 037F | Symbol Character Area |
| B0A1 – B0FE | 0380 – 03DD | ° ¡- - - - - - - - - - - - - - ° þ |
| B1A1 – B1FE | 03DE – 043B | ± ¡- - - - - - - - - - - - - - ± þ |
| B2A1 – B2FE | 043C – 0499 | ² ¡- - - - - - - - - - - - - - ² þ |
| B3A1 – B3FE | 049A – 04F7 | ³ ¡- - - - - - - - - - - - - - ³ þ |
| B4A1 – B4FE | 04F8 – 0555 | ´ ¡- - - - - - - - - - - - - - ´ þ |
| B5A1 – B5FE | 0556 – 05B3 | µ ¡- - - - - - - - - - - - - - µ þ |
| B6A1 – B6FE | 05B4 – 0611 | ¶ ¡- - - - - - - - - - - - - - ¶ þ |
| B7A1 – B7FE | 0612 – 066F | · ¡- - - - - - - - - - - - - - · þ |
| B8A1 – B8FE | 0670 – 06CD | ¸ ¡- - - - - - - - - - - - - - ¸ þ |
| B9A1 – B9FE | 06CE – 072B | ¹ ¡- - - - - - - - - - - - - - ¹ þ |
| BAA1 – BAFE | 072C – 0789 | º ¡- - - - - - - - - - - - - - º þ |
| BBA1 – BBFE | 078A – 07E7 | » ¡- - - - - - - - - - - - - - » þ |
| BCA1 – BCFE | 07E8 – 0845 | ¼ ¡- - - - - - - - - - - - - - ¼ þ |
| BDA1 – BDFE | 0846 – 08A3 | ½ ¡- - - - - - - - - - - - - - ½ þ |
| BEA1 – BEFE | 08A4 – 0901 | ¾ ¡- - - - - - - - - - - - - - ¾ þ |
| BFA1 – BFFE | 0902 – 095F | ¿ ¡- - - - - - - - - - - - - - ¿ þ |
| C0A1 – C0FE | 0960 – 09BD | À ¡- - - - - - - - - - - - - - À þ |
| C1A1 – C1FE | 09BC – 0A1B | Á ¡- - - - - - - - - - - - - - Á þ |
| C2A1 – C2FE | 0A1C – 0A7C | Â ¡- - - - - - - - - - - - - - Â þ |
| C3A1 – C3FE | 0A7D – 0AD7 | Ã ¡- - - - - - - - - - - - - - Ã þ |
| C4A1 – C4FE | 0AD8 – 0B35 | Ä ¡- - - - - - - - - - - - - - Ä þ |
| C5A1 – C5FE | 0B36 – 0B93 | Å ¡- - - - - - - - - - - - - - Å þ |
| C6A1 – C6FE | 0B94 – 0BF1 | Æ ¡- - - - - - - - - - - - - - Æ þ |
| C7A1 – C7FE | 0BF2 – 0C4F | Ç ¡- - - - - - - - - - - - - - Ç þ |
| C8A1 – C8FE | 0C50 – 0CAD | È ¡- - - - - - - - - - - - - - È þ |
| CAA1 – CAFE | 0CB0 – 0D0D | Ê ¡- - - - - - - - - - - - - - Ê þ |
| CBA1 – CBFE | 0D0E – 0D6B | Ë ¡- - - - - - - - - - - - - - Ë þ |
| CCA1 – CCFE | 0D6C – 0DC9 | Ì ¡- - - - - - - - - - - - - - Ì þ |
| CDA1 – CDFE | 0DCA – 0E27 | Í ¡- - - - - - - - - - - - - - Í þ |
| CEA1 – CEFE | 0E28 – 0E85 | Î ¡- - - - - - - - - - - - - - Î þ |
| CFA1 – CFFE | 0E86 – 0EE3 | Ï ¡- - - - - - - - - - - - - - Ï þ |
| D0A1 – D0FE | 0EE4 – 0F41 | Ð ¡- - - - - - - - - - - - - - Ð þ |
| D1A1 – D1FE | 0F42 – 0F9F | Ñ ¡- - - - - - - - - - - - - - Ñ þ |
| D2A1 – D2FE | 0FA0 – 0FFD | Ò ¡- - - - - - - - - - - - - - Ò þ |
| D3A1 – D3FE | 0FFE – 105B | Ó ¡- - - - - - - - - - - - - - Ó þ |
| D4A1 – D4FE | 105C – 10B9 | Ô ¡- - - - - - - - - - - - - - Ô þ |
| D5A1 – D5FE | 10BA – 1117 | Õ ¡- - - - - - - - - - - - - - Õ þ |
| D6A1 – D6FE | 1118 – 1175 | Ö ¡- - - - - - - - - - - - - - Ö þ |
| D7A1 – D7FE | 1176 – 11D3 | × ¡- - - - - - - - - - - - - - × þ |
| D8A1 – D8FE | 11D4 – 1231 | Ø ¡- - - - - - - - - - - - - - Ø þ |
| D9A1 – D9FE | 1232 – 128F | Ù ¡- - - - - - - - - - - - - - Ù þ |
| DAA1 – DAFE | 1290 – 12FD | Ú ¡- - - - - - - - - - - - - - Ú þ |
| DBA1 – DBFE | 12EE – 134B | Û ¡- - - - - - - - - - - - - - Û þ |
| DCA1 – DCFE | 134C – 13A9 | Ü ¡- - - - - - - - - - - - - - Ü þ |
| DDA1 – DDFE | 13AA – 1407 | Ý ¡- - - - - - - - - - - - - - Ý þ |

**KSC5601 CODE MAP (Continued)**

| KSC5601 Code (Hex) | KS0040 FCGROM Code (Hex) | Font Data |
|---|---|---|
| DEA1 – DEFE | 1408 – 1465 | Þ ¡- - - - - - - - - - - - - - Þ þ |
| DFA1 – DFFE | 1466 – 14C3 | ß ¡- - - - - - - - - - - - - - ß þ |
| E0A1 – E0FE | 14C4 – 1521 | à ¡- - - - - - - - - - - - - - à þ |
| E1A1 – E1FE | 1522 – 157F | á ¡- - - - - - - - - - - - - - á þ |
| E2A1 – E2FE | 1580 – 15DD | â ¡- - - - - - - - - - - - - - â þ |
| E3A1 – E3FE | 15DE – 163B | ã ¡- - - - - - - - - - - - - - ã þ |
| E4A1 – E4FE | 163C – 1699 | ä ¡- - - - - - - - - - - - - - ä þ |
| E5A1 – E5FE | 169A – 16F7 | å ¡- - - - - - - - - - - - - - å þ |
| E6A1 – E6FE | 16F8 – 1755 | æ ¡- - - - - - - - - - - - - - æ þ |
| E7A1 – E7FE | 1756 – 17B3 | ç ¡- - - - - - - - - - - - - - ç þ |
| E8A1 – E8FE | 17B4 – 1811 | è ¡- - - - - - - - - - - - - - è þ |
| E9A1 – E9FE | 1812 – 186F | é ¡- - - - - - - - - - - - - - é þ |
| EAA1 – EAFE | 1870 – 18CD | ê ¡- - - - - - - - - - - - - - ê þ |
| EBA1 – EBFE | 18CE – 192B | ë ¡- - - - - - - - - - - - - - ë þ |
| ECA1 – ECFE | 192C – 1989 | ì ¡- - - - - - - - - - - - - - ì þ |
| EDA1 – EDFE | 198A – 19E7 | í ¡- - - - - - - - - - - - - - í þ |
| EEA1 – EEFE | 19E8 – 1A45 | î ¡- - - - - - - - - - - - - - î þ |
| EEA1 – EFFE | 1A46 – 1AA3 | ï ¡- - - - - - - - - - - - - - ï þ |
| F0A1 – F0FE | 1AA4 – 1B01 | ð ¡- - - - - - - - - - - - - - ð þ |
| F1A1 – F1FE | 1B02 – 1B5F | ñ ¡- - - - - - - - - - - - - - ñ þ |
| F2A1 – F2FE | 1B60 – 1BBD | ò ¡- - - - - - - - - - - - - - ò þ |
| F3A1 – F3FE | 1BBE – 1C1B | ó ¡- - - - - - - - - - - - - - ó þ |
| F4A1 – F4FE | 1C1C – 1C79 | ô ¡- - - - - - - - - - - - - - ô þ |
| F5A1 – F5FE | 1C7A – 1CD7 | õ ¡- - - - - - - - - - - - - - õ þ |
| F6A1 – F6FE | 1CD8 – 1D35 | ö ¡- - - - - - - - - - - - - - ö þ |
| F7A1 – F7FE | 1D36 – 1D93 | ÷ ¡- - - - - - - - - - - - - - ÷ þ |
| F8A1 – F8FE | 1D94 – 1DF1 | ø ¡- - - - - - - - - - - - - - ø þ |
| F9A1 – F9FE | 1DF2 – 1E4F | ù ¡- - - - - - - - - - - - - - ù þ |
| FAA1 – FAFE | 1E50 – 1EAD | ú ¡- - - - - - - - - - - - - - ú þ |
| FBA1 – FBFE | 1EAE – 1F0B | û ¡- - - - - - - - - - - - - - û þ |
| FCA1 – FCFE | 1F0C – 1F69 | ü ¡- - - - - - - - - - - - - - ü þ |
| FDA1 – FDFE | 1F6A – 1FC7 | ý ¡- - - - - - - - - - - - - - ý þ |

## LOW POWER CONSUMPTION MODE

KS0040 has a sleep mode for saving power during standby period.
(Refer to “INITIALIZING & POWER SAVE MODE SETUP”)

**Sleep Mode**
In sleep mode, the power circuit and oscillation circuit are turned off.
This mode lowers power consumption by reducing current to almost the static current level.

- Liquid crystal display output
  - — COM1 to COM64, COMI1, 2: Vss level
  - — SEG1 to SEG128, SEGI1, 2, 3, 4: Vss level
- DDRAM, CGRAM, ICONRAM and register-written information is saved.
- Operation mode is retained, the same as it was prior to execution of sleep mode. All internal circuits are stopped.
- Power circuit and oscillation circuit
  - — The built-in supply circuit and oscillation circuit are turned off automatically by using the sleep command.

## LCD DRIVING CIRCUIT

LCD Driver circuit has 65 common and 132 segment signals for LCD driving.
The data from CGROM / CGRAM / ICONRAM is transferred to a 128-bit segment latch serially in 8-bit units, and then stored in the 128-bit shift latch. The data from ICONRAM is stored in a 4-bit latch.
When each common line is selected by a 65-bit common register, segment data and segment icon data also output through a segment driver from the 128-bit segment latch and 4-bit segment icon latch.
KS0040 has common and segment bidirectional functions for use in various panel applications.
(Refer to Table 9. and Table 10.)

**Table 8. SEG Data Shift Direction**

| DIRS | SEG Data Shift Direction |
|---|---|
| Low | SEGI1, SEGI2 ,SEG1 → . . . . . → SEG128, SEGI3, SEGI4 |
| High | SEGI4, SEGI3, SEG128 → . . . . . → SEG1, SEGI2, SEGI1 |

**Table 9. COM Data Shift Direction**

| Duty | DIRC | COM Data Shift Direction |
|---|---|---|
| 1/17 (1-line mode) | Low | COM1 → . . . . . → COM16, COMI1(COMI2) |
| | High | COM16 → . . . . . → COM1, COMI1(COMI2) |
| 1/33 (2-line mode) | Low | COM1 → . . . . . → COM32, COMI1(COMI2) |
| | High | COM32 → . . . . . → COM1, COMI1(COMI2) |
| 1/49 (3-line mode) | Low | COM1 → . . . . . → COM48, COMI1(COMI2) |
| | High | COM48 → . . . . . → COM1, COMI1(COMI2) |
| 1/65 (4-line mode) | Low | COM1 → . . . . . → COM64, COMI1(COMI2) |
| | High | COM64 → . . . . . → COM1, COMI1(COMI2) |

### DISPLAY SHIFT CONTROL

KS0040 has vertical dot-by-dot or character-by-character shift functions, which are useful when the display panel size is less than 4 lines and you want to display the hidden-line data, or when the extended DDRAM is set and you want to display extended DDRAM data.

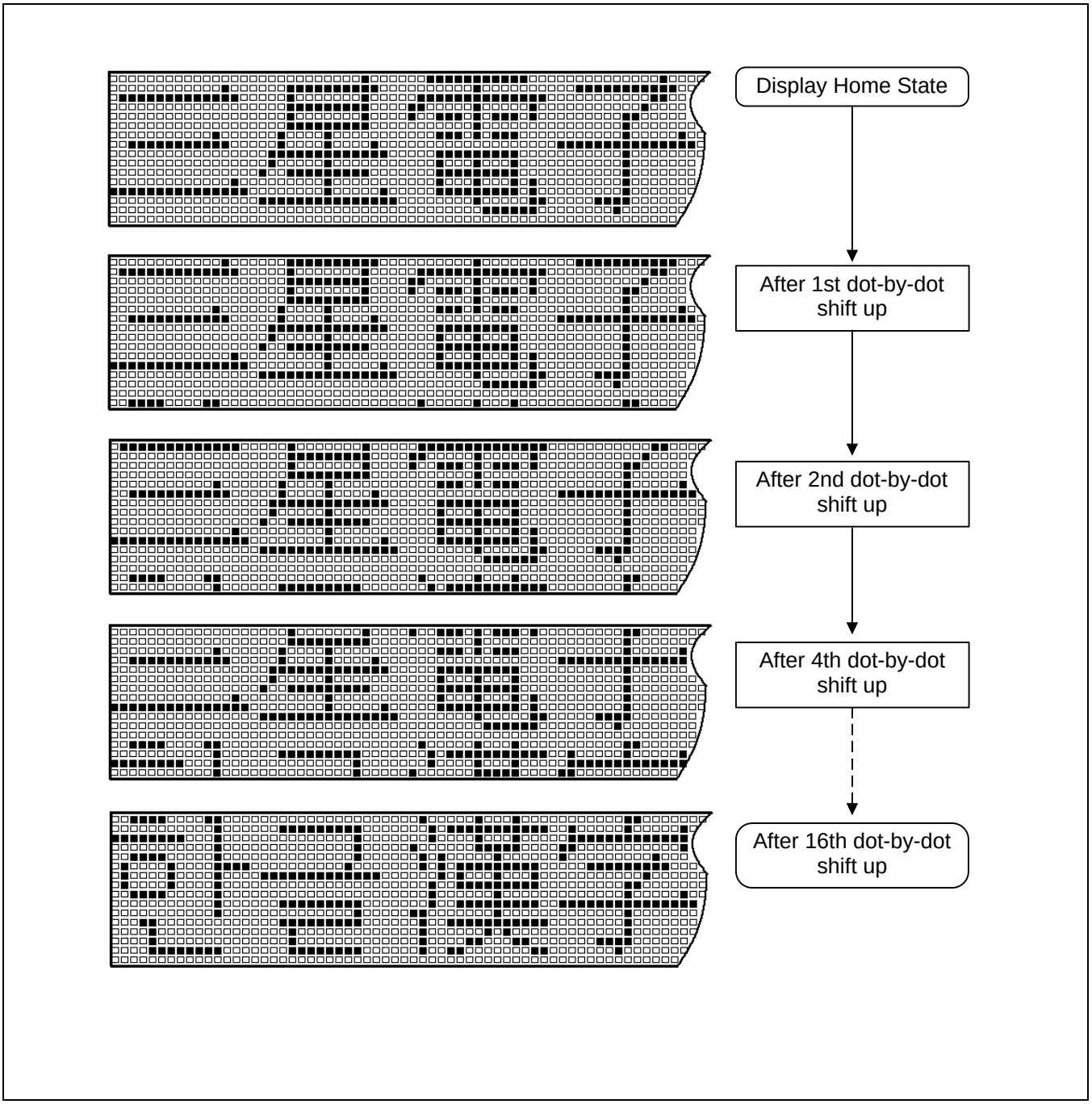



**Figure 12. Vertical Dot-by-Dot Shift Up (Down) Example**

# INSTRUCTION DESCRIPTION

## OUTLINE

To overcome the speed difference between the internal clock of KS0040 and the MPU clock, KS0040 performs its internal operation by storing control information to either IR or DR.
The internal operation is determined according to the signal from MPU, composed of read / write and data bus.

- There are four different types of instructions:
  - — System register set instructions (power control, contrast value set etc.)
  - — Internal RAM access instructions (RAM select, RAM address set, data read / write etc.)
  - — Display control instructions (Vertical shift, double height character etc.)
  - — Others

The address of internal RAM is automatically increased or decreased by 1.

**NOTE:** Every instruction takes one cycle execution time, so to execute the next instruction, a minimum of E cycle time (tc) must be kept.

**Table 10. Instruction Table**

| Instruction | Instruction Code | | | | | | | | | Description | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| NOP | 0 | 0 (hex) | | | | 0 | 0 | 0 | 0 | No operation | |
| Return home | 0 | 1 (hex) | | | | – | – | – | – | Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed | |
| Display control | 0 | 2 (hex) | | | | D | CC | LC | REV | Display (D), character cursor (CC), line cursor (LC), B/W reverse display (REV) on / off control | |
| Power save mode | 0 | 3 (hex) | | | | – | – | – | SLP | Sleep mode (SLP) on/off control | |
| Contrast increment / decrement | 0 | 4 (hex) | | | | – | – | – | CID | Contrast increment (CID=1) or decrement (CID=0) | |
| Vertical shift | 0 | 5 (hex) | | | | – | – | CD | UD | Vertical character (CD=1), dot (CD=0) shift up (UD=1), down (UD=0) | |
| Double height character | 0 | 6 (hex) | | | | – | EN | DH1 | DH0 | Double height character enable (EN) at selected line (DH1, DH0) | |
| RAM select / system register set | 0 | 7 (hex) | | | | R3 | R2 | R1 | R0 | R3 R2 R1 R0 | Selected RAM / Register |
| | | | | | | | | | | 0 0 0 0<br>0 0 0 1<br>1 0 0 0<br>~<br>1 1 1 1 | DDRAM<br>ICONRAM<br>CGRAM Page 0<br>~<br>CGRAM Page 7 |
| | | | | | | | | | | 0 1 0 0<br>0 1 0 1<br>0 1 1 0<br>0 1 1 1 | Power control register<br>Contrast control register<br>Environment control register<br>Function control register |
| RAM address set | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | DD/CG/ICON RAM address setting.<br>One of 3 RAMs is selected by the RAM select instruction. | |
| Write data | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DD/CG/ICON RAM and system register data write. | |
| Read data | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DD/CG/ICON RAM and system register data read. | |

**NOTE:** “-”: don’t care

**Table 11. System Register Values**

| Register Select Bit | | | | Selected System Register | Register Value Map | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R3 | R2 | R1 | R0 | | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 1 | 0 | 0 | Power control register (1) | OSC | VC | VR | VF | INTR | RR2 | RR1 | RR0 |
| 0 | 1 | 0 | 1 | Contrast control register (2) | – | – | C5 | C4 | C3 | C2 | C1 | C0 |
| 0 | 1 | 1 | 0 | Environment control register (3) | – | – | DT1 | DT0 | DIRC | DIRS | EXT | ID |
| 0 | 1 | 1 | 1 | Function control register (4) | – | – | – | FG | CM | FL1 | B1 | B0 |

**NOTES:**

1. OSC: Internal oscillator ON (OSC = 1), OFF (OSC = 0) control bit
   VC: Voltage converter ON (VC = 1), OFF (VF = 1) control bit
   VR: Voltage regulator ON (VR = 1), OFF (VR = 0) control bit
   VF: Voltage follower ON (VF = 1), OFF (VF = 0) control bit
   INTR: Use the internal voltage regulating resisters ON (INTR = 1), OFF (INTR = 0) control bit
   RR2 to RR0: Internal voltage adjusting resisters set control register bits (Refer to Table 17)
2. C5 to C0: Electronic contrast control register bits. (Refer to Figure 21)
3. DT1, DT0: Duty select bits (Refer to Table 15)
   DIRC, DIRS: Common data direction (DIRC), Segment data direction (DIRS) select bit
   (Refer to Table 9 and Table 10)
   EXT: DDRAM extended mode ON (EXT = 1), OFF (EXT = 0) control bit
   ID: DDRAM / CGRAM/ICONRAM address Increment (ID = 1), decrement (ID = 0) control bit
4. FG: CGRAM full graphic mode ON (FG = 1), OFF (FG = 0) control bit
   CM: Center display mode ON (CM = 1), OFF (CM = 0) control bit
   FL1: First line fix mode ON (FL1 = 1), OFF (FL1 = 0) control, during vertical shift
   B1, B0: Cursor attribute control bit

## RETURN HOME

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **1** | **–** | **–** | **–** | **–** |

Set the DDRAM address to “00h” in the address counter. If the display position has shifted, return it to the original position. When cursor or blinking is displayed on, bring the cursor to the left edge on first line of the display. The data in DDRAM does not change.

## DISPLAY CONTROL

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **1** | **0** | **D** | **CC** | **LC** | **REV** |

| **D** | **Display on / off control** |
|---|---|
| H | Display is turned on |
| L | Display is turned off, but display data remains in DDRAM. (default) |

| **CC** | **Character cursor on / off control bit** |
|---|---|
| H | character cursor is turned on |
| L | character cursor disappears in current display. (default) |

| **LC** | **Line cursor on / off control bit** |
|---|---|
| H | line cursor is turned on according to the most significant 2 bits (ADDR[6], ADDR[5]) of the current DDRAM address (ADDR[6:0]) |
| L | line cursor disappears in current display.(default) |

| **REV** | **Black / white reverse display on/off control bit** |
|---|---|
| H | all display areas except the icon area are black/white reversed |
| L | normal display status.(default) |

## POWER SAVE MODE

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **1** | **1** | **–** | **–** | **–** | **SLP** |

Power save mode is used to put KS0040 in sleep mode.

| SLP | Sleep mode on / off control bit |
|---|---|
| H | sleep mode is set.(default) |
| L | sleep mode is reset |

**NOTE:** Refer to “LOW POWER CONSUMPTION MODE” and INITIALIZING & POWER SAVE MODE SETUP”

## CONTRAST INCREMENT / DECREMENT

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **1** | **0** | **0** | **–** | **–** | **–** | **CID** |

Contrast control register value increment/decrement instruction

| CID | Contrast increment / decrement enable bit |
|---|---|
| H | contrast register value increased by 1 until 63 |
| L | contrast register value decreased by 1 until 0 |

## VERTICAL SHIFT UP / DOWN (SEE FIGURE 14)

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **1** | **0** | **1** | **–** | **–** | **CD** | **UD** |

Vertical dot-by-dot display shift up / down instruction.

| CD | Character / Dot shift select bit |
|---|---|
| H | display shift up / down by character is selected. It is the same as 16-times dot shift. |
| L | display shift up / down by dot is selected. |

| UD | Vertical display shift direction select |
|---|---|
| H | display shift up is performed |
| L | display shift down is performed |

## DOUBLE HEIGHT CHARACTER (SEE FIGURE 15)

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **1** | **1** | **0** | **–** | **EN** | **DH1** | **DH0** |

Double height character instruction.

| **EN** | **Double height character mode enable bit** |
|---|---|
| H | double height character mode is enabled |
| L | double height character mode is disabled.(default) |

| **DH1** | **DH0** | **Double height character line select** |
|---|---|---|
| L | L | 1, 2 line become double height |
| L | H | 2, 3 line become double height |
| H | L | 3, 4 line become double height |
| H | H | 1 line to 4 line become double height |

## RAM SELECT/SYSTEM REGISTER SET

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **1** | **1** | **1** | **R3** | **R2** | **R1** | **R0** |

RAM select (DDRAM / CGRAM/ICONRAM) or system register set instruction.
R3 / R2 / R1 / R0: RAM or system register select bits

| Select bits | | | | Selected RAM or Registers | Data Length / Value Map | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **R3** | **R2** | **R1** | **R0** | | **DB7** | **DB6** | **DB5** | **DB4** | **DB3** | **DB2** | **DB1** | **DB0** |
| 0 | 0 | 0 | 0 | DDRAM | 1-byte (half-size font) 2-byte (full-size font) | | | | | | | |
| 0 | 0 | 0 | 1 | ICONRAM | 1-byte | | | | | | | |
| 1 | 0 | 0 | 0 | CGRAM Page0 | 2-byte | | | | | | | |
| 1 | 0 | 0 | 1 | CGRAM Page1 | 2-byte | | | | | | | |
| 1 | 0 | 1 | 0 | CGRAM Page2 | 2-byte | | | | | | | |
| 1 | 0 | 1 | 1 | CGRAM Page3 | 2-byte | | | | | | | |
| 1 | 1 | 0 | 0 | CGRAM Page4 | 2-byte | | | | | | | |
| 1 | 1 | 0 | 1 | CGRAM Page5 | 2-byte | | | | | | | |
| 1 | 1 | 1 | 0 | CGRAM Page6 | 2-byte | | | | | | | |
| 1 | 1 | 1 | 1 | CGRAM Page7 | 2-byte | | | | | | | |
| 0 | 1 | 0 | 0 | Power control register | OSC | VC | VR | VF | INTR | RR2 | RR1 | RR0 |
| 0 | 1 | 0 | 1 | Contrast control register | – | – | C5 | C4 | C3 | C2 | C1 | C0 |
| 0 | 1 | 1 | 0 | Environment control register | – | – | DT1 | DT0 | DIRC | DIRS | EXT | ID |
| 0 | 1 | 1 | 1 | Function control register | – | – | – | FG | CM | FL1 | B1 | B0 |

**NOTE:** For writing 2-byte data into RAM, data write instruction must be performed twice.

**OSC** Oscillator circuit on (OSC = “high”), off (OSC = “low”: default) control.

**VC/VR/VF** Voltage converter / regulator / follower circuit on (VC / VR/VF = “high”), on (VC / VR/VF = “low”: default) control.

**INTR** Use the internal voltage regulating resistors on (INTR = “high”), off (INTR = “low”: default) control bit.

**RR2 to RR0** Internal voltage adjusting resistors set control register bits ([0, 0, 0]: default). (Refer to Table 17.)

**C5 to C0** Electronic contrast control register ([0, 0, 0, 0, 0, 0]: default). (Refer to Figure 21.)

**DT1, DT0** Duty select register ([1,1]: default). (Refer to Table 15.)

**DIRC, DIRS** Common data shift direction (DIRC) and Segment data shift direction (DIRS) flag register ([0, 0]: default). (Refer to Table 9. and Table 10.)

**EXT** DDRAM extended mode on (EXT = “high”), off (EXT = “low”: default) control.

**ID** RAM address Increment (ID = “high”: default), Decrement (ID = “low”) mode set.

**FG** CGRAM full graphic mode on / off control register (FG = “low”: default). (Refer to Figure 16.)

**CM** Center display mode on / off control register (CM= “low”: default). (Refer to Figure 15.)

**FL1** First line fix mode, during vertical scroll instruction, on/off control register (FL1 = “low”: default). (Refer to Figure 14.)

**B1, B0** Character/Line cursor attribute select register ([0,0]: default) (Refer to Table 14.)

## RAM ADDRESS SET

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **0** | **1** | **AC6** | **AC5** | **AC4** | **AC3** | **AC2** | **AC1** | **AC0** |

DDRAM / CGRAM / ICONRAM address set instruction.
Each RAM is selected by RAM select instruction.

## WRITE DATA

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **1** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |

DDRAM / CGRAM/ICONRAM data or system register value write instruction. Each RAM and system register is selected by RAM select / system register set instruction. After write operation, the address is increased/decreased by 1 automatically, according to the function control register set.
When writing a full-size character address to DDRAM, RAM data write instruction must be written twice, because the FCGROM address is 13-bits long.

## READ DATA (8-BIT BUS MODE MPU INTERFACE ONLY) (SEE FIGURE 13)

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| **1** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |

DDRAM / CGRAM/ICONRAM data or system register value read instruction.
Each RAM and system register is selected by RAM select / system register set instruction.
If you read RAM data after RAM address set instruction, you can get the correct RAM data from the second. The first data would be incorrect, because there is no timing margin for transferring RAM data to the output register.
After write or read operation, the address is increased/decreased by 1 automatically, according to the function control register set.
When reading a full size character address from DDRAM, RAM data read instruction must be executed twice, because the FCGROM address is 13-bits long. (Refer to Figure 13.)

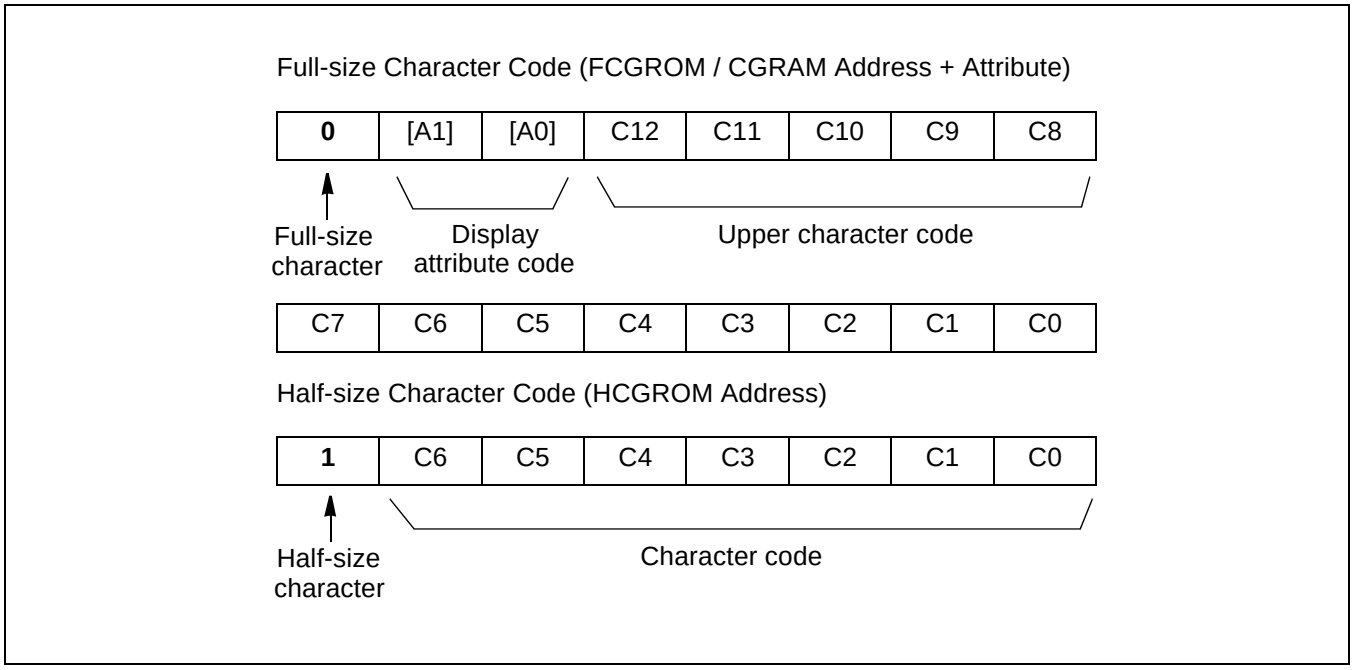



**Figure 13. DDRAM Data (FCGROM / HCGROM / CGRAM Address) Format**

**Table 12. Display Attributes**

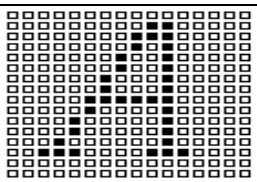
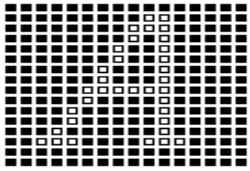
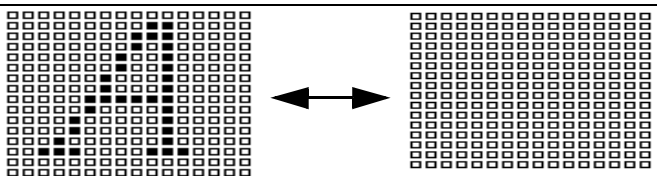
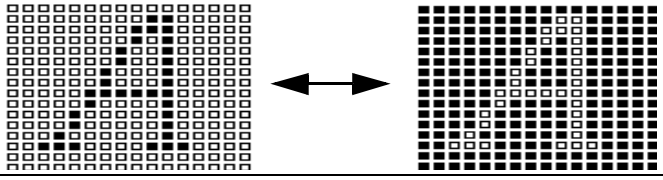
| [A1] | [A0] | Display State (When Cursor/Blink Off) | |
|---|---|---|---|
| 0 | 0 | Normal display |  |
| 0 | 1 | B/W reverse display |  |
| 1 | 0 | Character blink mode 1 |  |
| 1 | 1 | Character blink mode 2 |  |

**Table 13. Cursor Attributes**

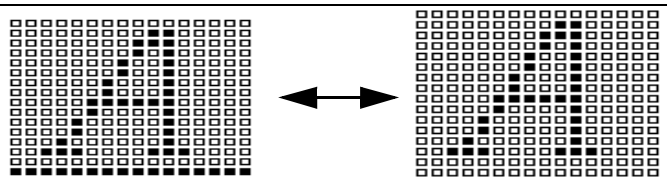
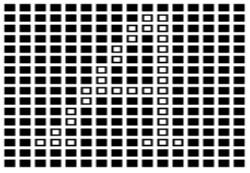
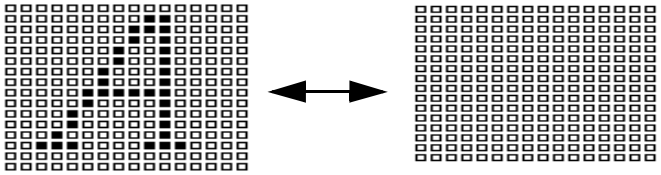
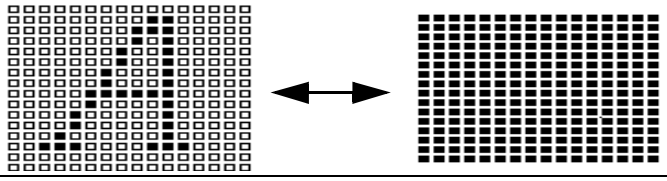
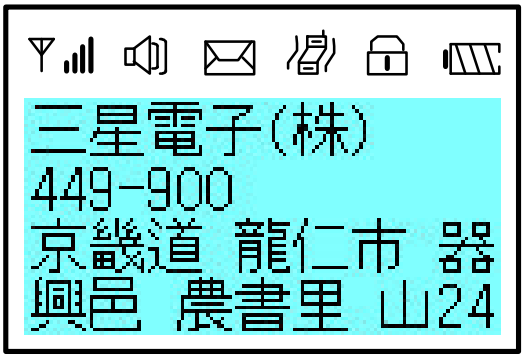
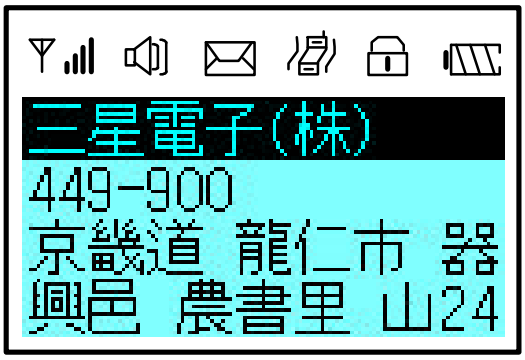
| B1 | B0 | Display State (at cursor position) | |
|---|---|---|---|
| 0 | 0 | Underline cursor |  |
| 0 | 1 | B/W reverse cursor |  |
| 1 | 0 | Blink cursor 1 |  |
| 1 | 1 | Blink cursor 2 |  |

**Table 14. The Relationship Between Duty and Environment set**

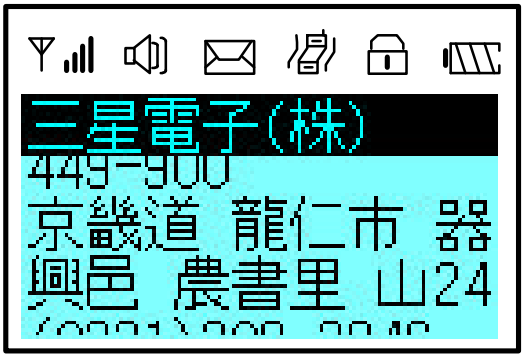
| DT1 | DT0 | Duty | Bias | fosc (kHz) | Display Line Number |
|---|---|---|---|---|---|
| 0 | 0 | 1/17 | 1/5 | 24.5 | 1-line display |
| 0 | 1 | 1/33 | 1/7 | 47.6 | 2-line display |
| 1 | 0 | 1/49 | 1/8 | 68.3 | 3-line display |
| 1 | 1 | 1/65 | 1/9 | 93.7 | 4-line display |



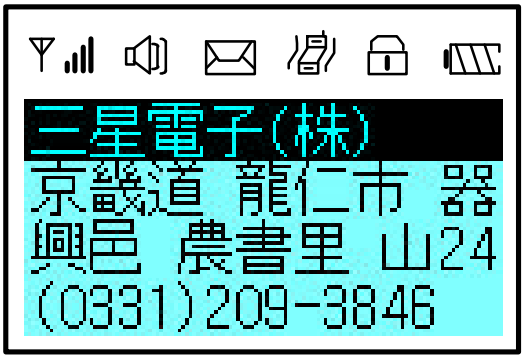

Normal Display
- Line Cursor(LC) Off
- First Line Fix Mode(FL1) Off
- Vertical Shift Off




Normal Display & Line Cursor
- Line Cursor(LC) On (B1,B0= [0, 1])
- First Line Fix Mode(FL1) Off
- Vertical Shift Off

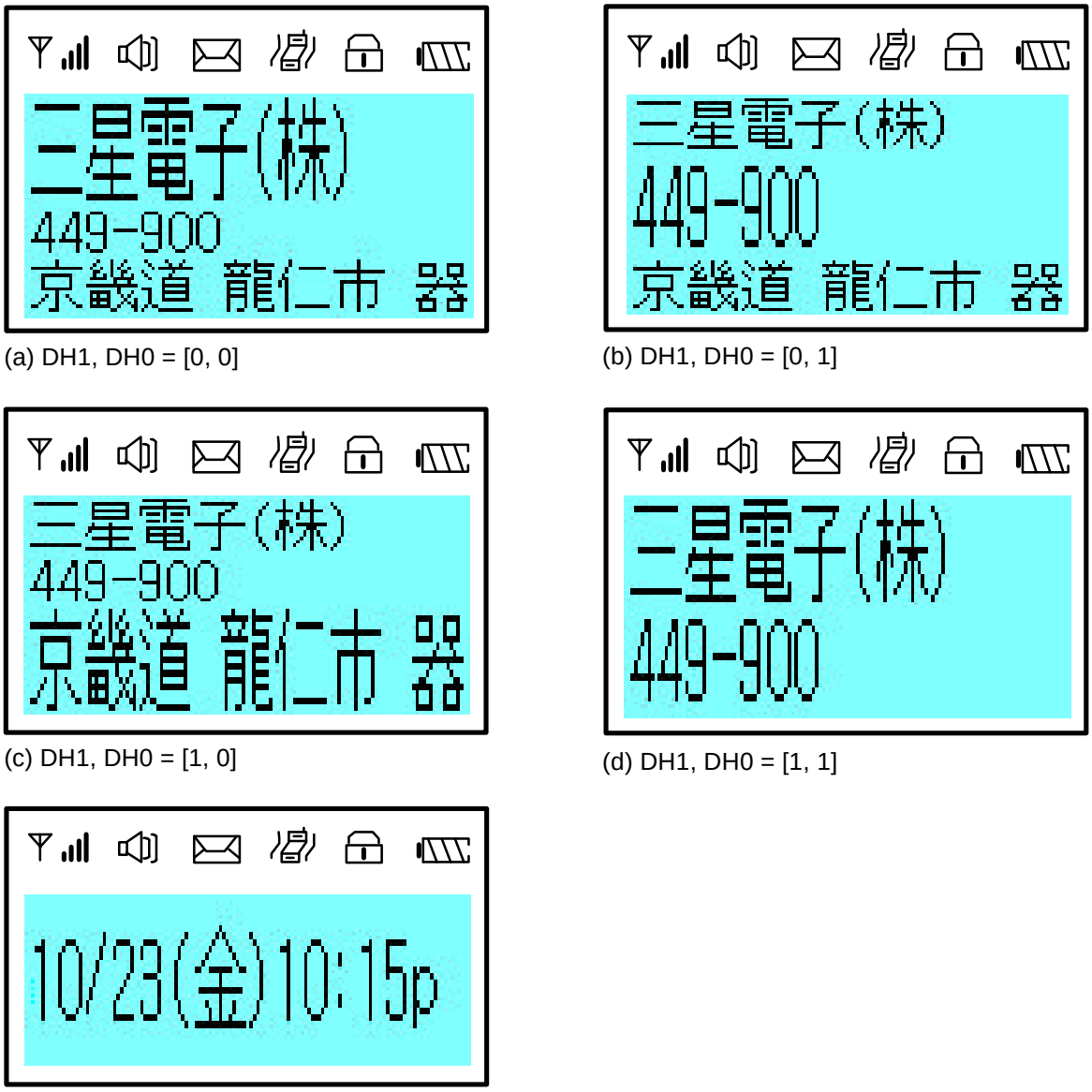



Vertical Shifted Display
(in First Line Fix Mode )
- Line Cursor(LC) On (B1,B0=[0, 1])
- First Line Fix Mode(FL1) On
- Vertical Shift Up by Dot 6-times




Vertical Shifted Display
(in First Line Fix Mode )
- Line Cursor(LC) On (B1,B0=[0, 1])
- First Line Fix Mode(FL1) On
- Vertical Shift Up by Dot 16-times or Vertical Shift Up by Character once

**Figure 14. The Examples of Vertical Shift and First Line Fix Mode**




(a) DH1, DH0 = [0, 0]

(b) DH1, DH0 = [0, 1]

(c) DH1, DH0 = [1, 0]

(d) DH1, DH0 = [1, 1]

(e) DH1, DH0 = [0, 0] and Center Mode On (CM = 1), when 3-line display

**Figure 15. The Examples of Double Height Character Display**

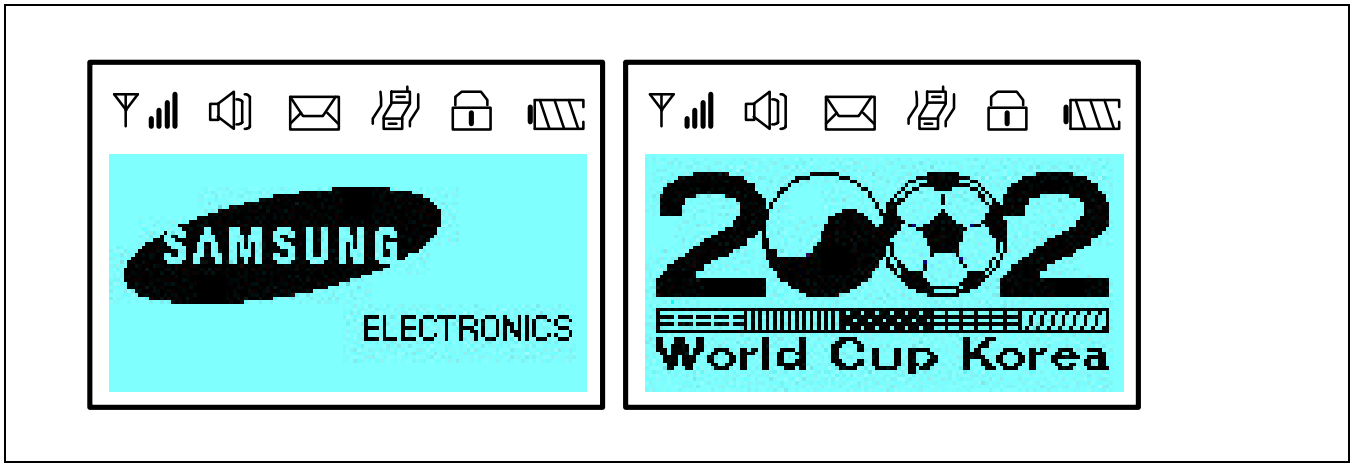



**Figure 16. The Examples of Full Graphic Mode Display (FG = 1)**

## INITIALIZING & POWER SAVE MODE SETUP

### HARDWARE RESET

When RESET pin = “Active (rising or falling)”, KS0040 can be initialized in the following state.

**Return home**
Address counter = 00H

**Control display ON / OFF instruction**

| | | |
|---|---|---|
| D | 0 | Display OFF |
| CC/LC | [0, 0] | Character / Line cursor OFF |
| REV | 0 | Reverse display OFF (Normal display) |

**Power save mode instruction**

| | | |
|---|---|---|
| SLP | 1 | Sleep mode ON |

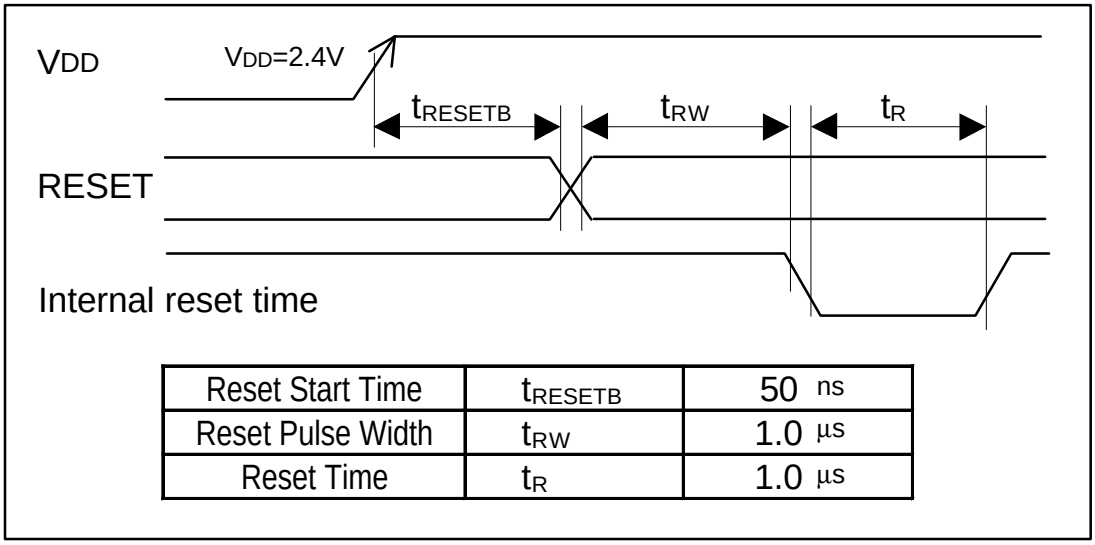
**RAM select instruction**

| | | |
|---|---|---|
| R3–R0 | [0, 0, 0, 0] | DDRAM is selected |

**System register set instruction**

| | | |
|---|---|---|
| OSC | 0 | Oscillator OFF |
| VC, VR, VF | [0, 0, 0] | Voltage converter / regulator / follower / OFF |
| INTR | 0 | Internal voltage regulating register OFF |
| RR2–RR0 | [0, 0, 0] | Internal voltage adjusting resistors set control register values are set to 000 |
| C5–C0 | [0, 0, 0, 0, 0] | Electronic contrast control register values are set to 00H |
| DT1, DT0 | [1, 1] | 4-Line display mode |
| DIRC | 0 | Normal direction of common outputs<br>(COM1 to COM64, COMI1 (COMI2)) |
| DIRS | 0 | Normal direction of segment outputs<br>(SEGI1, SEGI2, SEG1 to SEG128, SEGI3, SEGI4) |
| EXT | 0 | Normal DDRAM mode is selected |
| ID | 1 | RAM address increment condition |
| FG | 0 | CGRAM full graphic mode OFF |
| CM | 0 | Center display mode OFF |
| FL1 | 0 | First line fix mode OFF |
| B1, B0 | [0, 0] | Underline cursor attribute is selected |

**NOTE:** If initialization is not done by the RESET pin, an unstable condition might result. So, the RESET input pin must be active first for initialization.

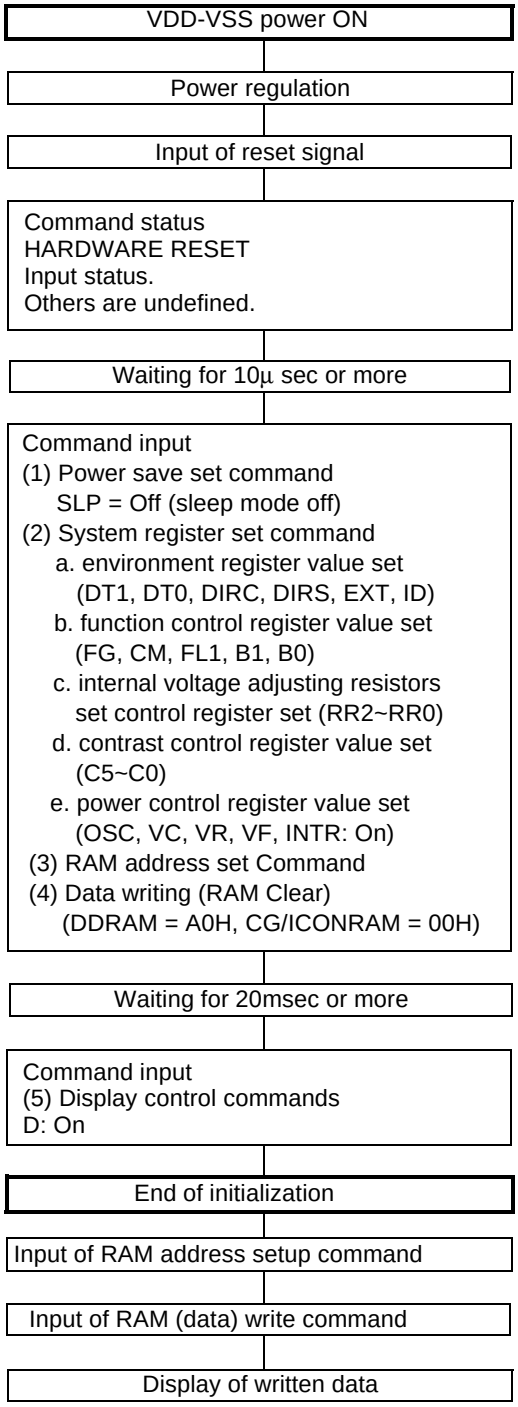



| | | |
|---|---|---|
| Reset Start Time | $t_{RESETB}$ | 50 ns |
| Reset Pulse Width | $t_{RW}$ | 1.0 µs |
| Reset Time | $t_R$ | 1.0 µs |

**NOTE:** $t_{RW}$ indicates the minimum RESET duration for activate internal reset signal.
$t_R$ indicates reset completion time of the internal circuit from the edge of the internal reset signal.

# INITIALIZING AND POWER SAVE SETUP

## INITIALIZING BY INSTRUCTION



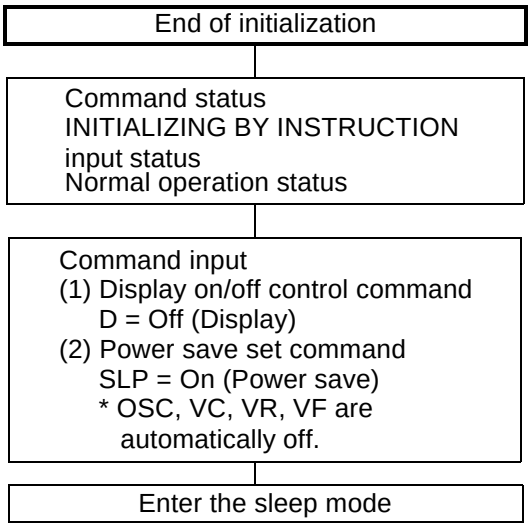

**NOTE:** Commands (3) and (4) initialize the RAM.
The non-display area must satisfy the following conditions (for RAM clear).

DDRAM: Write the A0H data. (Half character flag 1 and space character code 20H: 1 0100000)
CGRAM: Write the 00H data. (blank data)
ICONRAM: Write the 00H data. (off data)

As the RAM data is unstable during reset signal input (after power on), blank data must be written.
If not, unexpected display may result.

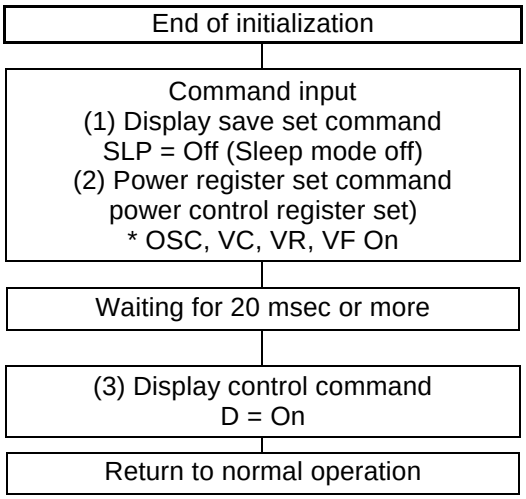
## SLEEP MODE SET OR RELEASE BY INSTRUCTION

(a) Sleep mode setting




**NOTE:**
Internal voltage regulating resistor control bit (INTR) and voltage adjusting resistors set control register bits (RR2 to RR0) are not changed in sleep mode.

(b) Sleep mode releasing



## LCD DRIVING POWER SUPPLY CIRCUIT

This power supply circuit generates the voltage to drive the LCD, and it consists of the following: voltage converter, voltage regulator, and voltage follower. The voltage converter boosts up the logic voltage ($V_{DD}$) 2, 3, 4 times and this boosted voltage (VOUT) is delivered to the voltage regulator. Voltage regulator adjusts V0 between VOUT and $V_{SS}$ and this adjusted voltage is sent to the voltage follower.
$V_{LCD}$ voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and the output impedances are converted by the voltage follower to increase drive capability.
Power supply circuit is controlled by the power control instruction.
There can be up to eight combination states according to the instruction sets (VC,VR,VF). Table 16. shows useful combinations which are recommended. The remaining combination states are impractical, and are not recommended for use.

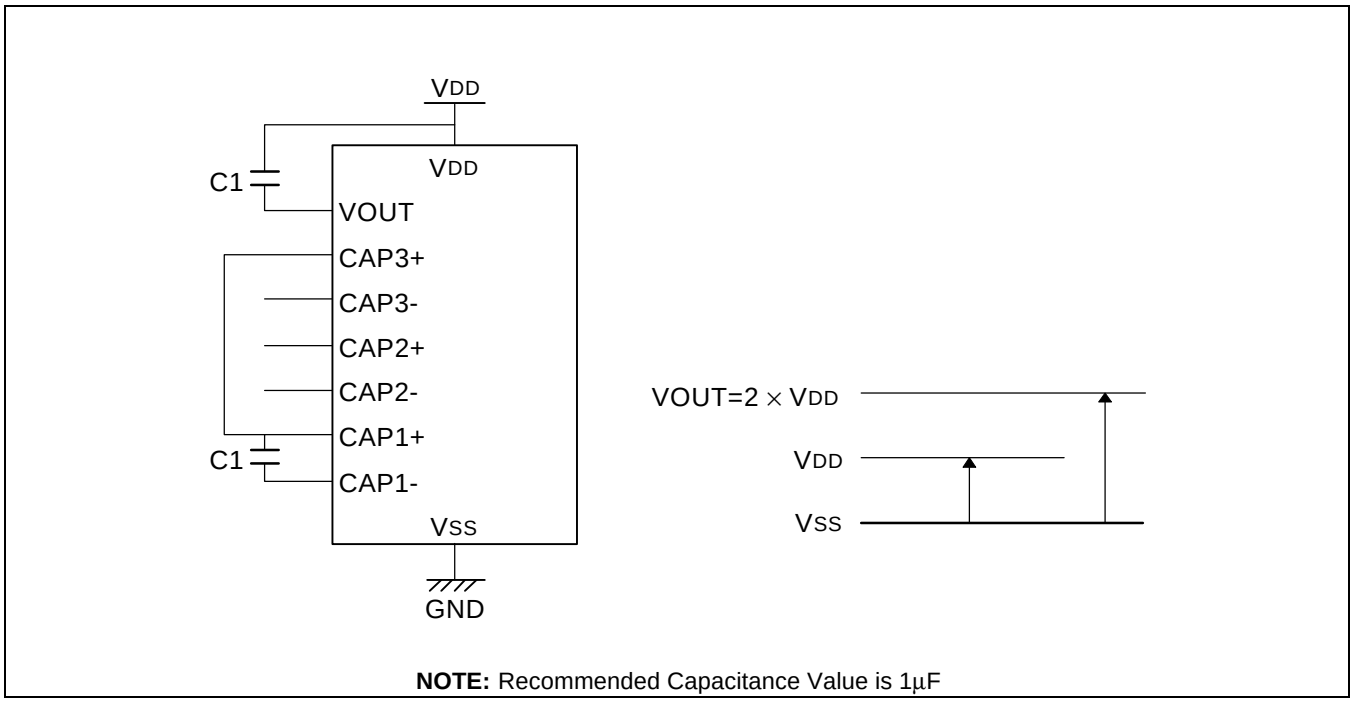
**Table 15. Recommended Power Supply Combination**

| VC | VR | VF | Voltage Converter | Voltage Regulator | Voltage Follower | VOUT | VO, VR | V1, V2, V3, V4 |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | Enable | Enable | Enable | Internal voltage output | Used for voltage adjustment | Internal voltage output |
| 0 | 1 | 1 | Disable | Enable | Enable | External voltage input | Used for voltage adjustment | Internal voltage output |
| 0 | 0 | 1 | Disable | Disable | Enable | Open | VO: External voltage input<br>VR: open | Internal voltage output |
| 0 | 0 | 0 | Disable | Disable | Disable | Open | VO: External voltage input<br>VR: open | External voltage input |

**NOTE:** Any other combination which is not written in this table is prohibited.

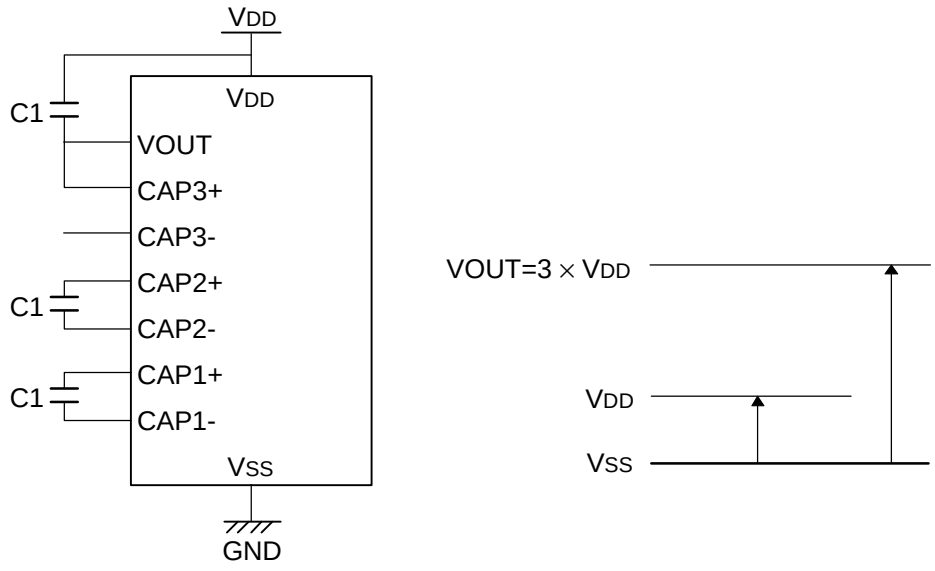
## VOLTAGE CONVERTER

This circuit boosts up the electric potential between $V_{DD}$ and $V_{SS}$ to 2, 3, or 4 times toward the positive side, and the boosted voltage comes out through the VOUT terminal.



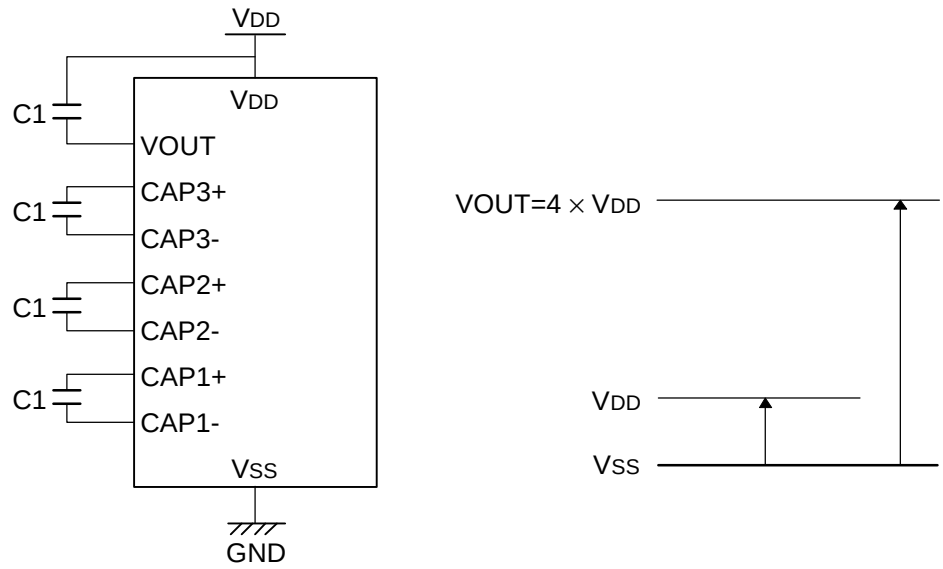

**NOTE:** Recommended Capacitance Value is 1μF

**Figure 17. Two Times Boosting**




**NOTE:** Recommended Capacitance Value is 1µF

**Figure 18. Three Times Boosting**




**NOTE:** Recommended capacitance value is 1µF

**Figure 19. Four Times Boosting**

## VOLTAGE REGULATOR

The boosting voltage generated at VOUT is sent to the voltage regulator. The voltage regulator determines the V0 LCD driver voltage by adjusting resistor Ra and Rb within the range of [V0] < |VOUT|. This V0 is determined by equation (1), where Ra and Rb are internal or external resistors and VREF is determined by equation (2) as the voltage source of the IC.
The electric potential of VREF is set to one of 64 levels by setting the 6-bit reference voltage register.

**<Equation 1>**

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \; [V]$$

**<Equation 2>**

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{300}\right) \times V_S \; [V]$$

Where $\alpha$ = value of 6-bit reference voltage register (0 to 63)

When REF = “high”, $V_S = V_{DD}$
REF = “low”, $V_S = V_{REF}$ (Internal reference voltage) = 2V

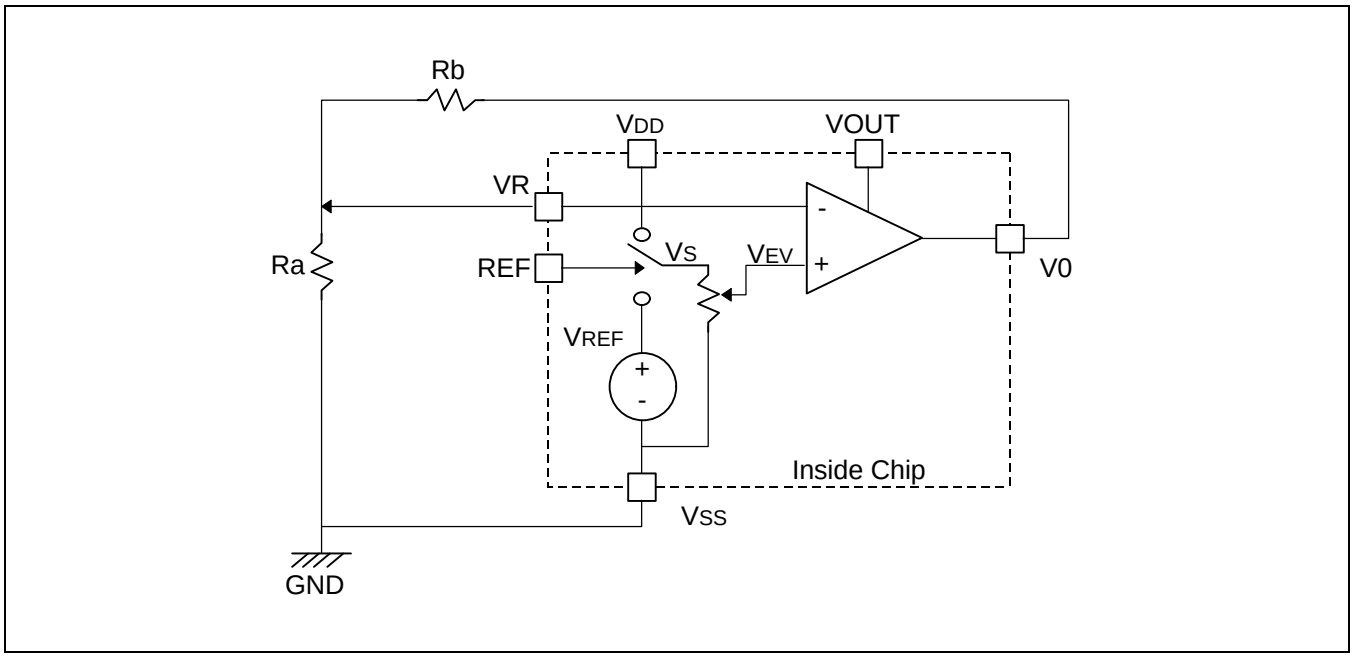



**Figure 20. Voltage Regulator Circuit**

### When Using Internal Resistors, Ra and Rb (INTR = "high")

When INTR bit is set to "high", built-in regulator resistor Ra is connected between VR and $V_{SS}$, and Rb is connected between V0 and VR. V0 voltage is determined by changing the ratio of Rb/Ra and reference voltage $V_{REF}$. The ratio of Rb / Ra is set to one of 8 ratios by selecting the regulator resistor with the 3-bit instruction register (RR2, RR1 and RR0).

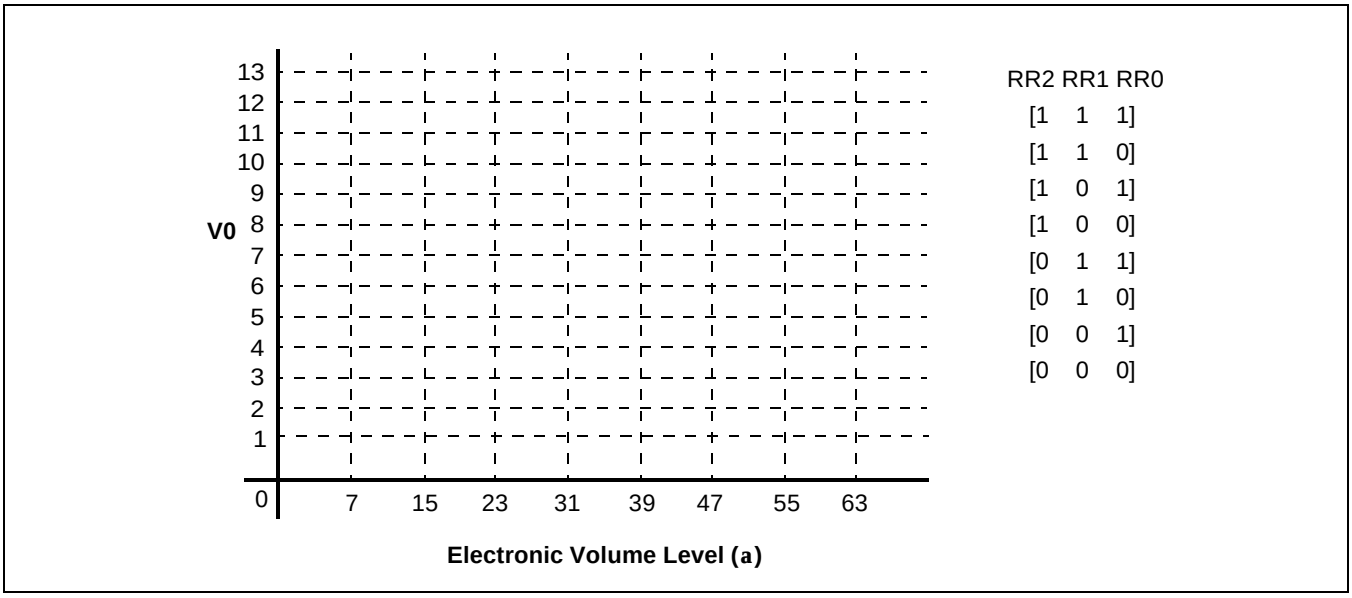



**Figure 21. V0 Voltages According to RR2 to RR0 (Ta = 25°C)**

**Table 16. The Relationship Between Electronic Volume Constant, a, and 6-bit Voltage Reference Register (C5, C4, C3, C2, C1, C0)**

| C5 | C4 | C3 | C2 | C1 | C0 | a |
|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| : | : | : | : | : | : | : |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 17. The Change Ratio of $V_{REF}$ and V0**

(RR2, RR1, RR0 = [0, 0, 0], Ta = 25°C)

| | a | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | **0** | **1** | **....** | **30** | **31** | **32** | **....** | **62** | **63** |
| V0 | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD |

**When Using External Resistors, Ra and Rb. (INTR = "low")**

When INTR pin is set to low, it is necessary to connect the external regulator resistor Ra between VR and Vss, and Rb between V0 and VR.

- Example: For the following requirements
  - — 1. LCD driver voltage, V0 = 10V
  - — 2. 6-bit reference voltage register = (1, 1, 1, 1, 1, 1)
  - — 3. Maximum current flowing Ra, Rb = 1μA

**From equation (1)**

$$V0 = 10\,[V] = \left(1 + \frac{Rb}{Ra}\right) \times V_{REF} \quad \ldots\ldots\ldots\ldots (4)$$

**From equation (2)**

$$V_{REF} = \left(1 - \frac{0}{300}\right) \times V_S = V_S = 2V \text{ or } V_{DD} \quad \ldots\ldots\ldots\ldots (5)$$

(Where $\alpha = 63$
$Vs = 2V$ or $V_{DD}$)

**From requirement (3)**

$$\frac{10}{Ra + Rb} = 1\,[\mu A] \ldots\ldots\ldots\ldots\ldots (6)$$

From equation (4), (5) and (6)

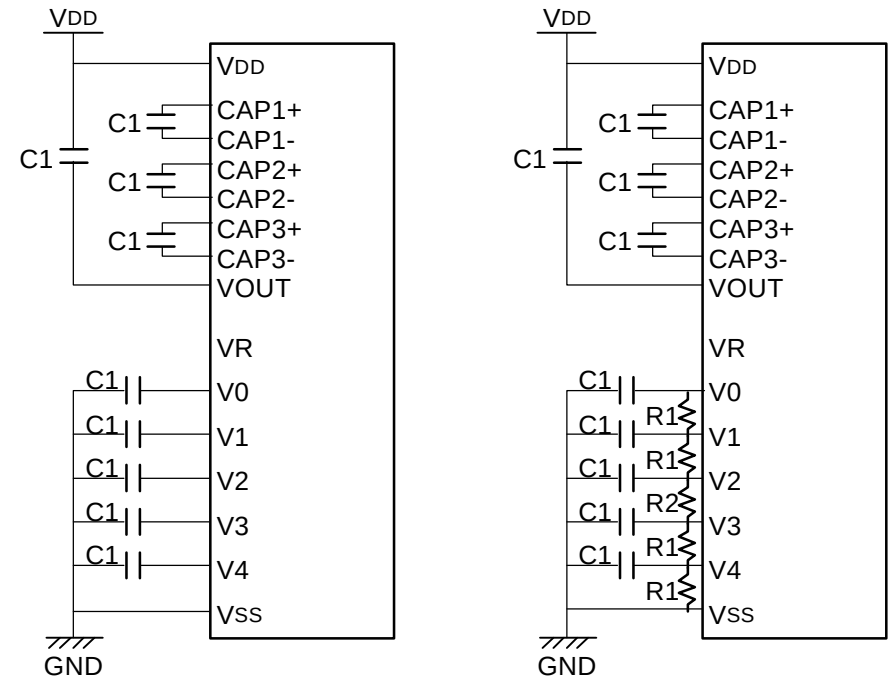
A. When $V_S$ = 2V (REF = "Low")

- — Ra = 2 [MΩ]
- — Rb = 8 [MΩ]

B. When $V_S$ = VDD = 3V (REF = "High")

- — Ra = 3 [MΩ]
- — Rb = 7 [MΩ]

## LCD BIAS RESISTOR & FOLLOWER




a) When use the internal bias circuit
( VC, VR, VF, INTR = [1,1,1,1] )

b) When use the external bias circuit
( VC, VR, VF, INTR = [1,1,0,1] )

* Recommended Capacitance value is 1μF

**Figure 22. LCD Bias Circuit**

**Table 18. Duty Select Input & Internal Bias Circuit**

| DT1 | DT0 | Duty | Internal Bias |
|---|---|---|---|
| Low | Low | 1/17 | 1/5 |
| Low | High | 1/33 | 1/7 |
| High | Low | 1/49 | 1/8 |
| High | High | 1/65 | 1/9 |

## USING THE EXTERNAL POWER SUPPLY

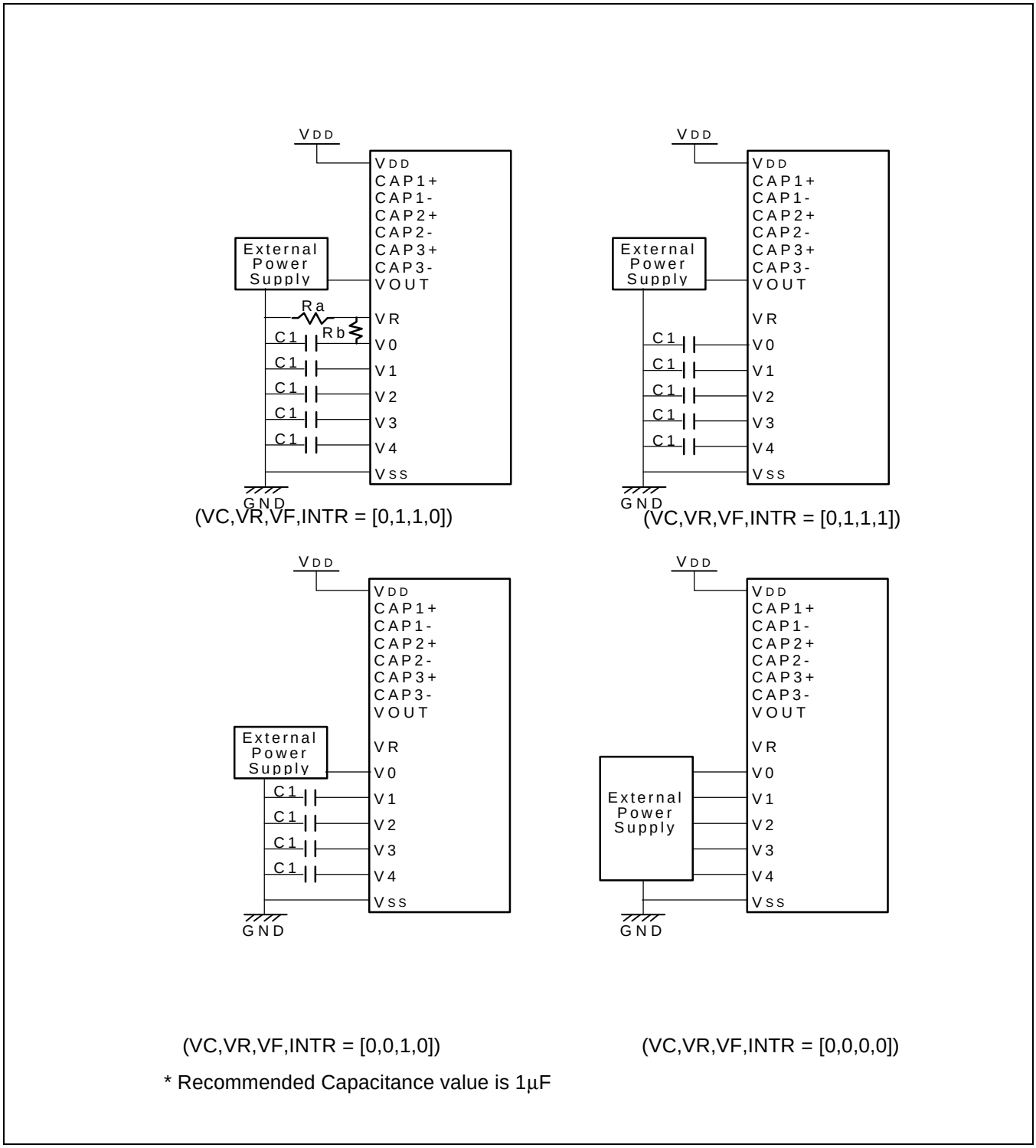
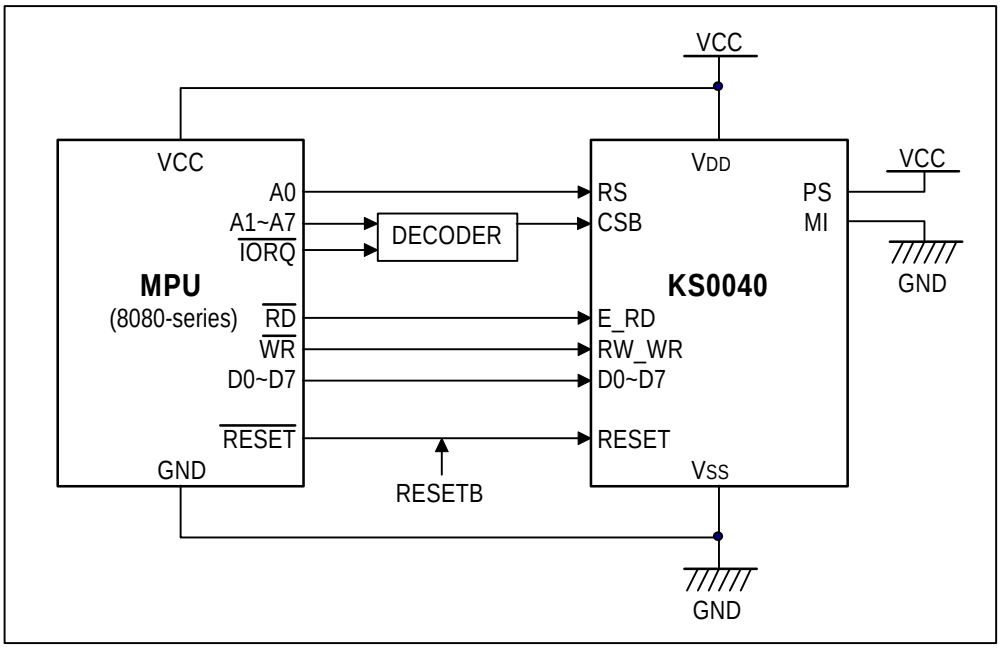



**Figure 23. When External Power Supply is Used**

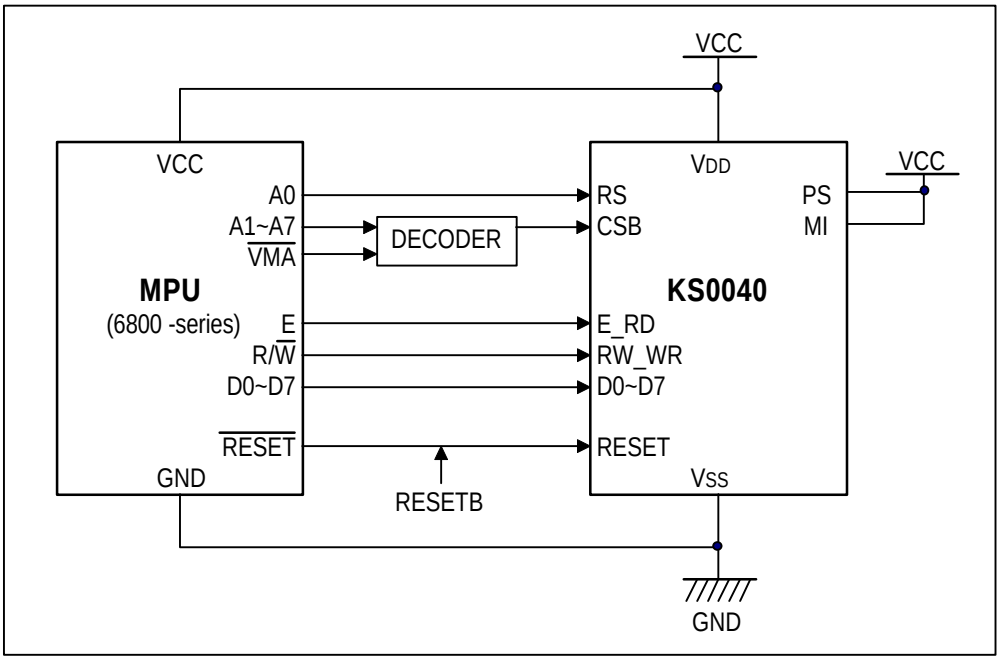
# APPLICATION INFORMATION

## MPU INTERFACE METHOD

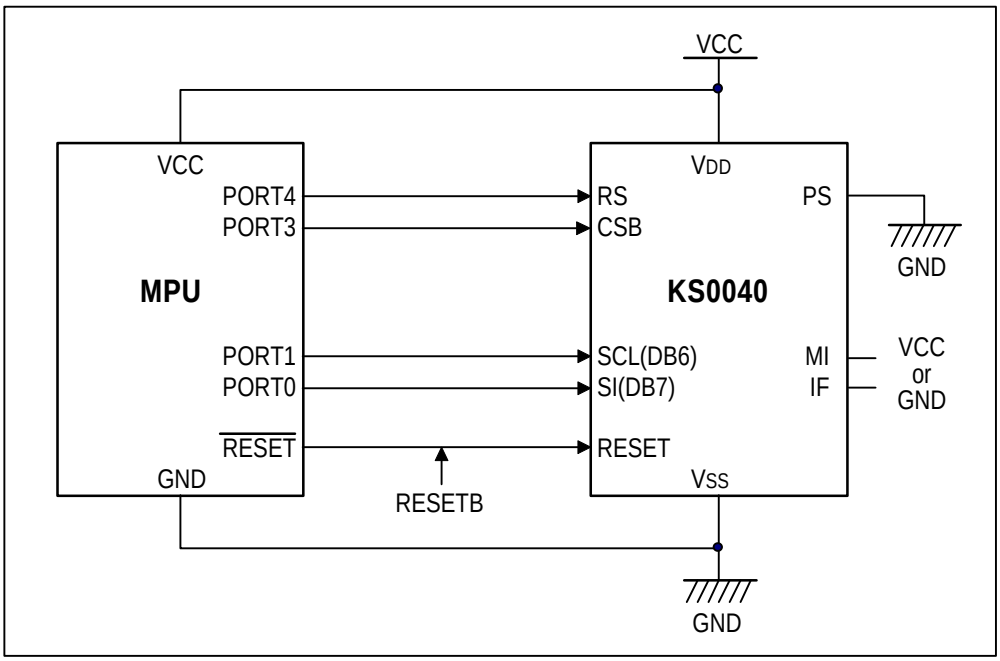
### Parallel interfacing with 8080-series microprocessors




### Parallel interfacing with 6800-series microprocessors



**Clock Synchronized Serial Interfacing with any Microprocessor**



## LCD PANEL CONNECTION METHOD (1/65 DUTY CONFIGURATION)

### Chip Bottom & Lower View (DIRS = 0, DIRC = 0)

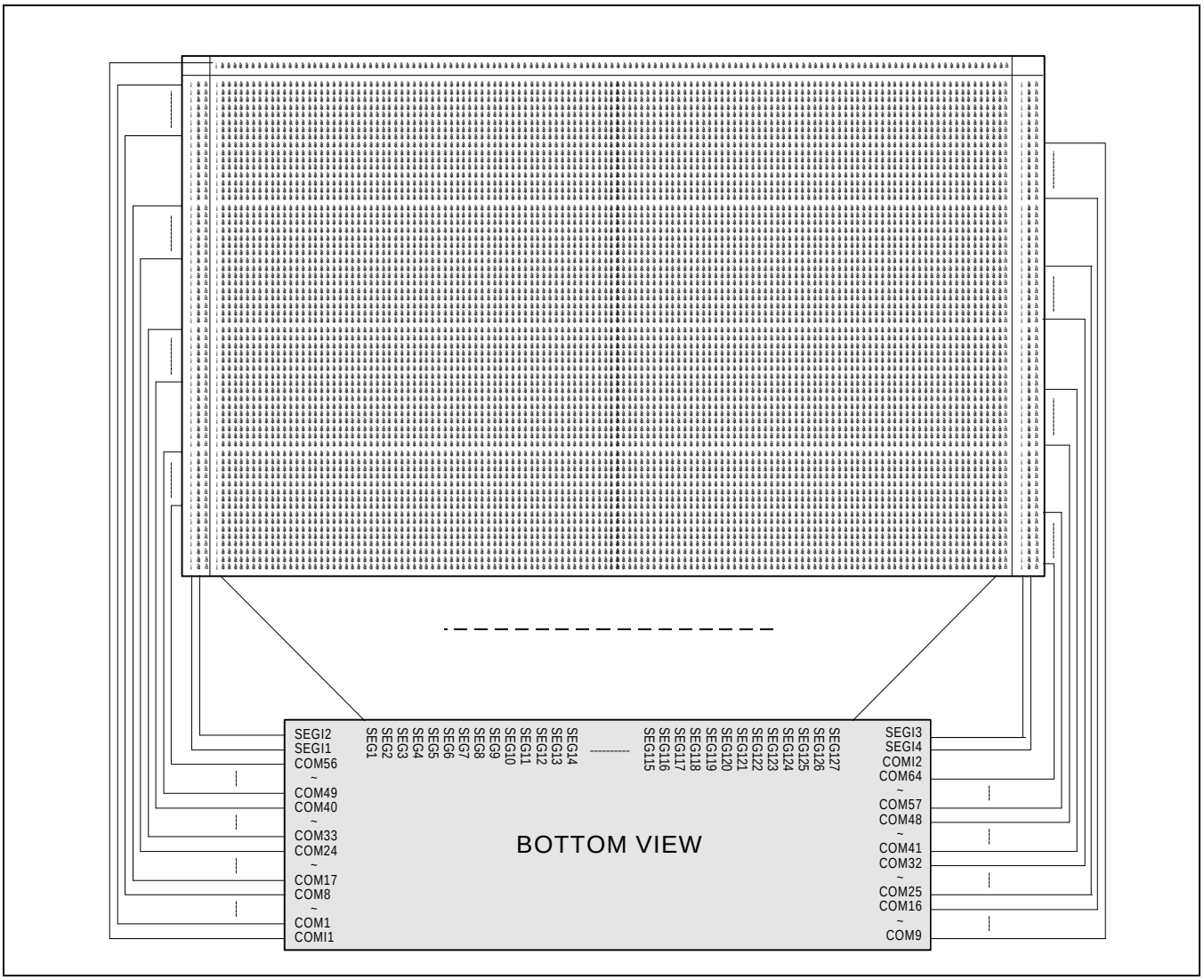



**Figure 24. Chip Bottom & Lower View (DIRS = 0, DIRC = 0)**

**Chip Bottom & Upper View (DIRS = 1, DIRC = 1)**

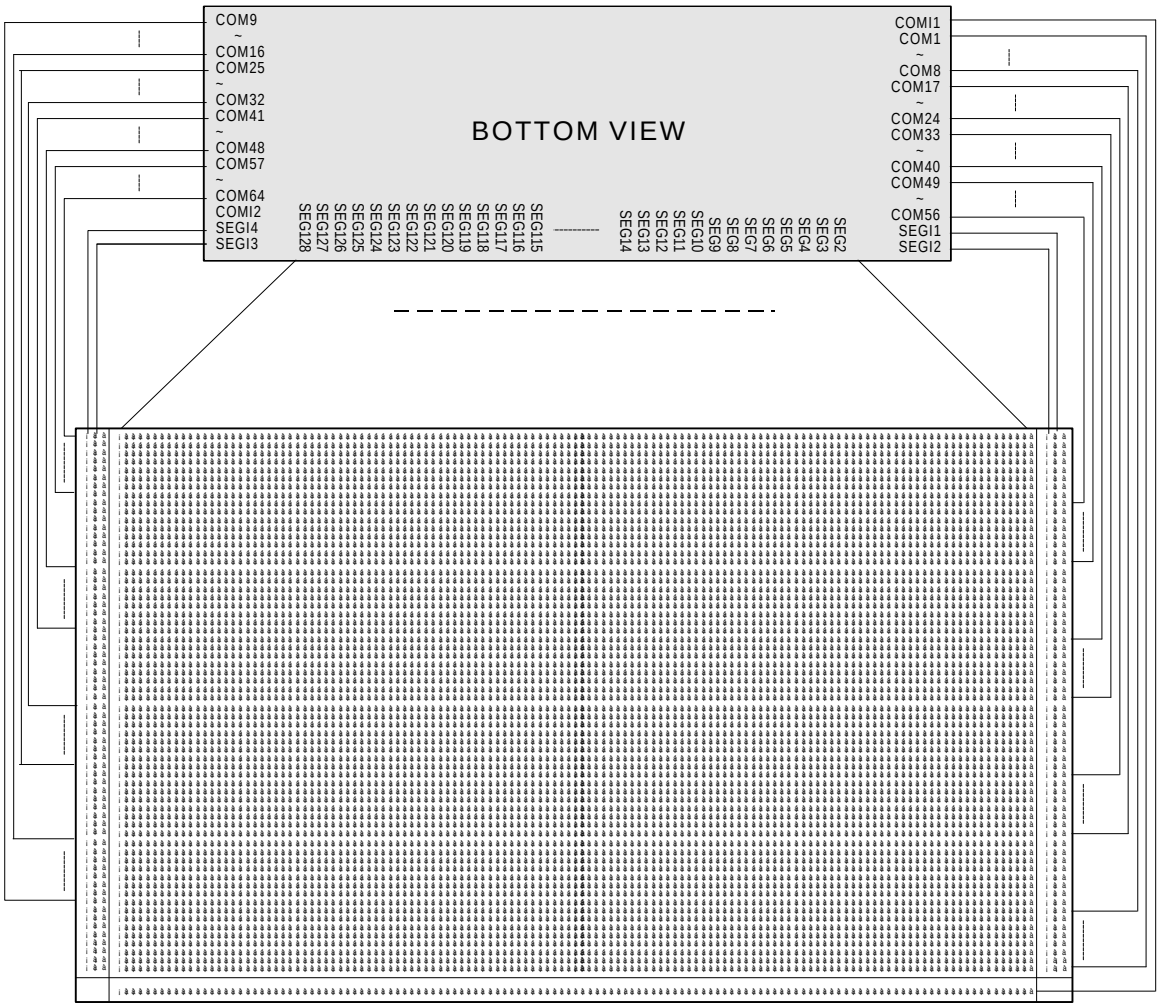



**Figure 25. Chip Bottom & Upper View (DIRS = 1, DIRC = 1)**

**Chip Top & Lower View (DIRS = 1, DIRC = 0)**

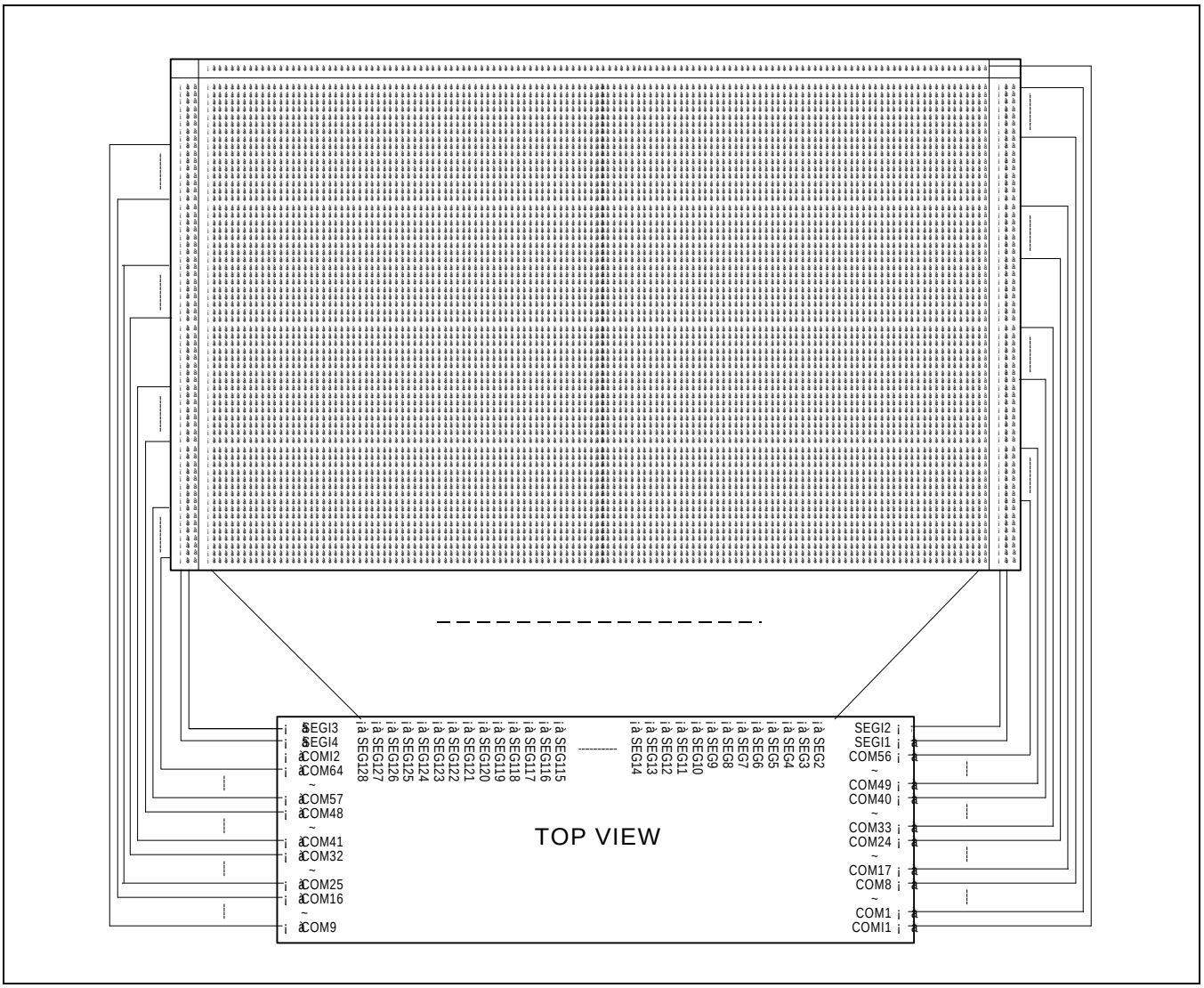



**Figure 26. Chip Top & Lower View (DIRS = 1, DIRC = 0)**

**Chip Top & Upper View (DIRS = 0, DIRC = 1)**

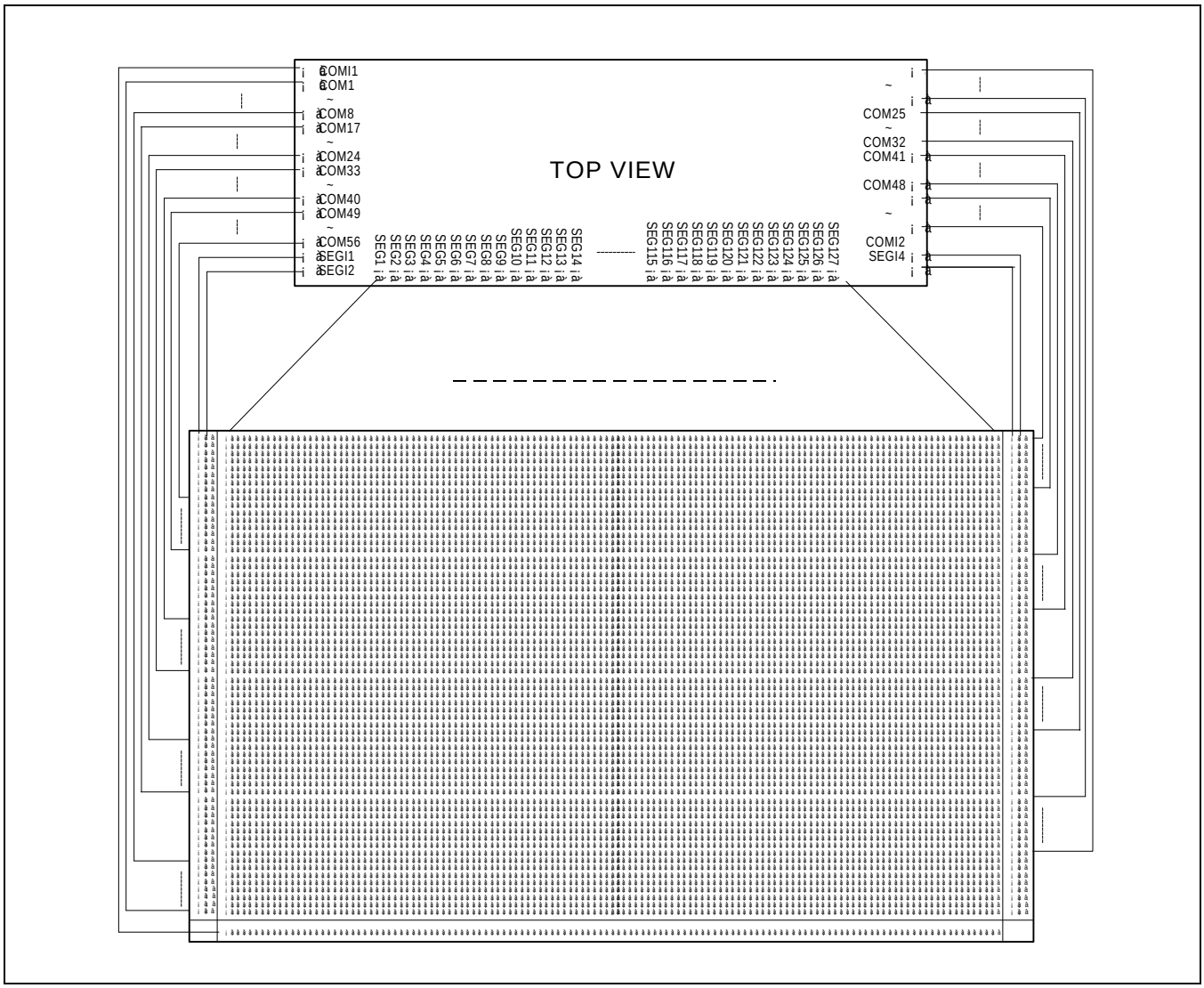
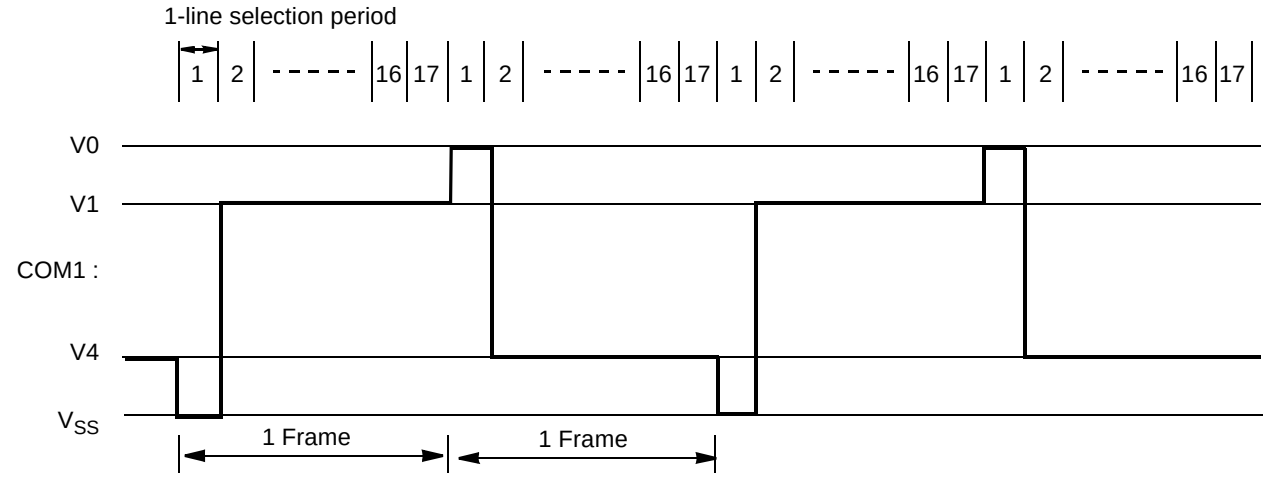



**Figure 27. Chip Top & Upper View (DIRS = 0, DIRC = 1)**

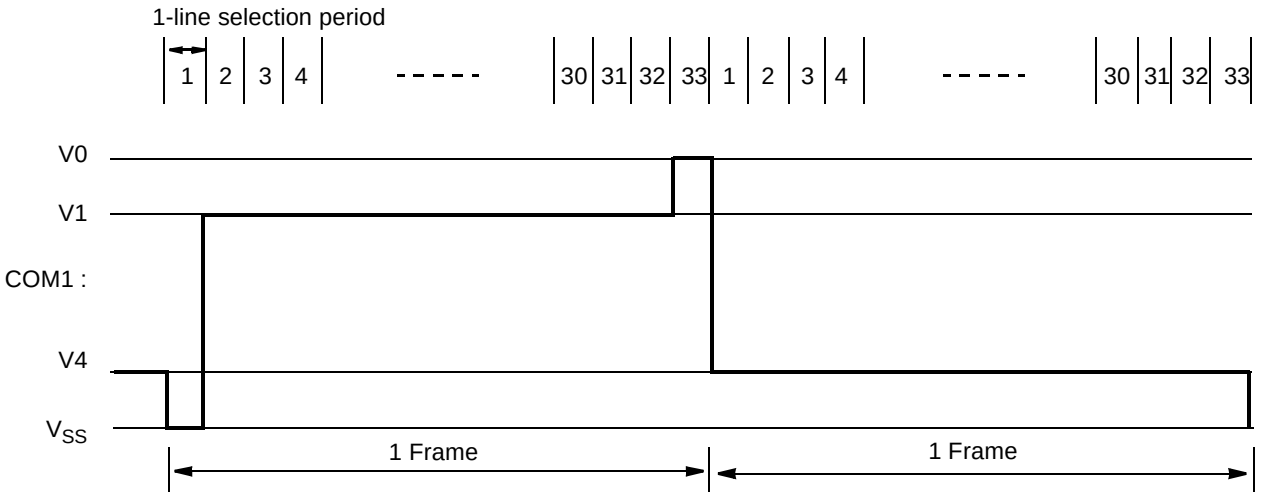
## FRAME FREQUENCY

### 1/17 DUTY (DT1, DT0 = [0, 0])



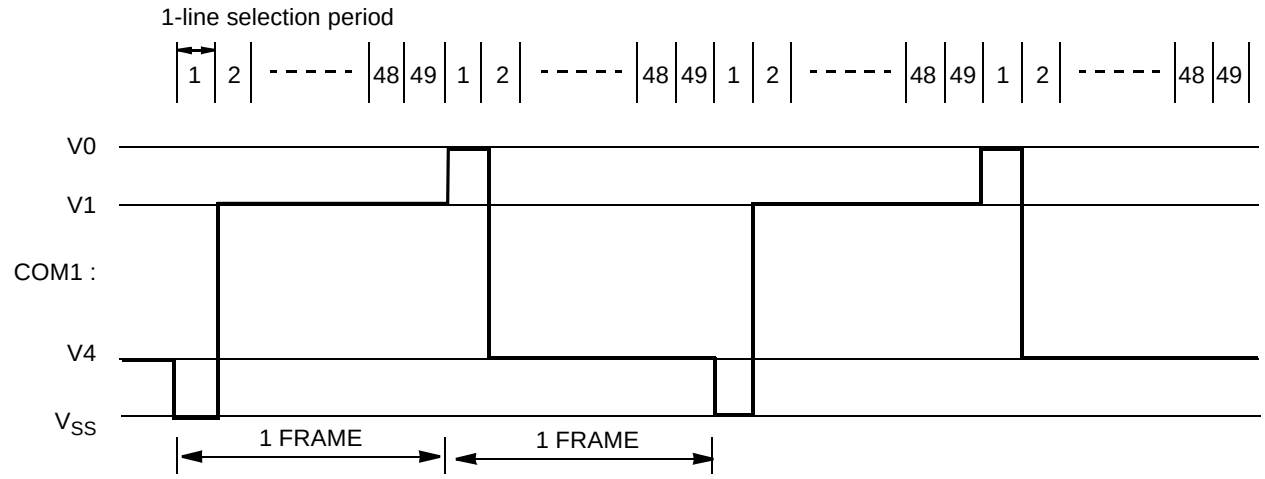

1-line selection period = 17 clock pulses
One Frame = 17 × 17 × 40.8μs = 11.8ms (1 clock = 40.8μs at fosc = 24.5kHz)
Frame frequency = 1/11.8ms = 85Hz

### 1/33 DUTY (DT1, DT0 = [0, 1])



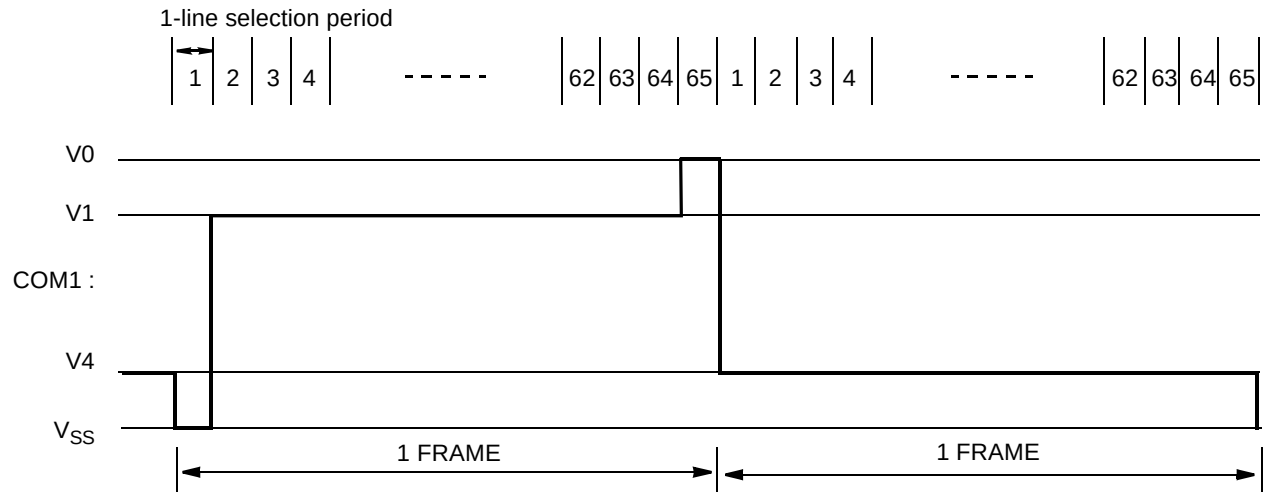

1-line selection period = 17 clock pulses
One Frame = 17 × 33 × 21.0μs = 11.8ms (1 clock = 21.0μs at fosc = 47.6kHz)
Frame frequency = 1/11.8ms = 85Hz

**1/49 DUTY (DT1, DT0 = [1, 0]**




1-Line selection period = 17 clock pulses
One Frame = 17 × 49 × 14.2µs = 11.8ms (1 clock = 14.2µs at fosc = 68.3kHz)
Frame frequency = 1/11.8ms = 85Hz

**1/65 DUTY (DT1, DT0 = [1, 1])**




1-Line selection period = 17clock pulses
One Frame = 17 × 65 × 10.7µs = 11.8ms (1clock = 10.7µs at fosc = 93.7kHz)
Frame frequency = 1/11.8 ms = 85Hz

**Table 19. Duty Select Input & Display Window Size**

| DT1 | DT0 | Duty | Display Window Size |
|---|---|---|---|
| Low | Low | 1/17 | 1-line × 8-character |
| Low | High | 1/33 | 2-line × 8-character |
| High | Low | 1/49 | 3-line × 8-character |
| High | High | 1/65 | 4-line × 8-character |

## ABSOLUTE MAXIMUM RATINGS

**Table 20. Absolute Maximum Ratings**

| Characteristics | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage (1) | $V_{DD}$ | – 0.3 to + 7.0 | V |
| Power supply voltage (2) | V0, VOUT | – 0.3 to + 15 | V |
| Input voltage | $V_{IN}$ | – 0.3 to $V_{DD}$ + 0.3 | V |
| Operating temperature | $T_{OPR}$ | – 30 to + 85 | °C |
| Storage temperature | $T_{STG}$ | – 55 to + 125 | °C |

**NOTES:**

1. All the voltage levels are based on $V_{SS}$ = 0 V
2. Voltage greater than above may damage the circuit
   Voltage level: VOUT ≥ V0 ≥ $V_{SS}$ ($V_{LCD}$ = V0 – $V_{SS}$)
   Voltage level: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ $V_{SS}$

# ELECTRICAL CHARACTERISTICS

## DC CHARACTERISTICS

**Table 21. DC Characteristics**

($V_{DD}$ = 2.4V to 3.6V, Ta = – 30 to + 85°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating voltage | $V_{DD}$ | – | 2.4 | – | 3.6 | V |
| Supply current ($V_{DD}$ = 3V, Ta = 25°C) | $I_{DD1}$ | Display operation<br>V0 = 9V without load<br>No access from MPU | – | – | 150 | µA |
| | $I_{DD2}$ | Sleep operation without load<br>oscillator OFF | – | – | 5 | |
| | $I_{DD3}$ | Access operation from MPU<br>fcyc = 200kHz | – | – | 500 | |
| Input voltage | $V_{IH}$ | – | $0.8V_{DD}$ | – | VDD | V |
| | $V_{IL}$ | – | $V_{SS}$ | – | 0.2 VDD | |
| Input leakage current | $I_{LEAK}$ | $V_{IN}$ = 0V to $V_{DD}$ | – 1 | – | 1 | µA |
| $R_{ON}$ resistance | $R_{COM}$ | $I_O$ = ± 50µA | – | – | 5 | KΩ |
| | $R_{SEG}$ | $I_O$ = ± 50µA | – | – | 10 | |
| Frame frequency | $f_{FR}$ | $V_{DD}$ = 3V, Ta = 25°C | 60 | 85 | 110 | Hz |
| External clock frequency | $f_{CK}$ | Display of 1 line mode | – | 24.5 | – | kHz |
| | | Display of 2 line mode | – | 47.6 | – | |
| | | Display of 3 line mode | – | 68.3 | – | |
| | | Display of 4 line mode | – | 93.7 | – | |
| Voltage converter VDD 2/3/4 times | $V_{OUT}$ | Ta = 25°C, C = 1µF<br>Without load | 95 | 99 | – | % |
| Voltage regulator reference voltage | $V_{REF}$ | Ta = 25°C | 1.94 | 2.0 | 2.06 | V |
| LCD driving voltage | $V_{LCD}$ | $V_{LCD}$ = V0 – $V_{SS}$ | 4.0 | – | 13.0 | |

**Table 22. DC Characteristics**

($V_{DD}$ = 3.6V to 5.5V, Ta = – 30 to + 85°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating voltage | $V_{DD}$ | – | 3.6 | – | 5.5 | V |
| Supply current ($V_{DD}$ = 5V, Ta = 25°C) | $I_{DD1}$ | Display operation V0 = 9V without load No access from MPU | – | – | 250 | µA |
| | $I_{DD2}$ | Sleep operation without load oscillator OFF | – | – | 10 | |
| | $I_{DD3}$ | Access operation from MPU fcyc = 200kHz | – | – | 1000 | |
| Input voltage | $V_{IH}$ | – | $0.8V_{DD}$ | – | VDD | V |
| | $V_{IL}$ | – | $V_{SS}$ | – | 0.2VDD | |
| Input leakage current | $I_{LEAK}$ | $V_{IN}$ = 0 V to $V_{DD}$ | – 1 | – | 1 | µA |
| $R_{ON}$ resistance | $R_{COM}$ | $I_O$ = ± 50µA | – | – | 5 | KΩ |
| | $R_{SEG}$ | $I_O$ = ± 50µA | – | – | 10 | |
| Frame frequency | $f_{FR}$ | $V_{DD}$ = 3V, Ta = 25°C | 60 | 85 | 110 | Hz |
| External clock frequency | $f_{CK}$ | Display of 1 line mode | – | 24.5 | – | kHz |
| | | Display of 2 line mode | – | 47.6 | – | |
| | | Display of 3 line mode | – | 68.3 | – | |
| | | Display of 4 line mode | – | 93.7 | – | |
| (NOTE) Voltage converter VDD 2/3 times | $V_{OUT}$ | Ta = 25°C, C = 1µF Without load | 95 | 99 | – | % |
| Voltage regulator reference voltage | $V_{REF}$ | Ta = 25°C | 1.94 | 2.0 | 2.06 | V |
| LCD driving voltage | $V_{LCD}$ | $V_{LCD}$ = V0 – $V_{SS}$ | 4.0 | - | 13.0 | |

**NOTE:** When power supply ($V_{DD}$) range is 3.6V to 5.5V, 4 times boosting is not allowed.

## AC CHARACTERISTICS

### Parallel Interface Mode

6800-series MPU interface & write instruction

($V_{DD}$ = 2.4V to 3.6V, Ta = – 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Write bus mode (6800-series MPU interface) | E cycle time | $t_C$ | 650 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | E pulse width high | $t_{WH}$ | 450 | – | – | |
| | E pulse width low | $t_{WL}$ | 150 | – | – | |
| | RS and CSB setup time | $t_{SU1}$ | 60 | – | – | |
| | RS and CSB hold time | $t_{H1}$ | 30 | – | – | |
| | DB setup time | $t_{SU2}$ | 100 | – | – | |
| | DB hold time | $t_{H2}$ | 50 | – | – | |

($V_{DD}$ = 3.6V to 5.5V, Ta = – 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Write bus mode (6800-series MPU interface) | E cycle time | $t_C$ | 350 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | E pulse width high | $t_{WH}$ | 250 | – | – | |
| | E pulse width low | $t_{WL}$ | 100 | – | – | |
| | RS and CSB setup time | $t_{SU1}$ | 40 | – | – | |
| | RS and CSB hold time | $t_{H1}$ | 10 | – | – | |
| | DB setup time | $t_{SU2}$ | 40 | – | – | |
| | DB hold time | $t_{H2}$ | 10 | – | – | |

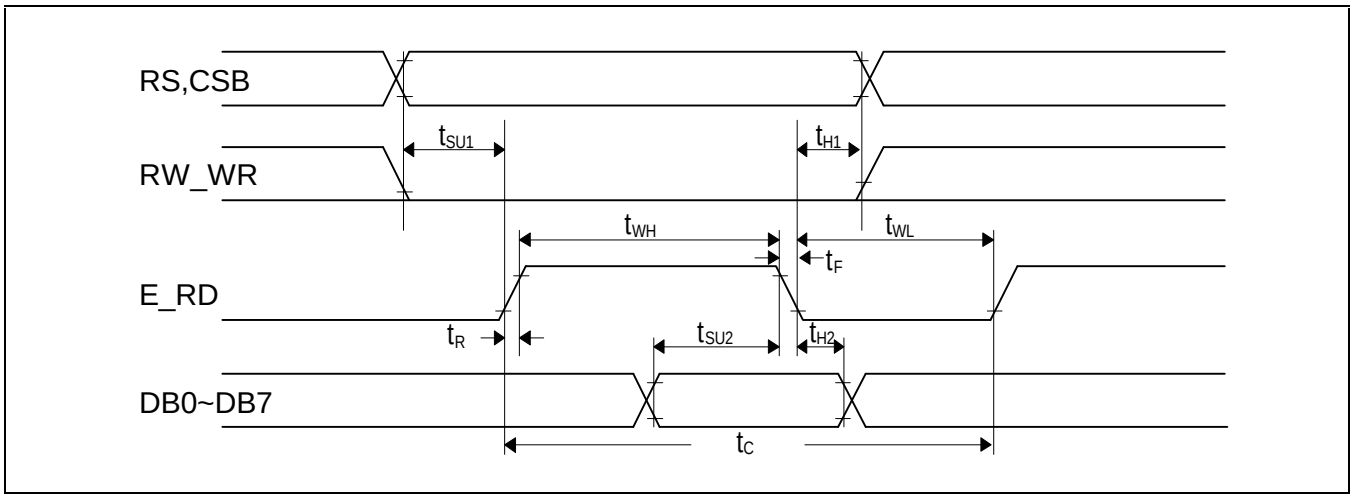



**Figure 28. Write Bus Mode Timing (6800-series MPU Interface)**

8080-series MPU Interface & Write Instruction

($V_{DD}$ = 2.4V to 3.6V, Ta = – 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Write bus mode (8080-series MPU interface) | WR cycle time | $t_C$ | 650 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | WR pulse width high | $t_{WH}$ | 150 | – | – | |
| | WR pulse width low | $t_{WL}$ | 450 | – | – | |
| | RS and CSB setup time | $t_{SU1}$ | 60 | – | – | |
| | RS and CSB hold time | $t_{H1}$ | 30 | – | – | |
| | DB setup time | $t_{SU2}$ | 100 | – | – | |
| | DB hold time | $t_{H2}$ | 50 | – | – | |

($V_{DD}$ = 3.6V to 5.5V, Ta = – 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Write bus mode (8080-series MPU interface) | WR cycle time | $t_C$ | 350 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | WR pulse width high | $t_{WH}$ | 100 | – | – | |
| | WR pulse width low | $t_{WL}$ | 250 | – | – | |
| | RS and CSB setup time | $t_{SU1}$ | 40 | – | – | |
| | RS and CSB hold time | $t_{H1}$ | 10 | – | – | |
| | DB setup time | $t_{SU2}$ | 40 | – | – | |
| | DB hold time | $t_{H2}$ | 10 | – | – | |

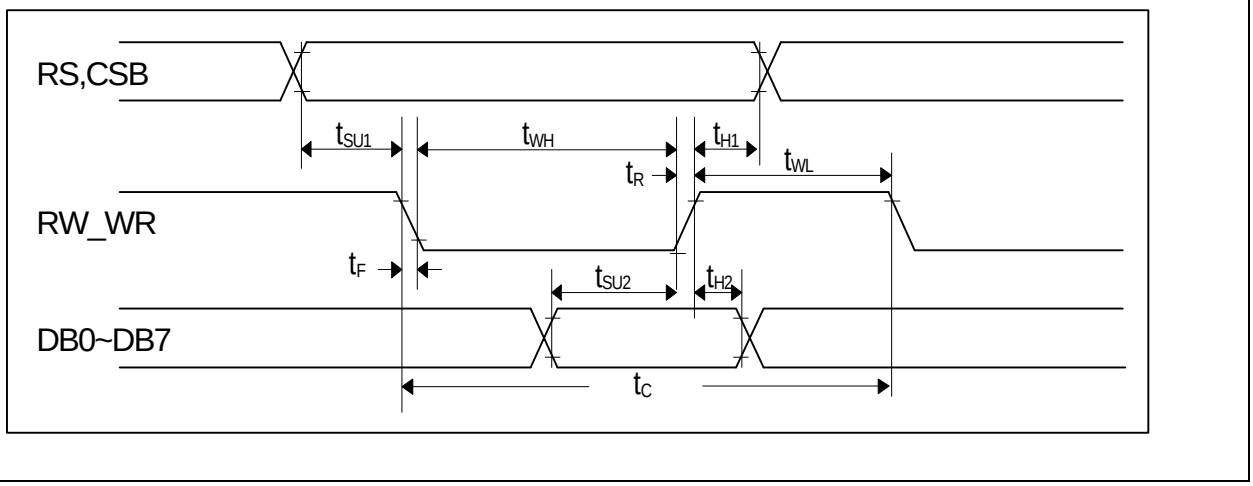



**Figure 29. Write Bus Mode Timing (8080-series MPU Interface)**

6800-Series MPU Interface & Read Instruction

($V_{DD}$ = 2.4V to 3.6V, Ta = - 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Read bus mode (6800-series MPU interface) | E cycle time | $t_C$ | 650 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | E pulse width high | $t_{WH}$ | 450 | – | – | |
| | E pulse width low | $t_{WL}$ | 150 | – | – | |
| | RS and CSB setup time | $t_{SU}$ | 60 | – | – | |
| | RS and CSB hold time | $t_H$ | 30 | – | – | |
| | DB output delay time | $t_D$ | 100 | – | – | |
| | DB output hold time | $t_{DH}$ | 50 | – | – | |

($V_{DD}$ = 3.6V to 5.5V, Ta = – 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Read bus mode (6800-series MPU interface) | E cycle time | $t_C$ | 350 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | E pulse width high | $t_{WH}$ | 250 | – | – | |
| | E pulse width low | $t_{WL}$ | 100 | – | – | |
| | RS and CSB setup time | $t_{SU}$ | 40 | – | – | |
| | RS and CSB hold time | $t_H$ | 10 | – | – | |
| | DB output delay time | $t_D$ | 40 | – | – | |
| | DB output hold time | $t_{DH}$ | 10 | – | – | |

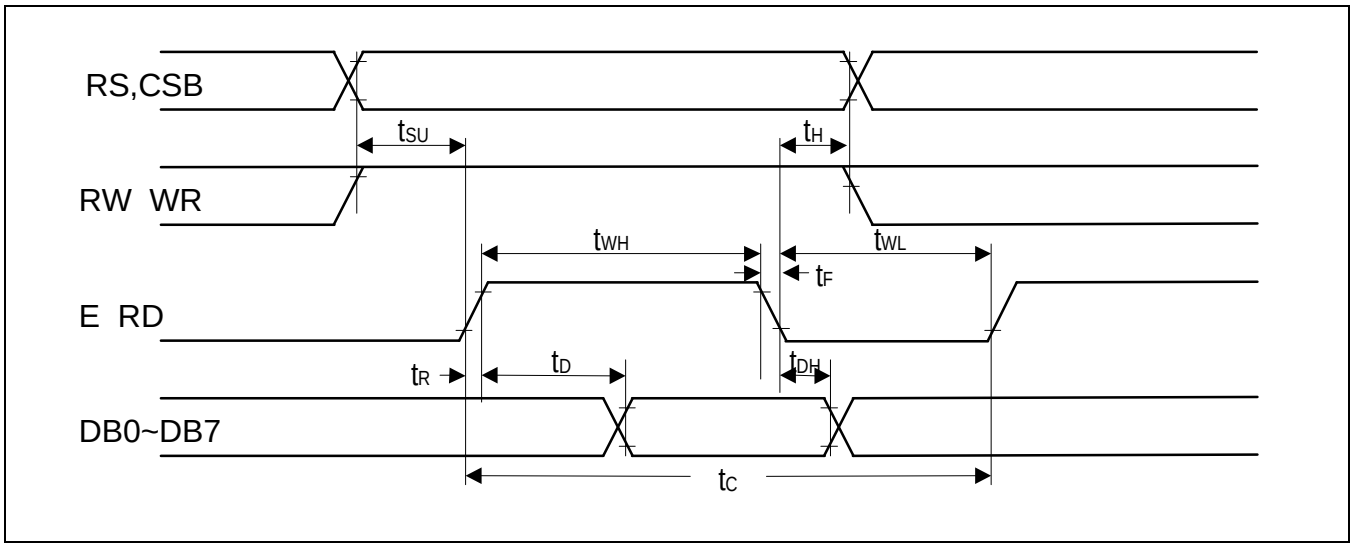



**Figure 30. Read Bus Mode Timing (6800-series MPU Interface)**

8080-Series MPU Interface & Read Instruction

($V_{DD}$ = 2.4V to 3.6V, Ta = – 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Read bus mode (8080-series MPU interface) | RD cycle time | $t_C$ | 650 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | RD pulse width high | $t_{WH}$ | 150 | – | – | |
| | RD pulse width low | $t_{WL}$ | 450 | – | – | |
| | RS and CSB setup time | $t_{SU}$ | 60 | – | – | |
| | RS and CSB hold time | $t_H$ | 30 | – | – | |
| | DB output delay time | $t_D$ | 100 | – | – | |
| | DB output hold time | $t_{DH}$ | 50 | – | – | |

($V_{DD}$ = 3.6V to 5.5V, Ta = – 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Read bus mode (8080-series MPU interface) | RD cycle time | $t_C$ | 350 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | RD pulse width high | $t_{WH}$ | 100 | – | – | |
| | RD pulse width low | $t_{WL}$ | 250 | – | – | |
| | RS and CSB setup time | $t_{SU}$ | 40 | – | – | |
| | RS and CSB hold time | $t_H$ | 10 | – | – | |
| | DB output delay time | $t_D$ | 40 | – | – | |
| | DB output hold time | $t_{DH}$ | 10 | – | – | |

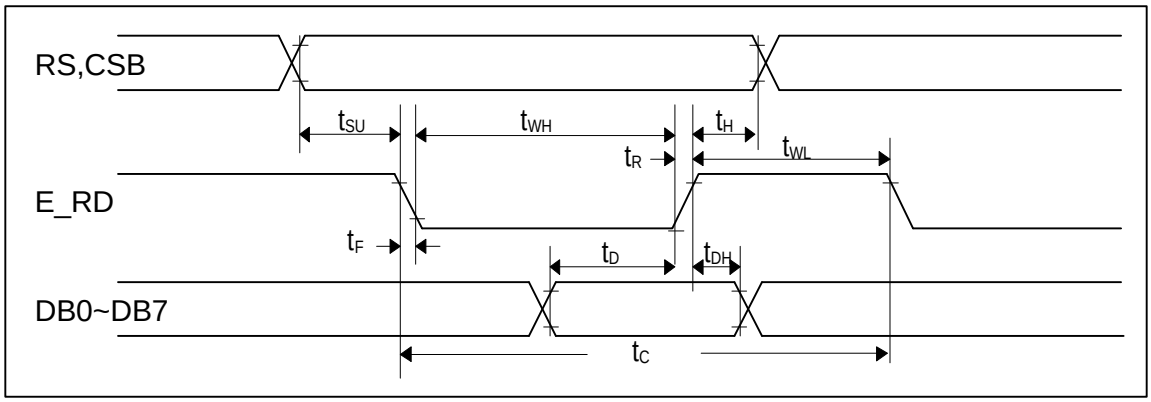



**Figure 31. Read Bus Mode Timing (8080-series MPU Interface)**

### Clock Synchronized Serial Mode

($V_{DD}$ = 2.4V to 3.6V, Ta = – 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock synchronized serial interface mode | SCL clock cycle time | $t_C$ | 1000 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | SCL clock width (H/L) | $t_W$ | 300 | – | – | |
| | CSB setup time | $t_{SU1}$ | 150 | – | – | |
| | CSB hold time | $t_{H1}$ | 700 | – | – | |
| | RS data setup time | $t_{SU2}$ | 50 | – | – | |
| | RS data hold time | $t_{H2}$ | 300 | – | – | |
| | SI data setup time | $t_{SU3}$ | 50 | – | – | |
| | SI data hold time | $t_{H3}$ | 50 | – | – | |

($V_{DD}$ = 3.6V to 5.5V, Ta = – 30 to + 85°C)

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock synchronized serial interface mode | SCL clock cycle time | $t_C$ | 600 | – | – | ns |
| | Pulse rise / fall time | $t_R$, $t_F$ | – | – | 25 | |
| | SCL clock width (H/L) | $t_W$ | 200 | – | – | |
| | CSB setup time | $t_{SU1}$ | 100 | – | – | |
| | CSB hold time | $t_{H1}$ | 400 | – | – | |
| | RS data setup time | $t_{SU2}$ | 40 | – | – | |
| | RS data hold time | $t_{H2}$ | 200 | – | – | |
| | SI data setup time | $t_{SU3}$ | 40 | – | – | |
| | SI data hold time | $t_{H3}$ | 40 | – | – | |

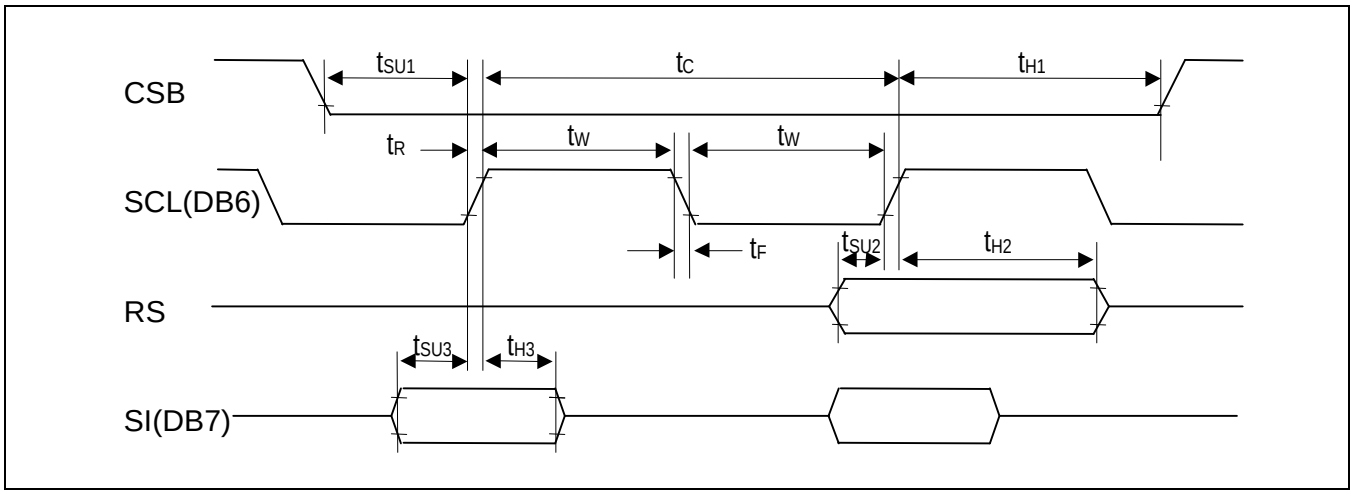



**Figure 32. Clock Synchronized Serial Interface Mode Timing Diagram**