CYNCP80192 Network Database Coprocessor

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 Overview

Cypress Semiconductor Corporation's (Cypress's) network database coprocessor (NDC) performs the following three primary functions.

- ***Interconnection bridge function.*** The CYNCP80192 device acts as a bridge between network processor(s) and a search subsystem of Cypress's CYNSE70XXX network search engines (NSEs) plus optional associated SSRAMs that contain a search database and the associated data for a variety of network protocol layers. The CYNCP80192 device interfaces to the network processor with an SSRAM interface and offloads the search function to provide support for fast packet processing in routers and switches.
- ***Pipeline management function.*** Cypress's NSEs have a pipelined architecture to optimize search performance and throughput. The CYNCP80192 device manages the pipeline for optimal search performance and packs instructions back to back in order to avoid any bubbles in the pipeline.
- ***Table management function.*** The CYNCP80192 device builds on the simple instructions of the NSEs to provide advanced instructions for table management.

There are two ways to build the NDC system.

- In the first system the associative data SRAMs are connected to the CYNCP80192 device and the NSE(s) (see Subsection 8.0, "NDC Subsystem Powerup Initialization Procedure" on page 15), and the CYNCP80192 device returns the associated data in response to a search operation. This type of implementation is suited to applications where the associative data size is up to eight bytes.
- In the second system, the CYNCP80192 device returns the index of the successful search entry to the network processor. The network processor uses this index to access SSRAMs in order to get the required results. The SSRAMs containing the associative data are connected directly to the network processor's SSRAM bus. This is suitable for applications where the associative data size is longer than eight bytes.

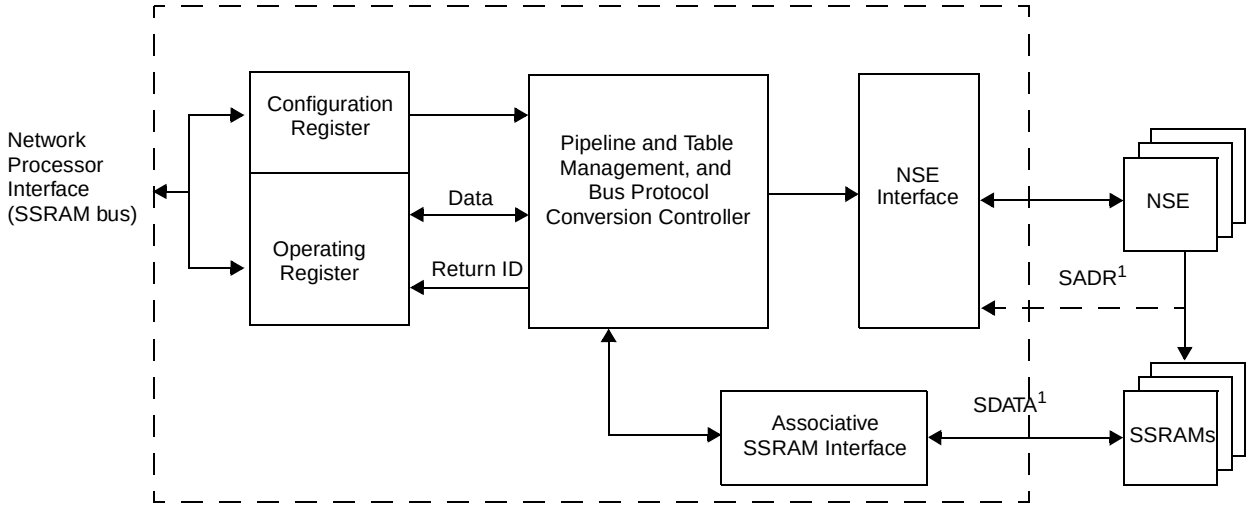
The NDC runs up to 100 MHz. At that speed and running with a 64-bit bus interface, the NDC performs at a peak rate of 33 million searches on 68-bit entries, 25 million searches on 136-bit entries, and 16.67 million searches on 272-bit entries. At 100 MHz speed and running with a 32-bit bus interface, the NDC performs at a peak rate of 25 million searches on 68-bit entries, 16.67 million searches on 136-bit entries, and 10 million searches on 272-bit entries.

The NDC supports centralized, multiple layer, multiwidth tables in order to provide cost effective search solutions for Ethernet, asynchronous transfer mode (ATM), and Sonet-based switches and routing systems. It supports the following advanced capabilities: quality of service (QoS), class of service (CoS), virtual private network (VPN), packet and flow classification, and security.

2.0 Features

- The hardware interface to the NDC uses an SSRAM interface. The CYNCP80192 device supports ZBT pipelined, ZBT flowthrough, SyncBurst pipelined, and SyncBurst flowthrough types of SSRAMs.
- All instructions and/or responses are mapped into the SSRAM address (ADR) space.
- The CYNCP80192 device provides simultaneous multiple layer, variable-width tables (×68, ×136, ×272).
- There is support for table sizes up to four million ×34 entries.
- There are 33 million searches per second (Msps) in the ×68 configuration (CFG).
- The CYNCP80192 device is compatible with 1 Mb, 2 Mb, and 4 Mb NSEs.
- It has a glueless interface to industry standard synchronous SRAMs and NSEs.
- The CYNCP80192 device uses up to 100 MHz master clock frequency.
- It has an IEEE 1149.1 test access port.
- There is a 2.5V/3.3V power supply and a 388-pin BGA package.

The CYNPC80192 NDC contains the following function blocks, as shown in Figure 2-1.



1. The device can be configured for returning SADR or SDATA.

Figure 2-1. CYNCP80192 Block Diagram

3.0 Functional Description

3.1 Configuration Registers

The CFG registers contain information for configuring the CYNPC80192. These registers also include error, status, mask, and information registers.

3.2 Operating Registers

This logic block contains the random access registers through which the network processor(s) perform most of the table programming, management functions, and search operations (via a request-response protocol). A network processor posts operation requests and Reads responses back from this access block.

3.3 Pipeline and Table Management and Bus Protocol Conversion Logic

This unit uses pipeline management logic to optimize the search performance through the NSE pipeline. This unit posts the commands to the NSE and steers the results to the appropriate locations in the operating registers. It also converts the SSRAM interface information from a network processor into protocol cycles of the NSE transactions. This unit builds on the commands provided by the NSE to provide more advanced table management commands to the network processor.

3.4 NSE Interface

This interface generates the appropriate hardware handshake with the NSE(s). This block is a slave to the pipeline control unit and drives the NSE(s) bus with the appropriate commands.

3.5 Associative SSRAM Interface

The data transfer between the SSRAM and the pipeline unit takes place in this interface. The pipeline unit further transfers this information to the operating registers.

4.0 Signal Description

Table 4-1 provides information on pins and signal names for the CYNCP80192 device. Under the “Type” heading, I = Input, O = Output, and T = 3-state.

Table 4-1. Search Coprocessor Pin Description

Symbol	Type	Description
Network Processor Interface		
IRST_L	I	***Synchronous Reset Input***. Active low. Initializes the device to a known state.
CLK[1]	I	***Coprocessor Clock Input***. CLK may be run up to 100 MHz.
ADR[9:0]	I	***Coprocessor Location Address***. This 10-bit address bus ADRs up to 1024 32-bit locations in the coprocessor. These 1024 locations are further divided into 512 32-bit locations of CFG area and 512 32-bit locations of the operating register area. When the data bus is configured as 64 bits wide (using the IWIDTH pin described below), the ADR[0] is ignored by the device. When the data bus is configured as 32 bits wide (using the IWIDTH pin described below), all the ADR bits are used by the device.
DATA[63:0]	IO	***Coprocessor Data Bus***. Only the [31:0] field of this bus is used when the coprocessor is configured for a 32-bit interface (using the IWIDTH pin described below).
CE_L	I	***Coprocessor Chip Enable***. This active low signal is used to enable the device. This is one of the three chip enables (CEs) to the coprocessor. All three CEs must be active to select the coprocessor.
CE2_L	I	***Coprocessor Chip Enable***. This active low signal is used to enable the device. This is another one of the three CEs to coprocessor. All three CEs must be active to select the coprocessor.
CE2	I	***Coprocessor Chip Enable***. This active high signal is used to enable the device. This is another one of the three CEs to the coprocessor. All three CEs must be active to select the coprocessor.
R/W_L	I	***Read/Write***. This input determines whether it is a Read or a Write cycle. A low on this pin means it is a Write operation, and a High means it is a Read operation.
OE_L	I	***Coprocessor Output Enable***. This active low asynchronous signal enables the output drivers of the data bus.
BW_L[7:0]	I	***Synchronous Byte Write Enables***. These active low signals allow individual bytes to be written when a Write cycle is active. When the data bus is configured as 32 bits wide, only BW_L[3:0] is used and the BW_L[7:4] should be tied to V_{DD} externally.
BWE_L	I	***Byte Write Enable***. This active low signal allows the byte Write signals (BW_L[7:0]) to control the Write operation.
STRB	O	When the done bit is set in result register 0, STRB qualifies the CPID[7:0]. The network processor can use STRB signal to latch the CPID signals.
CPID[7:0]	O	***Context ID and Processor ID***. When the result is Ready in the descriptor, the NDC outputs the processor and context IDs are concatenated as follows: {processor ID, context ID}. The bit length of the processor and context IDs can be programmed using the CFG register 0 (see CPCFG). See the STRB signal description also.
INTR/INTR_L	O	This interrupt pin is asserted when the SE_FULL, DESC_AFULL, or error bits filed is set in the error status register. Interrupt can be active high or low, depending upon the polarity selected in the CFG register.
SE_FULL	O	NSE table full indicator to the network processor.
DESC_AFUL	O	This bit indicates that the descriptor array is almost full. When this flag is set, the processor can send only two more commands to the descriptor. The DESC_AF flag will be cleared if more that two descriptors are available.
NSE Command and DQ Bus		
CLK2X	O	***NSE Master Clock***. CYNPC80192 drives this CLK to the NSE. The frequency of this CLK is twice the frequency of the NSE. This CLK runs up to 100 MHz and is derived by buffering the input CLK at the coprocessor interface.
PHS_L	O	***Phase Signal to the NSE***. This signal runs at half the frequency of CLK2X and synchronizes the alignment of the instruction to the NSE.
ORST_L	O	***Reset Output to the NSE***. Driving ORST_L low initializes the NSE.
CMD[8:0]	O	***Command Bus to the NSE***. Bits [1:0] specify the command and [8:2] contain the command parameters. The descriptions of individual commands explain the details of the parameters. The encoding of commands based on the [1:0] field are: 00: Read; 01: Write; 10: Search; 11: Learn.

Symbol	Type	Description
CMDV	O	***Command Valid to the NSE***. Qualifies the CMD bus. 0: No command. 1: Command valid.
DQ[67:0]	IO	***NSE Address/Data Bus***. This signal carries the Read and Write address and data during register, data, and mask array operations. It carries the compare data during search operations. It also carries the SSRAM address during SSRAM accesses to the SSRAMs containing the associative data.
DQ_72	IO	When the CYNSE70128 NSE is used, the four additional DQ bits DQ[68:71] on the CYNSE70128 should be connected to the DQ_72 output from the CYNPC80192. The DQ_72 signal is driven low from the CYNPC80192.
ACK	I	***Read Acknowledge***. This signal indicates that valid data is available on the DQ bus during register, data, and mask array Read operations to the NSE, or that the data is available on the SRAM data bus during Read operations of the SRAM containing associative data.
EOT	I	***End of Transfer***. This signal indicates the end of a burst transfer during Read or Write burst operations to the NSE.
SSF	I	***Search Successful Flag***. This signal indicates that the search was successful in the NSE bank.
SSV	I	***Search Successful Flag Valid***. When asserted, this signal qualifies the SSF signal.
FULL	I	NSE entries full indicator.
XVER_0	O	Transceiver enable for driving signals to the NSE. Active high.[2]
XVER_0_L	O	Transceiver enable for driving signals from the NSE. Active low.[2]
XVER_1	O	Transceiver enable for driving signals to the NSE. Active high.[2]
XVER_1_L	O	Transceiver enable for driving signals from the NSE. Active low.[2]
XVER_2	O	Transceiver enable for driving signals to the NSE. Active high.[2]
XVER_2_L	O	Transceiver enable for driving signals from the NSE. Active low.[2]
Associated SRAM Interface		
SDATA[63:0]/ SADR[23:0]	I/O I/O	***SRAM Data/Address***. This bus contains either the data from the associative SSRAM or the ADR (Index) from an NSE, depending on the value of the SRAM present bit in CFG register 0. {SDATA[63:0]} from SSRAMs should be connected to the 64-bit bus if the associative SSRAM is present, or else {SADR[23:0]} from the NSEs should be connected to the 64-bit bus.
SOE_L	I	***SSRAM Output Enable***. This signal is the output enable control for the off-chip SSRAM bank that contains associative data and is driven by the NSE.
SCLK	O	***SSRAM Clock***. This is the same in phase and frequency as the one created internally by the NSE. It is generated by dividing CLK by two, and is used to drive the SSRAM CLK input.
Configuration		
IWIDTH	I	This signal selects coprocessor data bus width. 1: 64 bits; 0: 32 bits.
BIG/LTL_L	I	This is the network processor addressing mode. 1: Big Endian; 0: Little Endian.
IFC_CFG[2:0]	I	This signal selects coprocessor interface type: 000: ZBT pipelined mode 001: ZBT flowthrough mode 010: SyncBurst pipelined mode (early Write) 011: SyncBurst pipelined mode (late Write) 100-111: Reserved.
Test Access Port		
TDI	I	IEEE 1149 JTAG test data in.
TCK	I	IEEE 1149 JTAG test clock.
TDO	T	IEEE 1149 JTAG test data out.
TMS	I	IEEE 1149 JTAG test mode select.
TRST_L	I	IEEE 1149 JTAG reset.

1. “CLK” is an internal clock signal.
2. Detailed information on the external transceiver is given in Section 14.0, “Information on External Transceivers,” on page 20.

5.0 Clocks

The CYNPC80192 receives up to a 100 MHz master CLK at the coprocessor interface. The CYNPC80192 then generates the CLK2X and a phase signal PHS_L for the NSEs, and the SCLK for the associative data SSRAMs, as shown in Figure 5-1.

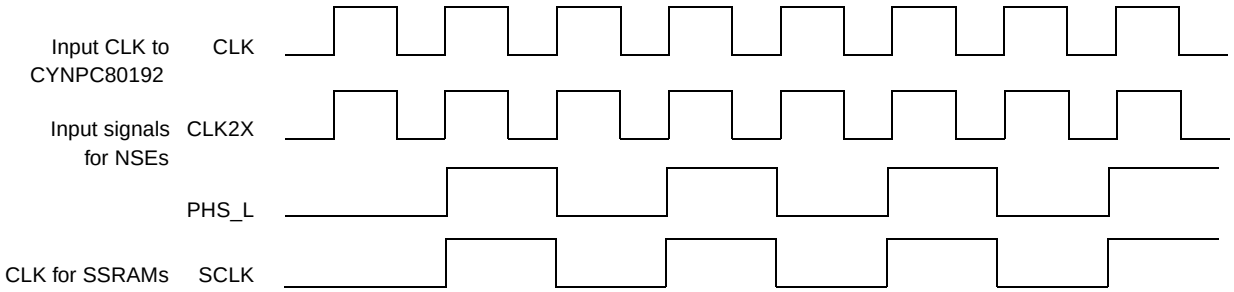


Figure 5-1. NDC Clocks

6.0 Registers

6.1 Coprocessor Interface Register

The network processor(s) access the NDC using the coprocessor (SSRAM) interface. The NDC has a CFG and status registers area and an operating registers area, as shown in Table 6-1.

Table 6-1. Register Partitions for Coprocessor Access

Address	Abbreviation	Type	Description
0–511	CFG and Status Registers	R/W	These registers are for configuring the NDC (Read/Write), reporting the error code in the status register (Read only), setting up the mask register for asserting INTR (Read/Write), and obtaining information on the device (Read only).
512–1023 ADR[9] = 1	Operating Registers	R/W	Dynamic access for searches and table management happens through this area of the coprocessor address space.[1]

1. The resulting registers of the context descriptors are Read only.

The CFG area shown in Table 6-2 is used for programming the NDC via a 64-bit CFG register.[1]

Table 6-2. Configuration and Status Registers Area

Address	Configuration and Status Registers Area
0–1	CFG Register
2–3	Error, Status Registers (Read only)
4–5	Mask Registers
6–7	Reserved
8–9	Information Registers (Read only)
10–511	Reserved

1. Once the NDC is configured, the network processors will use the operating registers area to configure the NSEs, initialize and manage the protocol layer tables, and perform searches through such tables.

6.2 Configuration and Status Registers

6.2.1 Configuration Register

The 64-bit CFG register contains the following fields, as shown in Table 6-3.

Table 6-3. Configuration Register

Configuration Register [63:0]									
ADR	63–12	11	10	9	8	7–6	5–3	2–1	0
0–1	Reserved	External Transceiver Present	Search Result Bit in Data Field	INTR_Polarity	SSRAM Present	CPCFG	HLAT	TLSZ	SRST

SRST. This active high bit resets the state of the device. The reset bit will be active for 32 CLK cycles and will be automatically cleared after the reset has taken effect.

Table Size (TLSZ). This determines the NSE CFG for the specific table size.[1]

Latency of Hit Signals (HLAT). This determines the data access latency of associated data SSRAM.[2]

CPCFG. This field sets the width of the processor and context IDs that will be driven on the CPID bus after the completion of the operation. The contents of the CPID bus are generated by concatenating LSBs of the processor ID and the LSBs of the context ID.

00: CPID[7:0] = {processor ID[2:0], context ID[4:0]}.

01: CPID[7:0] = {processor ID[3:0], context ID[3:0]}.

10: CPID[7:0] = {processor ID[4:0], context ID[2:0]}.

11: Reserved.

SSRAM Present. This field informs the coprocessor whether the associative data SSRAM is connected to the NSE (bit is set to 1; see Figure 13-1) or connected to the network processor SRAM interface (bit is set to 0; see Figure 13-2).

INTR_Polarity. This bit controls the polarity of the INTR/INTR_L signal. When this signal is high, the INTR/INTR_L signal is active high. When this signal is low, the INTR/INTR_L signal is active low.

Search Result Bit in Data Field. If this bit is set to 1, the Hit or Miss information will be attached to the associative data field in bit 63. This bit has significance only when associative SSRAM is present (see Result Register 1 for the Search command). This bit does not replace the hit bit located in Result Register 0.

External Transceiver Present. If an external transceiver is used to drive several NSE devices, this bit should be set to 1.

6.2.2 Error and Status Register

The error and status register is 64 bits wide. Table 6-4 shows the bit positions of the error status register. The errors shown in Table 6-5 will be detected by the NDC and the corresponding error bit will be set in the error and status register. Once it is Read, the error and status register will be cleared.

Error Bits. The error bits field holds the type of error. In the case of multiple errors, multiple error bits may be set. The context descriptor index will contain the index where the last error occurred. When an error occurs, the error bit is set along with the done bit in Result Register 0. The class and type of error (soft error [SE] or hard error [HE]) are indicated in the error and status register. When an error occurs, the INTR signal is asserted and a corresponding error bit is set along with the context descriptor index to identify the erroneous command. The interrupt signal is programmable as active low or active high depending upon the system requirement. See the description of the CFG register for further detail.

Table 6-4. Error and Status Register

63–32	31	30	29	28	27	26–13	12–8	7–0
Reserved	HE	SE	SE_FULL	DESC_FULL	DESC_AFULL	Reserved	Context Desc Index	Error Bits

1. Though the NDC does not program the NSE with this information, the coprocessor uses it to determine the duration of operations such as Search and Learn. (More details on this field can be found in the datasheets for CYNSE70XXX NSEs.)
2. Though the NDC does not program the NSE with this information, the coprocessor uses it to determine the duration of operations such as Search and Read from the SSRAMs. (More details on this field can be found in the datasheet on CYNSE70XXX NSEs.)

Table 6-5. Error Codes

Error Bit	Error Description
0	Invalid Command (SE)
1	Reserved
2	Reserved
3	Search or Learn size invalid (i.e., 11 in search size field is not allowed) (SE)
4	NSE access time out (HE)
5	Reserved
6	Reserved
7	Reserved

Context Descriptor Index. This field identifies the context descriptor that caused the last error condition. In the case of multiple errors, this field will be overwritten.

DESC_AFULL. This bit indicates that the descriptor array is almost full. When this flag is set, the processor(s) can send only two more commands to the descriptors. The DESC_AF flag will be cleared if more that two descriptors are available.

DESC_FULL. This bit indicates that the descriptor array is full. When this flag is set, the processor can send no commands to the descriptor. The DESC_FULL flag is cleared upon Reading the status register.

SE_FULL.[1] This bit indicates that the table in the NSE is full.

SE. The SE bit indicates that the error is recoverable and that the command has to be reissued.

HE. The HE bit indicates that the error is not recoverable, and that the coprocessor has to be reset and reinitialized by the software before further operations are attempted.

6.2.3 Mask Register

The mask register is 64 bits wide. The bits in this field can be used to mask the INTR generated by any of the bits set in the error and status register. Setting the bits in this register causes the interrupt to be masked. The default value in the mask register is FFFFFFFF (lower 32 bits only).

6.2.4 Information Register

The information register is 64 bits wide. Table 6-6 describes the lower-order 32 bits in the information register. It uses ADRs 8 and 9 of the CFG register area.

Table 6-6. Information Register Description

ADR	Field	Range	Initial Value	Description
8	Revision	[3:0]	0001	***Revision Number***. This is the current device revision number. Numbers start at one and increment by one for each revision of the device.
	Implementation	[6:4]	001	This is the CYNPC80192 implementation number.
		7	0	Reserved.
	Device ID	[15:8]	00000011	Product code for CYNPC80192.
	MFID	[31:16]	1101_1100_0111_1111	***Manufacturer ID***. This field is the same as the manufacturer ID used in the TAP controller.
9	–	[63:32]	–	Reserved.

7.0 Operating Registers

There are 512 uniquely addressable 32-bit-wide registers (see Table 7-1). These 512 registers are divided into 32 descriptors and are called context descriptors (or “context”). Each context comprises 16 registers (i.e., 32 × 16 = 512). Each of these contexts is used for storing commands, data, and responses (returned results from NSEs). These 32 contexts provide a 32-deep pipeline for the network processor(s) system. The allocation of contexts between the multiple processors (or one processor running multiple processors) can be done by the network processor system. For example, a network processor system having four processing elements can assign eight contexts for each processor.

1. SE_FULL may be altered as a result of executing a Learn or Write command by the NSE. This flag will be cleared upon reading the status register.

7.1 Address Mapping

Table 7-1. Operating Registers Addressing Mapping (ADR[9] = 1)

ADR[8:0]	Contents
0–15	Context 0
16–31	Context 1
32–47	Context 2
48–63	Context 3
64–79	Context 4
80–95	Context 5
96–111	Context 6
112–127	Context 7
128–143	Context 8
144–159	Context 9
160–175	Context 10
176–191	Context 11
192–207	Context 12
208–223	Context 13
223–239	Context 14
240–255	Context 15
256–271	Context 16
272–287	Context 17
288–303	Context 18
304–319	Context 19
320–335	Context 20
336–351	Context 21
352–367	Context 22
368–383	Context 23
384–399	Context 24
400–415	Context 25
416–431	Context 26
432–447	Context 27
448–463	Context 28
464–479	Context 29
480–495	Context 30
496–511	Context 31

7.2 Context Descriptor Organization

Table 7-2 shows the organization of the context descriptor. During normal operation, the network processor Writes in the context descriptor block (addresses 0–9 within the block) with the command and the appropriate data and Reads the results from the context descriptor block (addresses 12–15 within the block). ***Note***. In 64-bit bus mode, the even and the next odd location are accessed in the same cycle, and ADR[0] is ignored.

Table 7-2. Context Descriptor Organization

ADR	Context Descriptor Organization	Access
0–1	Command Descriptor	R/W
2–3	Data 0	R/W
4–5	Data 1	R/W
6–7	Data 2	R/W
8–9	Data 3	R/W
10–11	Reserved	—
12–13	Result Register 0	R
14–15	Result Register 1	R

Depending on the type of command, the network processor may only need to Write to selected locations of Data 0–3, and may only need to Read from selected locations of Result Register 0 or 1. ***Note***. Addresses 0–9 are Read/Write and addresses 12–15 are Read-only locations.

7.3 Context Descriptor Commands

This 64-bit word (eight bytes) describes the command to the coprocessor. The contents of each of these eight bytes and a description of each of these fields are described below in Table 7-3.

Table 7-3. Descriptor Command

Bit Positions	Field Description							
	7	6	5	4	3	2	1	0
63–56	Reserved			Context ID				
55–48	Reserved			Processor ID				
47–40	Reserved	Search Successful Register Index			Reserved	Global Mask Index		
39–32	Reserved	SSRAM Address Prefix			Comparand Register Index			
31–24	Reserved		Direct/Indirect	Access Location		Search Size		Start
23–16	Layer Attribute/Valid Bit for Data 3				Layer Attribute/Valid Bit for Data 2			
15–8	Layer Attribute/Valid Bit for Data 1				Layer Attribute/Valid Bit for Data 0			
7–0	Command							

Context ID. This field contains the context ID that a network processor has assigned to this specific context.

Processor ID. This field contains the ID number of the network processor that wrote the descriptor.

Global Mask Index. This field is used only for Search, Write, Move, and Swap commands to the NSE(s). This field selects one of the eight global mask register (GMR) pairs from the NSE bank for Search, Write, Move and Swap commands. In the case of a 272-bit search, two pairs of GMRs are used. These two pairs include one that is specified in the command and other is a subsequent pair. For example, if the GMR pair 7 is specified, the GMR pair 0 will be used as the subsequent pair for 272-bit-wide searches.

Search Successful Register Index. The search successful register (SSR) index field is used only for Search and Write operations to the NSEs. Up to eight search successful indexes are stored in each of the NSEs. This field selects one of those eight registers for the Search and indirect Write operations to the NSEs. (Refer to the datasheet specifications of the CYNSE70XXX devices for further information.)

Comparand Register Index. This field is used only for Search and Learn operations. This field specifies the comparand register in each of the NSEs that will store the comparands (as they are searched). A subsequent Learn instruction can insert the stored comparands in a table residing in the NSE(s). (Refer to the datasheet specifications of CYNSE70XXX devices for further information.)

SSRAM Address Prefix. In the implementation with a SSRAM connected to the NSE (see Figure 13-1), these three bits are used as an SSRAM address prefix (SAP) to generate the address of the associative SSRAM. (Refer to the datasheet specifications of the CYNSE70XXX devices for further information.)

Start. When the command and associated parameters have been written to the command descriptor, a process running on the network processor can set this bit to initiate the operation by the CYNPC80192.

Search Size. This 2-bit field is used only by Search and Learn instructions and describes the word size for these operations. ***Note***. Learn command is not supported in the 272-bit wide table. The following describes the data that will be presented to the NSE for various search sizes.

000: ×68 ({Data 0, layer attribute/valid bit for Data 0})

001: ×136 ({Data 1, layer attribute/valid bit for Data 1; Data 0, layer attribute/valid bit for Data 0})

010: ×272 ({Data 3, layer attribute/valid bit for Data 3; Data 2, layer attribute/valid bit for Data 2; Data 1, layer attribute/valid bit for Data 1; Data 0, layer attribute/valid bit for Data 0}.

Note. The two-bit search size must contain 00 for non-Search/Learn instructions.

Access Location. This two-bit field is used by Read, Write, Move, and Swap instructions, and indicates the region accessed in the NSEs or the associative data SSRAMs.

000: NSE data array.

001: NSE mask array.

010: SRAM connected to the NSE.

011: NSE internal registers.

Direct/Indirect. This one-bit field is used by Read and Write instructions and controls the address generation to the NSEs and the associated data SSRAMs. When this bit is set, it specifies indirect addressing using SSRs in the NSEs. (Refer to the specifications of CYNSE70XXX for further information.)

Layer Attribute and Valid Bit for Data 0. This field contains the three-bit layer attribute as well as a valid bit to accompany data in the Data 0, in the context descriptor. The layer attributes bits may be used for maintaining multiple search tables (of different widths) in the NSE(s). However, if multiple search tables are not used, these bits can be used for any purpose.

Layer Attribute and Valid Bit for Data 1. This field contains a three-bit layer attribute as well as a valid bit to accompany data in the Data 1, in the context descriptor. The layer attributes bits may be used for maintaining multiple search tables (of different widths) in the NSE(s). However, if multiple search tables are not used, these bits can be used for any purpose.

Layer Attribute and Valid Bit for Data 2. This field contains the three-bit layer attribute as well as a valid bit to accompany data in the Data 2, in the context descriptor. The layer attributes bits may be used for maintaining multiple search tables (of different widths) in the NSE(s). However, if multiple search tables are not used, these bits can be used for any purpose.

Layer Attribute and Valid Bit for Data 3. This field contains the three-bit layer attribute as well as valid bit to accompany data in the Data 3, in the context descriptor. The layer attributes bits may be used for maintaining multiple search tables (of different widths) in the NSE(s). However, if multiple search tables are not used, these bits can be used for any purpose.

Commands. NDC currently supports six basic commands. Command bits 7 through 3 are reserved and must be programmed as 0s for the following commands:

000: Read

001: Write

010: Search

011: Learn

100: Move

101: Swap.

7.3.1 Command Description and Parameters

Read Command (00 H). Table 7-4 shows the format for the Read command. The Read command's structure is rd(ADR). The Read command uses two 64-bit words in the context descriptor, command descriptor word, and Data 0 word. The Read command is issued through the command descriptor. The Read access location, either data array, mask array, NSE register, or external SSRAM is encoded in the command descriptor word. Bits 15–0 of the Data 0 word contain the Read address. Bits 23–19 of the Data 0 word supply the NSE ID (SEID).

Result Registers 0 and 1 return the result of the Read operation in two 64-bit words.

Table 7-4. Read Command

Address	63–24	23–19	18–16	15–0
Data 0	Reserved	SEID	Reserved	Address Pointer

Write Command (01 H). Table 7-5 shows the format for the Write command. The Write command's structure is wr(ADR, dt). The Write command uses three 64-bit words in the context descriptor: command word, Data 0 word and Data 1 word. The Write command is issued through the command descriptor. The Write access location could be either the data array, mask array, NSE register or associative SSRAM connected to the NSE. Bits 15–0 of the Data 0 word contain the Write address. Bits 23–19 of the Data 0 supply the SEID. The Data 1 word contains the data bits [67:4], while the data bits [3:0] (called layer bits for Data 1) are passed in the command descriptor word.

Table 7-5. Write Command

Address	63–24	23–19	18–16	15–0
Data 0	Reserved	SEID	Reserved	Address Pointer
Data 1	Data [67: 4]			

Search Command (02H). The Search command's structure is se(dt0) for 68-bit word, se(dt0,dt1) for 136-bit word and se(dt0,dt1,dt2,dt3) for 272-bit word. The Search command uses two, three, or five 64-bit words in the context descriptor depending upon the size of the search entry (68-bit, 136-bit, or 272-bit). The search size is encoded in the command word, bits [26:25]. Data bits [3:0] for each 68-bit NSE word are stored in the command word in layer attribute bits for Data 0 through Data 3. The number of layer attribute bits used in the command word depends upon the search size. Thus, for a 68-bit search the descriptor command bits [11:8] will be used; for a 136-bit search, bits [15:8] will be used and for a 272-bit search, bits [23:8] will be used. The indices for SSR, GMR, and comparand register are stored in the command word also. (For further explanation of these indices, refer to datasheets for the CYNSE70XXX NSEs.)

Successive search operations are pipelined. For a 64-bit network processor interface running at 100 MHz, the NDC can sustain 33 Msps for tables configured as ×68 bit in the NSEs. For ×136-bit CFG, the performance will be 25 Msps, and for ×272-bit CFG, the peak performance will be 16.67 Msps. For a 32-bit network processor Interface, the peak performance will drop by a factor of one half compared to the performance of the 64-bit interface.

7.3.2 Context Descriptor Data 0–Data 3

For the Search command these words contain the search key that will be presented to the NSEs. Table 7-6 shows the meaningful fields for each search size that are driven on the NSE bus DQ from the descriptors.The data driven on the DQ[3:0] for various searches is picked from the command word as follows.

68-bit search: layer attribute and valid bits for Data 0.

136-bit search: layer attribute and valid bits for Data 0 and Data 1.

272-bit search: layer attribute and valid bits for Data 0, Data 1, Data 2, and Data 3.

Table 7-6. Search Data

Search Size	Meaningful Data (64 bits each)
00	Data 0 —> DQ[67:4] (Cycle A and B)
01	Data 0 —> DQ[67:4] (Cycle A), Data 1 —> DQ[67:4] (Cycle B)
10	Data 0 —> DQ[67:4] (Cycle A), Data 1 —> DQ[67:4] (Cycle B) Data 2 —> DQ[67:4] (Cycle C), Data 3 —> DQ[67:4] (Cycle D)
11	Reserved

Result Registers 0 and 1 return the result of the search operation.

Learn Command (03H). The Learn command's structure is le(indx). The Learn command will use two 64-bit words (command descriptor word and Data 0) in the context descriptor. The command includes an index for a Comparand register of the NSE, where the data to be Learnt was stored by a prior search instruction. Data 0 contains the data to be written in associative SRAM. Learn will result in error if the Learn is performed when the NSE SE_FULL is high. The error bit in the result register will indicate the error. The Learn error will be set in the error and status register.

Move Command (04 H). The Move command's structure is mv(addr1, addr2, len). The Move command utilizes two 64-bit words in the context descriptor: command descriptor word, and Data 0 word. Bits 15–0 of the Data 0 word will contain the source address; bits 23–19 will contain the SEID; bits 39–24 will contain the destination address, bits 47–43 will contain the destination SEID; and bits 56–48 will contain the move block length (see Table 7-7). Current implementation restricts the maximum move block length to 256 words (of 68-bit each) in between/within the NSE(s). The minimum length for the Move command is four locations.

Table 7-7. Move Command Parameters

ADR	63–57	56–48	47–43	42–40	39–24	23–19	18–16	15–0
Data 0	Reserved	Move Length	Destination SEID	Reserved	Destination Address Pointer	Source SEID	Reserved	Source Address Pointer

For Move instruction, Data 0 is used to pass the source address pointer and SEID, destination address pointer and the SEID, and the number of ×68 entries to be moved move/swap length.

The NDC implements the Move instruction as Burst Read and then a Burst Write into the NSEs.

Swap Command (05H). The Swap command's structure is sw(addr1, addr2, len). The Swap command will use two 64-bit words in the context descriptor: command word, and Data 0 word. Bits 15–0 of the Data 0 word will contain the first address; bits 23–19 will contain the first SEID; bits 39–24 will contain the second address, bits 47–43 will contain the second SEID; and bits 56–48

will contain the Swap block length (see Table 7-8). The maximum Swap block length is 128 words (of 68-bit each) in the NSE. The minimum length for Swap is four locations.

Table 7-8. Swap Command Parameters

ADR	63–7	56–48	47–43	42–40	39–24	23–19	18–16	15–0
Data 0	Reserved	Swap Length	Second SEID	Reserved	Second Address Pointer	First SEID	Reserved	First Address Pointer

For Swap instruction, Data 0 is used to pass the first address pointer and SEID, the second address pointer and SEID, and the number of ×68 entries to be swapped. The NDC implements the Swap instruction as two burst Reads and then two burst Writes into the NSEs. ***Note***. The Move and Swap commands will not work across the NSE boundaries if several NSEs are cascaded.

7.3.3 SSRAM Read/Write

For SSRAM (connected to the NSE) Read or Write operations, Data 0 is used to pass the SSRAM address and SEID. Data 1 is used for passing the data for a Write operation. Table 7-9 shows the format for Data 0 and Data 1 for accessing the SSRAM.

Table 7-9. SSRAM Data

ADR	63–24	23–19	18–16	15–0
Data 0	Reserved	SEID	Reserved	Address[15:0]
Data 1	Data[63:0]			

For NSE Read and Write operations, the Data 0 is used to pass address and SEID. Data 1 is used for passing data for Write operations. This 64-bit Data 1 field holds data[67:4] for the NSE, while data[3:0] is held in the layer attribute and valid bits field of the command descriptor word. The NSE operation can be on the array, mask array, or the command registers. Table 7-10 shows the format for Data 0 and Data 1 for accessing the NSE data, mask, and register locations.

Table 7-10. NSE Data, Mask, and Register Locations

ADR	63–24	23–19	18–16	15–0
Data 0	Reserved	SEID	Reserved	Address[15:0]
Data 1	Data[67:4]			

7.3.4 Result Register 0 and 1 for Read Operation

These two registers return the result of the Read operation in two 64-bit words. Result Register 0 contains the four least significant bits of data (layer attribute/valid bits) and the status of Read operation along with the processor and context ID. This is shown in Table 7-11.

Table 7-11. Read Response at Result Register 0

Bit Positions	Associative Data SSRAM Connected to Coprocessor Bus							
	7	6	5	4	3	2	1	0
63–56	Reserved							
55–48	Reserved							
47–40	Reserved							
39–32	Reserved			Processor ID[4:0]				
31–24	Done	Reserved		Context ID [4:0]				
23–16	Reserved							
15–8	Reserved							
7–0	Reserved				SE Data[3:0]			

Processor ID[4:0]. The processor ID from the command descriptor is identified here.

Context ID[4:0]. The context ID from the command descriptor is identified here.

Done. This field indicates that the Read operation is complete. When the done bit is set, the next command can be written in the descriptor. The done bit is cleared when the Result Register 0 is Read by the network processor.

SE Data[3:0]. This field contains the least four significant bits (layer attribute/valid bits) Read from the NSE 68-bit word. (This field is valid only when Reads are done from the NSE.)

Result Register 1 contains the SE Data[67:4] Read from the NSE (Table 7-12) or Data[63:0] Read from the SSRAM connected to the NSE (Table 7-13).

Table 7-12. Data Read from NSE

ADR	63–0
Result 1	SE Data[67:4]

Table 7-13. Data Read from SSRAM

ADR	63–0
Result 1	SSRAM Data[63:0]

7.3.5 Result Register 0 and 1 for Write/Move/Swap/Learn Operations

Only Result Register 0 carries meaningful data, as is shown in Table 7-14 below.

Table 7-14. Write/Move/Swap/Learn Results Register 0

Bit Positions	Associative Data SSRAM Connected to Coprocessor Bus							
	7	6	5	4	3	2	1	0
63–56	Reserved							
55–48	Reserved							
47–40	Reserved							
39–32	Reserved			Reserved				
31–24	Done	Reserved	Reserved	Reserved				
23–16	Reserved							
15–8	Reserved							
7–0	Reserved							

Done. This field indicates that the command has been processed. When the done bit is set, the next command can be written in the descriptor. The done bit is cleared when the Result Register 0 is Read by the network processor.

Result Register 1 is not used for Write/Move/Swap/Learn commands.

7.3.6 Result Register 0 and 1 for Search Operation (Case 1)

For the search operation where an SSRAM is connected to the NSE (Figure 7), the Result Register 0 carries search status, processor ID and context ID and is shown in Table 7-15. The associative data is returned in Result Register 1 if the search succeeded, as shown in Table 7-16. In addition, if the search result in data field bit in the CFG register is set, then bit[63] of Result Register 1 indicates a search success (bit[63] = 1) or search failure (bit[63] = 0). In this case bits 62–0 contain the 63-bit associative data from the SSRAM, as is shown in Table 7-17.

Table 7-15. Result Register 0 for Search Operation

Bit Positions	SE Data/Mask Array access Results							
	7	6	5	4	3	2	1	0
63–56	Reserved							
55–48	Reserved							
47–40	Reserved							
39–32	Reserved			Processor ID [4:0]				
31–24	Done	Hit	Reserved	Context ID [4:0]				
23–16	Reserved							
15–8	Reserved							
7–0	Reserved							

Processor ID[4:0]. The processor ID from the command descriptor is identified here.

Context ID[4:0]. The context ID from the command descriptor is identified here.

Hit. The hit flag indicates whether the search was successful.

Done. This field indicates that the command has been processed. The done bit is cleared when the Result Register 0 is Read by the network processor. A new command can be initiated by the network processor through this descriptor after the done bit has cleared.

Table 7-16. Result Register 1 (Search Result Bit in Data Field = 0)

ADR	63–0
Result 1	Associative Data[63:0]

Table 7-17. Result Register 1 (Search Result Bit in Data Field = 1)

ADR	63–0	
Result 1	Hit	Associative Data[62:0]

7.3.7 Result Register 0 and 1 for Search Operation (Case 2)

For the search operation where the SSRAM is connected to the network processor (see Figure 13-1), the Result Register 0 carries the search response (see Table 7-18) and result register 1 is unused.

Table 7-18. Search Response in Result Register 0 (type I)

Bit Positions	Associative Data SSRAM connected to Coprocessor Bus							
	7	6	5	4	3	2	1	0
63–56	Reserved							
55–48	Reserved							
47–40	Reserved							
39–32	Reserved		Reserved	Processor ID[4:0]				
31–24	Done	Hit	Reserved	Context ID [4:0]				
23–16	Index [23:16]							
15–8	Index [15:8]							
7–0	Index [7:0]							

Processor ID[4:0]. The processor ID set in the command descriptor is set here.

Context ID[4:0] . The context ID set in the command descriptor is set here.

Hit. The hit flag indicates whether the search was successful.

Done. This field indicates that the command has been processed. The done bit is cleared when the Result Register 0 is Read by the network processor. A new command can be initiated by the network processor through this descriptor after the done bit has cleared.

Index. This field contains index returned by the NSEs where a successful hit was found. This field is valid only if the hit bit in the Result Register 0 is a 1. Table 7-19 below shows the number of index bits for various NSEs. ***Note***. CYNSE70032 and CYNSE70064 bits 23–22 of the index will always be 00. (Refer to the specifications of the CYNSE70XXX for the description of the index returned by the NSEs.)

Table 7-19. Index Bits for NSEs

Device	SAP	SEID	Index
CYNSE70032	21:19	18:14	13:0
CYNSE70064	21:20	19:15	14:0
CYNSE70128	23:21	20:16	15:0

Note. SAP is the SSRAM Address (SADR) Prefix. These bits are passed along with the command descriptor word in the SAP field.

7.3.8 Functional Overview of Context Descriptor

The network processor(s) can Write up to 32 contexts. There can be up to 32 operations in flight through the database coprocessing subsystem. If 30 descriptor entries are in use, the NDC will issue the DESC_AFUL signal to inform that command descriptor ring is almost full. The database coprocessor continually executes the commands posted in the descriptors. The commands are executed and the results written in the Result Registers 0 and 1 of the corresponding descriptor entries. The network processor(s) will Read the results and free the descriptor entry for another command.

The handshake for the command handoff from the network processor uses the start bit in the command descriptor. The network processor will load the command and the associative parameter along with the start bit in the descriptors. As the start bit in a descriptor is set, the NDC will take the command and insert it in the pipeline queue for execution. The commands in the pipeline queue are strictly handled in a first-in, first-out manner. ***Note***. The network processor must make sure that the start bit is set in the last access to the descriptor to complete the command.

The commands from the pipeline queue are continually executed by the NDC and the results are loaded back to the command initiating descriptor's Result Registers 0 and 1. The handshake for the results from the NDC back to network processor is done through any of the following mechanisms:

- Done bit
- CPID bus, STRB signal.

In the first method, after the network processor has issued a command to the NDC, the network processor will continually poll that command descriptor entry for the done bit. Once done bit is set, it signals to the network processor that the results are Ready in Results Registers 0 and 1 for Readout. Reading of these registers by the network processor will clear the done bit. This descriptor entry is free and may now be used for another command.

In the second method, the network processor uses the interrupt mechanism for Reading the command results. After the results are Ready in Result Registers 0 and 1 and the done bit is set, the NDC will assert pins CPID[7:0] (with the concatenated processor and context ID information) and activate the STRB signal for one CLK cycle. This STRB signal interrupts and the CPID identifies the context and/or processor for which the result are Ready. The context within that processor can wake up and Read the results (Result Register 0 and 1) from the appropriate descriptor. Reading of these registers by the network processor will reset the done bit. This descriptor entry is free and may now be used for another command.

8.0 NDC Subsystem Powerup Initialization Procedure

On power up (boot), the network processor will apply the following sequence of operations.

1. Write SRST and CFG information to 1 in the CFG register.
2. Wait at least 32 cycles, then poll on SRST.
3. Write the CFG registers to each of the NSEs, starting with the one residing at the least significant address.
4. Write the CFG registers of the last NSE in the depth-cascaded system, setting the LDEV and LRAM bits to a 1.
5. The descriptor block is now Ready for use by the network processor(s) for building, managing, and/or searching the database.

Hardware Interface Timing Protocols—NDC Interface. The network processor interface of the NDC supports a variety of SSRAM interfaces. It supports both SyncBurst as well as ZBT SSRAMs. IFC_CFG[2:0] pins select the interface type for the device as follows. (Refer to SSRAM specifications and application notes from such vendors as IDT and Micron.)

000: ZBT pipelined mode

001: ZBT flowthrough mode

010: SyncBurst pipelined mode (early Write)

011: SyncBurst pipelined mode (late Write)

100–111: Reserved.

9.0 ZBT Pipelined SSRAM Interface Mode

The ADR and control signals (R/W_L, BW_L[7:0], CE_L, CE2, CE2_L) are sampled on a CLK edge. For Write cycles, the data is sampled two cycles later; for Read cycles, the data is available to the processor two cycles later. Both Write- and Read-cycle latency is two cycles and there is no gap required between Read and Write operations. Every cycle is available for the network processor(s) for full utilization of the bus bandwidth. See Figure 9-1. ***Note***. BWE_L is not used in this mode and should be tied inactive.

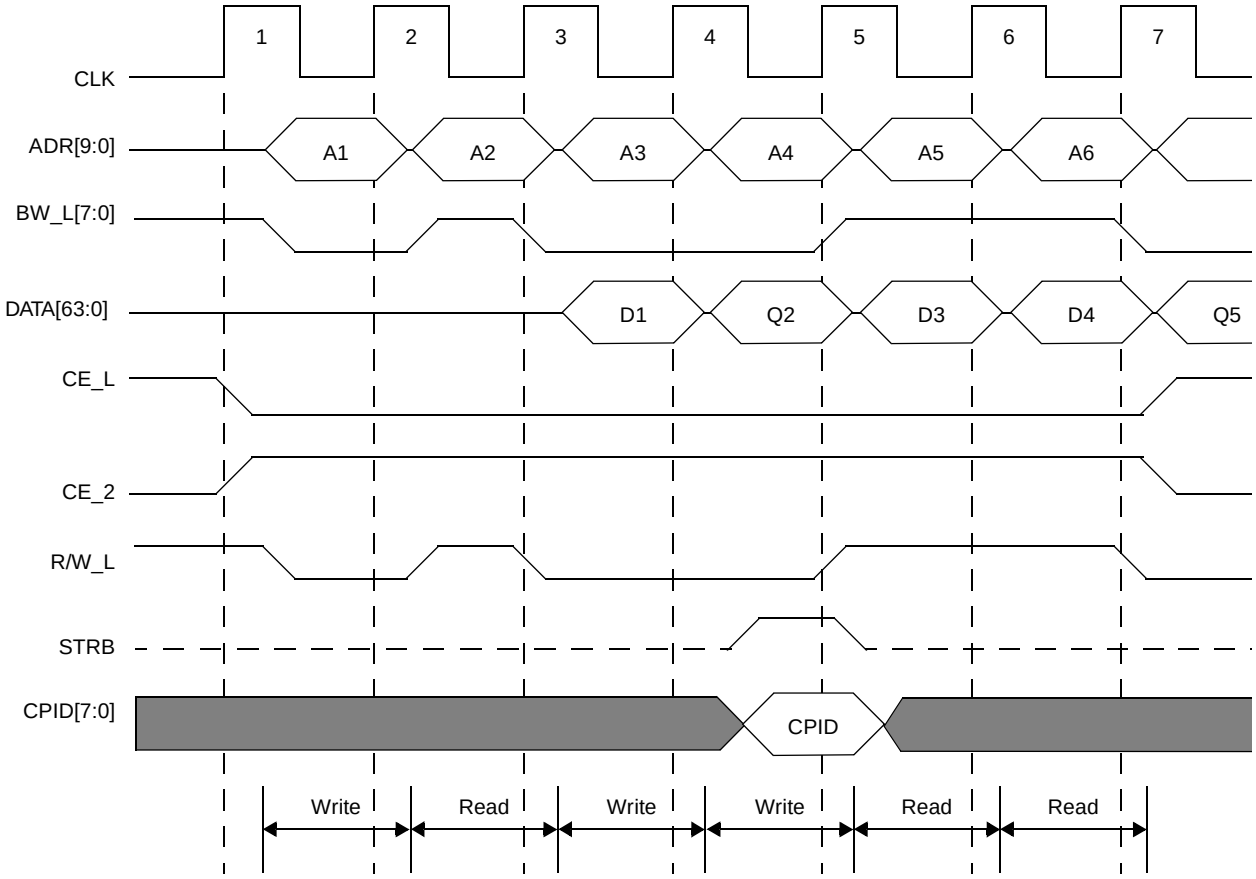


Figure 9-1. ZBT Pipelined SRAM Interface (Mode 000)

10.0 ZBT flowthrough SSRAM Interface Mode

The ADR and control signals (R/W_L, BW_L[7:0], CE_L, CE2, CE2_L) are sampled on a CLK edge. For Write cycles, the data is sampled one cycle later; for Read cycles, the data is available to the processor one cycle later. Both Write- and Read-cycle latency is one cycle, and there is no gap required between Read and Write operation. Every cycle is available for the network processor(s) for full utilization of the bus bandwidth. See Figure 10-1. ***Note***. BWE_L is not used in this mode and should be tied inactive.

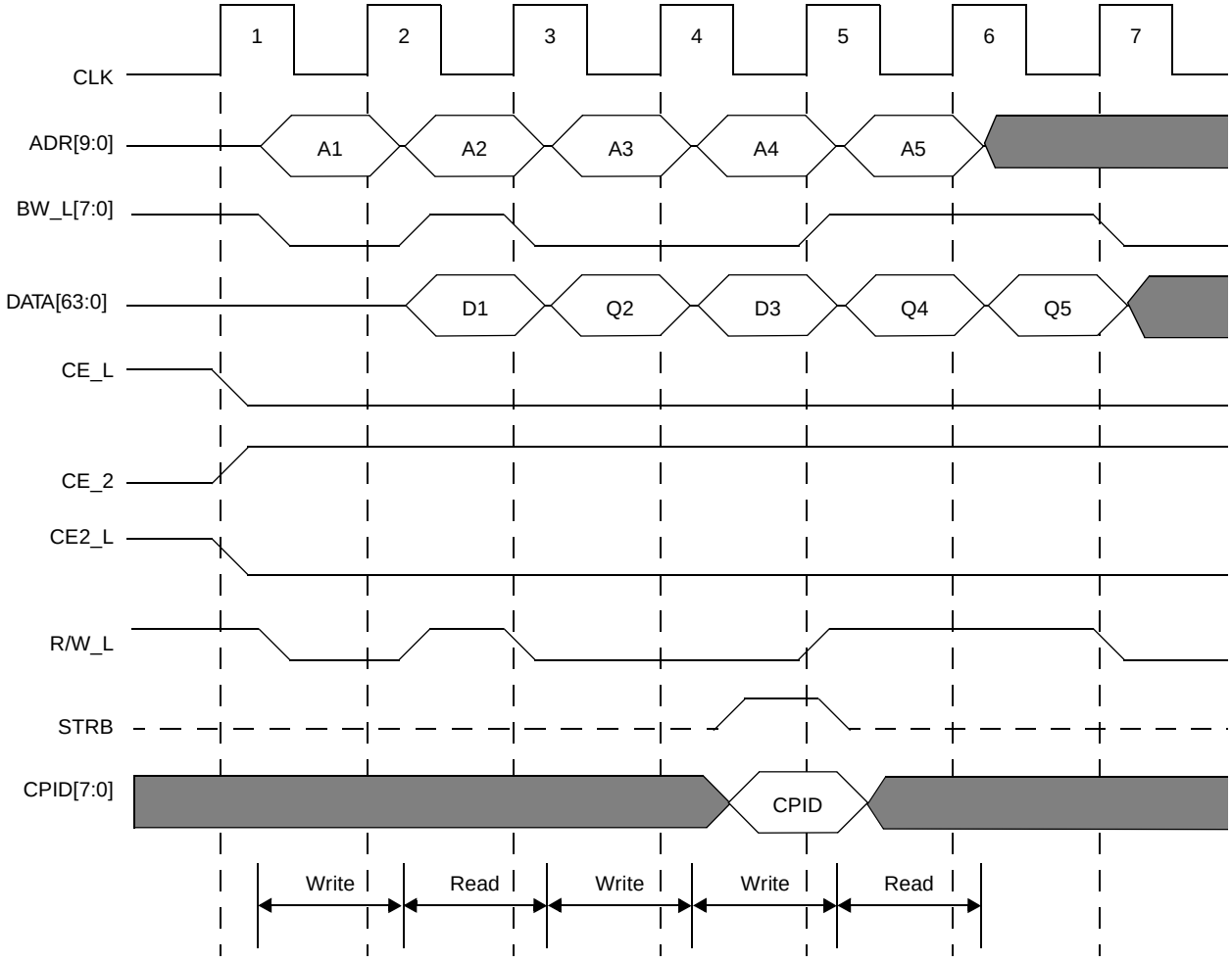


Figure 10-1. ZBT Flowthrough SSRAM Interface (Mode 001)

11.0 SyncBurst Pipelined SSRAM Interface (Early Write)

The ADR and control signals (R/W_L, BW_L[7:0], CE_L, CE2, CE2_L) are sampled on a CLK edge. For Write cycles, the data is sampled one cycle later; for Read cycles, the data is available to the processor one cycle later. Both Write- and Read-cycle latency is one cycle, and there is no gap required between Read and Write operation. Every cycle is available for the network processor(s) for full utilization of the bus bandwidth. See Figure 11-1. ***Note***. BWE_L is not used in this mode and should be tied inactive.

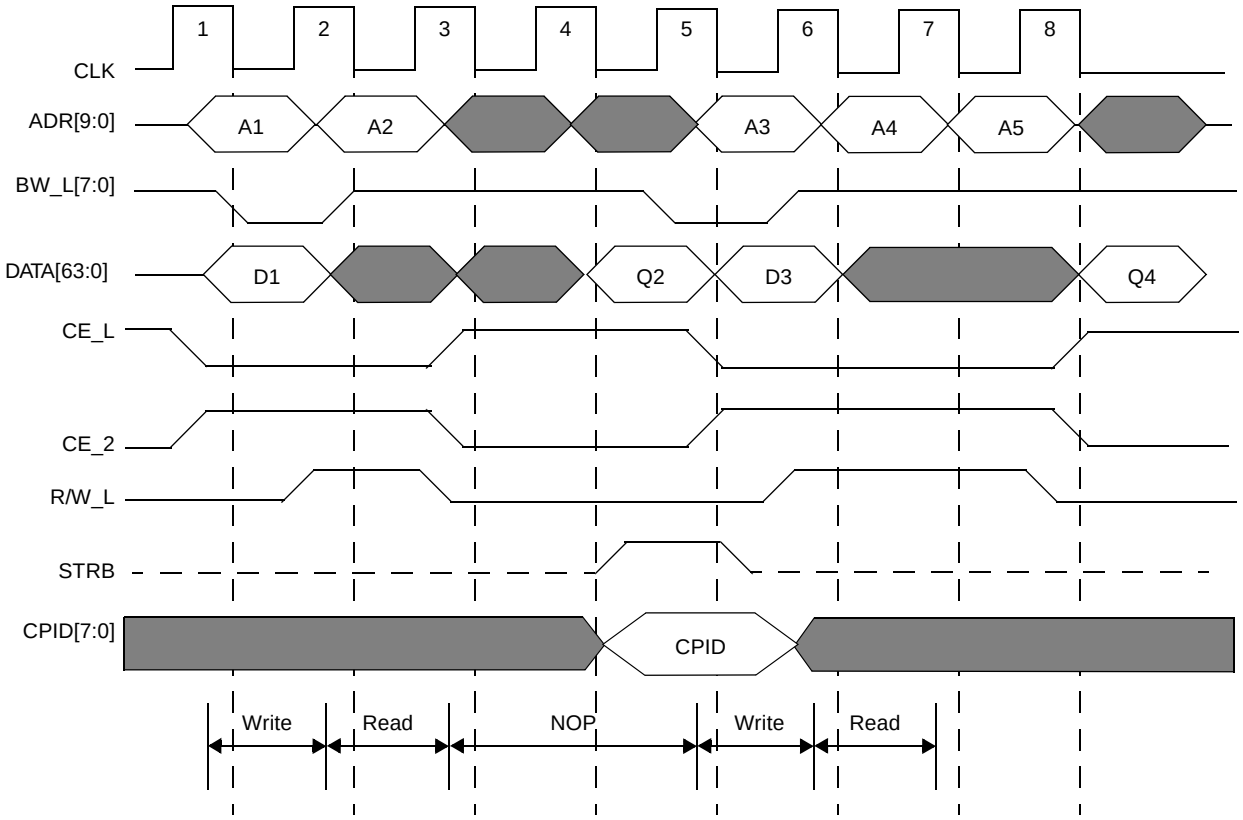


Figure 11-1. SyncBurst Pipelined SSRAM Interface (Early Write)

12.0 SyncBurst Pipelined SSRAM Interface Mode (Late Write)

The ADR and control signals (R/W_L, BW_L[7:0], CE_L, CE2, CE2_L) are sampled on a CLK edge. For Write cycles, the data is sampled one cycle later; for Read cycles, the data is available to the processor one cycle later. Both Write- and Read-cycle latency is one cycle, and there is no gap required between Read and Write operation. Every cycle is available for the network processor(s) for full utilization of the bus bandwidth. See Figure 12-1. ***Note***. BWE_L is not used in this mode and should be tied inactive.

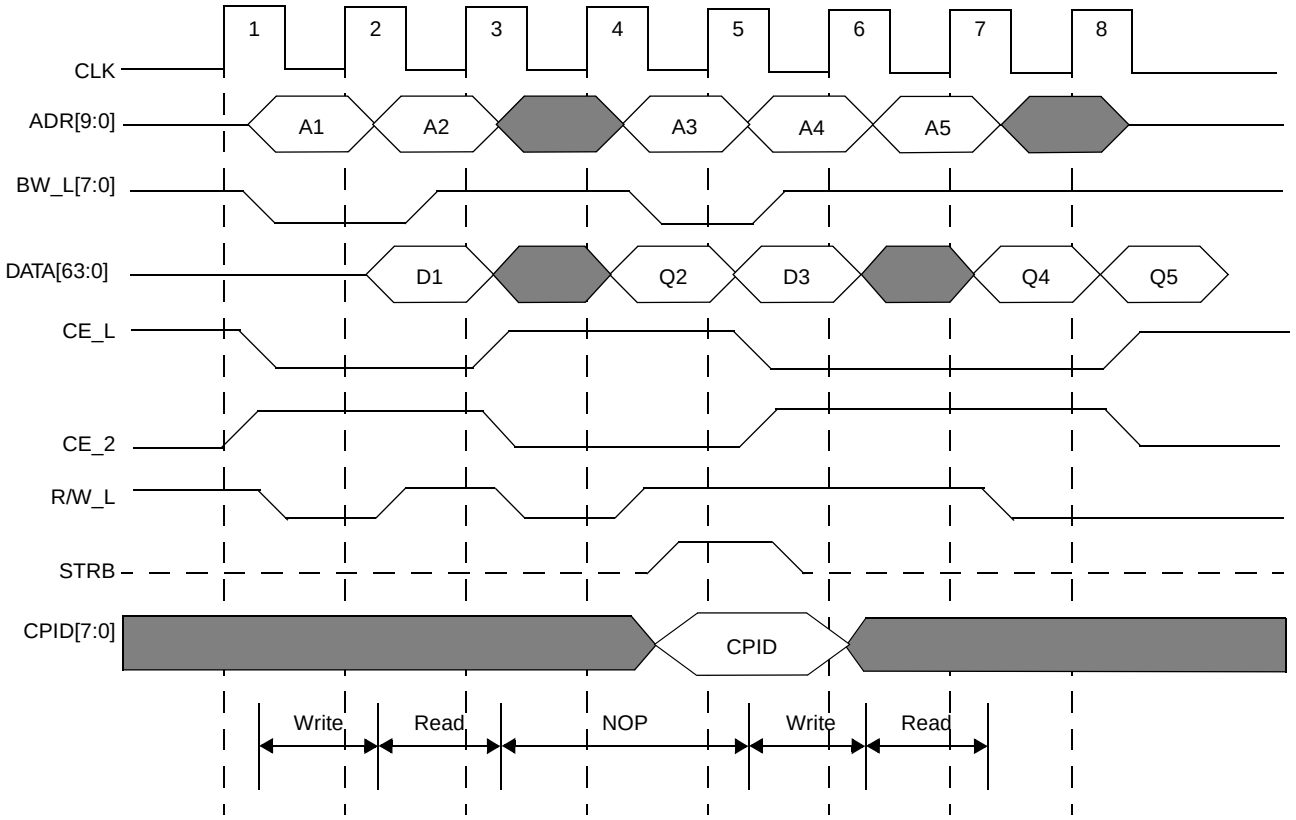


Figure 12-1. SyncBurst Pipelined SSRAM Interface (Late Write)

13.0 Application Information

There are two ways to build a database coprocessing subsystem using CYNPC80192, CYNSE70XXX, and SSRAMs. In the first system the associative data SSRAMs are connected to the coprocessor and the NSE (Figure 13-1) and the coprocessor returns the associated data in response to a search operation. This type of implementation is suited to applications where the associative data size is up to eight bytes.

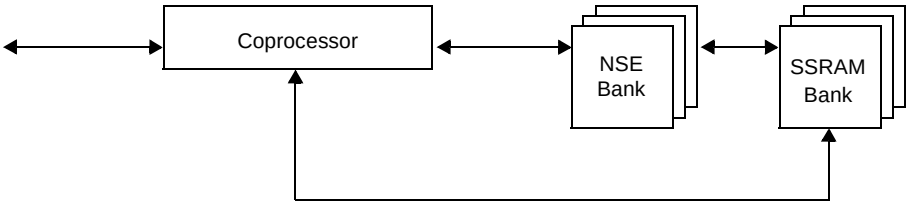


Figure 13-1. Configuration 1—Associative SSRAM Mode

In the second system, the coprocessor returns the index of the successful search entry. The network processor uses the index as the page offset to access the associative data from SSRAM directly (see Figure 13-2). This implementation is suited to applications where the associative data size is longer than eight bytes.

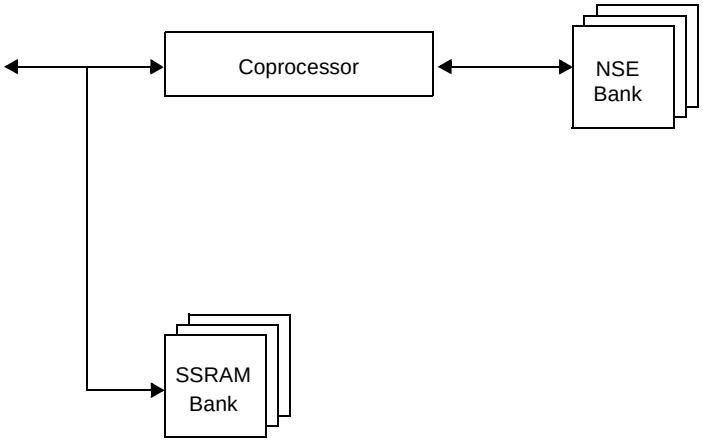


Figure 13-2. Configuration 2—Index Mode

Single or multiple network processors with the arbitration to the SRAM interface can access the database coprocessing subsystem to implement a parallel packet processing system, as shown in Figure 13-3.

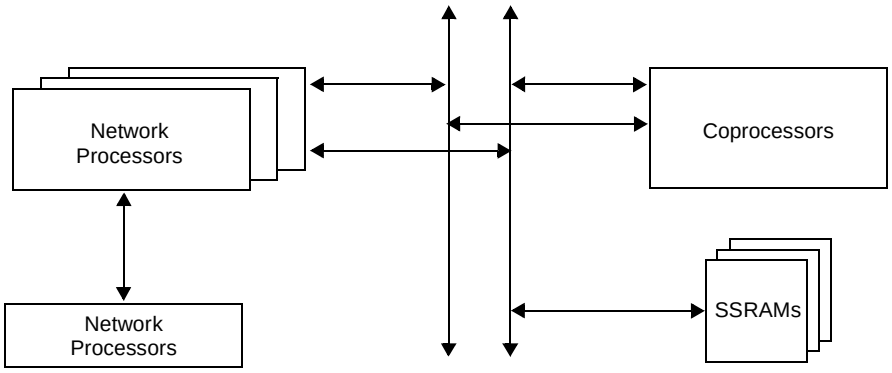


Figure 13-3. Switching Systems Block Diagram

14.0 Information on External Transceivers

As more NSEs are added to the DQ bus, the capacitive load on the bus increases, reducing the bus speed. CYNSE80192 gets around this by using external transceivers, and provides a glueless support to add the transceivers (Phillips 74ALVT16652) between a bank of NSEs and the CYNPC80192 (see Figure 14-1).

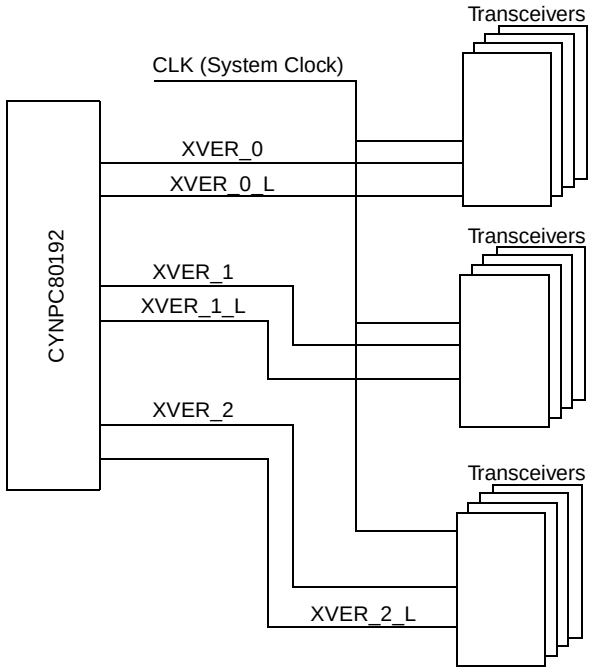


Figure 14-1. Use of Transceiver Enables

The XVER_0, XVER_1, and XVER_2 are electrically buffered versions of the same logical signal in the CYNPC80192 device. The XVER_0_L, XVER_1_L, and XVER_2_L are also electrically buffered versions of the same logical signal in the CYNPC80192 device. Multiple copies of these signals are provided in order to increase the ability of the signal to drive many transceiver devices of eight-bit width. Figure 14-2 shows one example of the distribution of signals driving the transceivers.

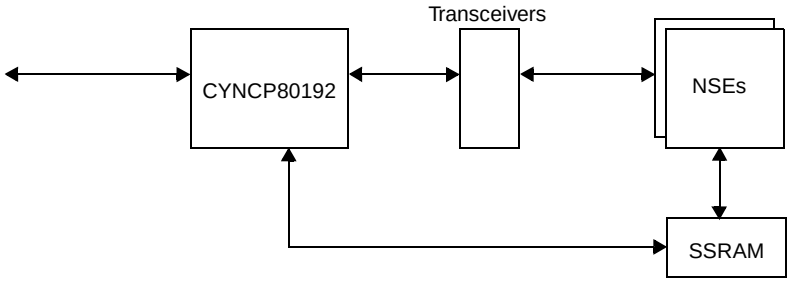


Figure 14-2. Transceiver Connected Between CYNPC80192 and CYNSE70XXX Devices

15.0 JTAG (1149.1) Testing

The CYNPC80192 supports the Test Access Port and Boundary Scan Architecture as specified in the IEEE JTAG Standard 1149.1. The pin interface to the chip consists of five signals with the standard definitions: TCK, TMS, TDI, TDO, and TRST_L. Table 15-1 and Table 15-2 describe the operations that the test access port controller supports and the test access port device ID register.

Table 15-1. Test Access Port Controller Instructions

Instruction	Type	Description
SAMPLE/PRELOAD	Mandatory	***Sample/Preload***. Loads the values of signals going to and from I/O pins into the boundary scan shift register to provide a snap-shot of the normal functional operation.
EXTEST	Mandatory	***External Test***. Uses boundary scan values shifted in from TAP to test connectivity external to the device.
INTEST	Optional	***Internal Test***. Allows slow-speed functional testing of the device using the boundary scan register to provide the I/O values.

Table 15-2. Test Access Port Device ID Register

Field	Range	Initial Value	Description
Revision	[31:28]	0001	***Revision Number***. This is the current device revision number. Numbers start from one and increment by one for each revision of the device.
Part Number	[27:12]	0000 0000 0000 0011	This is the part number for this device.
MFID	[11:1]	000_1101_1100	***Manufacturer ID***. This field is the same as the manufacturer ID used in the TAP controller.
LSB	0	1	***Least Significant Bit***.

16.0 Electrical Characteristics

This section describes the electrical specifications, capacitance, operating conditions, DC characteristics, and AC timing parameters for the NDC (see Table 16-1, Table 16-2, Table 16-3, Table 16-4, and Table 16-5).

Table 16-1. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 < V_{IN} < V_{DDQ}$	–10	10	uA
I_{LO}	Output Leakage Current[1]	$0 < V_{OUT} < V_{DDQ}$	–10	10	uA
V_{OL}	Output Low Voltage	8 mA, V_{DDQ} = 3.3V		0.4	V
V_{OH}	Output High Voltage	4 mA, V_{DDQ} = 3.3V	2.4		V
I_{CC}_core	2.5 V Supply Current[2]			TBD	mA
I_{CC}_IO	3.3 V Supply Current			TBD	mA

1. Applies only for outputs in 3-state.
2. Average operating current at maximum frequency. Transient peak currents may exceed these values.

Table 16-2. Capacitance

Symbol	Parameter	Max	Unit
C_{IN}	Input Capacitance	TBD	pF[1]
C_{OUT}	Output Capacitance	TBD	pF[2]

1. f = 1 MHz, V_{IN} = 0V.
2. f = 1 MHz, V_{OUT} - 0V.

Table 16-3. Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{DDQ}	Operating Voltage for IO	3.14	3.45	V
V_{DD}	Operating Supply Voltage	2.37	2.63	V
V_{IH}	Input High Voltage[1]	2.0	V_{DD}+0.3	V
V_{IL}	Input Low Voltage[2]	–0.3	0.8	V
T_A	Ambient Operating Temperature	0	70	ºC
	Supply Voltage Tolerance	–5%	+5%	

1. Maximum allowable applies to overshoot only (V_{DDQ} is 3.3V supply).
2. Minimum allowable applies to undershoot only.

Table 16-4. AC Timing Parameters for Pipelined ZBT SSRAM and SyncBurst SSRAM

Row	Description	Symbol	CYNPC80192 –100		CYNPC80192 –83		Unit	Test Conditions
			Min	Max	Min	Max		Load (pF)
1	CLK period: max frequency	T_{CLK}		100		83	MHz	
2	CLK high pulse; worst-case 40%–60% duty cycle[1]	T_{CKHI}	4.0		4.8		ns	
3	CLK low pulse; worst-case 40%–60% duty cycle[1]	T_{CKLO}	4.0		4.8		ns	
4	Setup Time to CLK rising edge[2]	T_{SA}	2.5		3.0		ns	
5	Hold Time to CLK rising edge[3]	T_{HA}	1.5		1.5		ns	
6	Clock to output valid (Network Processor Interface)	T_{CKOV}		8.0		9.0	ns	30
7	Clock to CLK2X delay	T_{CK2X}		3.5		4.0	ns	
8	Clock to PHS_L delay	$T_{CLKPHSL}$		6		7	Ns	
9	Clock to output valid (NSE Interface)	T_{CKSE}		9		11	ns	40
10	Clock to SCLK delay	T_{SCK}		5		6	ns	
11	Clock to output valid (SDATA)	T_{CKSD}		10		12	ns	20
12	Clock to output in Low-Z	T_{CKOLZ}	3		3		ns	
13	Clock to output in High-Z	T_{CKOHZ}		6		7	ns	

1. T_{CLKHI} and T_{CLKO} duty cycle values are based on 20–80% signal levels.
2. Set-up time for ADR, CLK enable, data, Read/Write, CE, and byte Write enable.
3. Hold time for ADR, CLK enable, data, Read/Write, CE, and byte Write enable.

Table 16-5. AC Timing Parameters for ZBT and flowthrough SSRAM

Row	Description	Symbol	CYNPC80192–83		Unit	Test Conditions Load (pF)
			Min	Max		
1	CLK period: max frequency	T_{CLK}		50	MHz	
2	CLK high pulse; worst-case 40%–60% duty cycle	T_{CKHI}	8		ns	
3	CLK low pulse; worst-case 40%–60% duty cycle	T_{CKLO}	8		ns	
4	Address setup time to CLK rising edge	T_{SA}	6		ns	
5	Address hold time to CLK rising edge	T_{HA}	2		ns	
6	Clock to output valid (network processor interface)	T_{CKOV}		18	ns	30
7	Clock to CLK2X delay	T_{CLK2}		4	ns	
8	Clock to PHS_L delay	$T_{CLKPHSL}$		7	ns	
9	Clock to output valid (NSE Interface)	T_{CKSE}		12	ns	40
10	Clock to SCLK delay	T_{SCK}		6	ns	
11	Clock to output valid (SDATA)	T_{CKSD}		13	ns	20
12	Clock to output in low-Z	T_{CKOLZ}	3		ns	
13	Clock to output in high-Z	T_{CKOHZ}		7	ns	

	AF	AE	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	Data 2	DATA5	DATA6	DATA9	Data 12	Data 15	Data 18	Data 21	Data 23	Data 26	BW_L6	BW_L3	BW_L2	BW_L1	ADR1	ADR4	ADR7	CE2	RW_L	BWE_L	Data 30	Data 33	Data 36	Data 39	DATA42	DATA43	1
2	STRB	Data 1	Data 3	DATA7	Data 10	Data 13	Data 16	Data 19	Data 22	Data 25	BW_L7	BW_L4	CLK	BW_L0	ADR2	ADR5	ADR8	CE_L	OE_L	Data 29	Data 32	Data 35	Data 38	DATA41	GND	DATA44	2
3	CBID1	CPID0	Data 0	DATA4	DATA8	Data 11	Data 14	Data 17	Data 20	Data 24	Data 27	BW_L5	XVER_2_L	ADR0	ADR3	ADR6	ADR9	CE2_L	Data 28	Data 31	Data 34	Data 37	DATA40	GND	DATA45	DATA47	3
4	BIG_LTL_L	CPID2	IRST_L	GND	VDD	VDD	VDD	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	GND	GND	VDDQ	VDDQ	VDDQ	VDDQ	VDD	VDD	VDD	VDD	GND	DATA46	DATA48	DATA50]	4
5	CPID4	IFC_CFG0	IWIDTH	VDD																			VDD	DATA49	DATA51	DATA58	5
6	IFC_CFG2	CPID5	CPID3	VDD																			VDD	DATA52	DATA54	DATA56	6
7	TCK	TDI	IFC_CFG1	VDD																			VDD	DATA55	DATA57	DATA59	7
8	CPID7	CPID6	TMS	VDDQ																			VDDQ	DATA58	DATA60	DATA61	8
9	DESC_AFULL	CAM_FULL	TRST_L	VDDQ																			VDDQ	DATA62	DATA63	INTR	9
10	TDO	CLK2X	PHS_L	VDDQ																			VDDQ	SCANE	SCANM	TESTM	10
11	CMD1	CMD0	ORST_L	VDDQ							VDD	VDD	GND	GND	VDD	VDD							VDDQ	XVER_2	XVER_1_L	XVER_1	11
12	CMD4	CMD3	CMD2	VDDQ							VDD	GND	GND	GND	GND	VDD							VDDQ	DQ_72	SCLK	SOE_L	12
13	CMD7	CMD6	CMD5	GND							GND	GND	GND	GND	GND	GND							GND	SDATA63	SDATA62	SDATA61	13
14	CMD8	CMDV	DQ0	GND							GND	GND	GND	GND	GND	GND							GND	SDATA58	SDATA59	SDATA60	14
15	DQ1	DQ2	DQ3	VDDQ							VDD	GND	GND	GND	GND	VDD							VDDQ	SDATA55	SDATA56	SDATA57	15
16	DQ4	DQ5	DQ6	VDDQ							VDD	VDD	GND	GND	VDD	VDD							VDDQ	SDATA52	SDATA53	SDATA54	16
17	DQ7	DQ8	DQ9	VDDQ																			VDDQ	SDATA49	SDATA50	SDATA51	17
18	DQ10	DQ11	DQ12	VDDQ																			VDDQ	SDATA45	SDATA47	SDATA48	18
19	DQ13	DQ14	DQ16	VDDQ																			VDDQ	SDATA42	SDATA44	SDATA46	19
20	DQ15	DQ17	DQ19	VDD																			VDD	SData 39	SDATA41	SDATA43	20
21	DQ18	DQ20	DQ22	VDD																			VDD	SData 36	SData 38	SDATA40	21
22	DQ21	DQ23	DQ25	VDD																			VDD	SData 33	SData 35	SData 37	22
23	DQ24	XVER_0	DQ26	GND	VDD	VDD	VDD	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	GND	GND	VDDQ	VDDQ	VDDQ	VDDQ	VDD	VDD	VDD	VDD	GND	SData 28	SData 32	SData 34	23
24	XVER_0_L	DQ27	DQ29	DQ32	DQ37	FULL	DQ42	SSV	DQ47	DQ50	DQ53	DQ55	DQ58	DQ61	DQ65	SData 0	SData 3	SDATA6	SData 10	SData 13	SData 16	SData 19	SData 22	SData 25	SData 29	SData 31	24
25	DQ28	DQ30	DQ33	DQ36	DQ39	DQ41	DQ44	DQ46	DQ49	DQ51	DQ54	DQ56	DQ59	DQ62	DQ64	DQ67	SData 2	SDATA5	SDATA8	SData 11	SData 14	SData 17	SData 20	SData 23	SData 26	SData 30	25
26	DQ31	DQ34	DQ35	DQ38	DQ40	DQ43	DQ45	DQ48	SSF	DQ52	EOT	DQ57	ACK	DQ60	DQ63	DQ66	SData 1	SDATA4	SDATA7	SDATA9	SData 12	SData 15	SData 18	SData 21	SData 24	SData 27	26
	AF	AE	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Figure 16-1. Pinout Diagram

Table 16-6 contains an alphabetical listing of the pins marked out in Figure 16-1, above.

Table 16-6. CYNPC80192 Pinout Description

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
A1	DATA[43]	I/O	AB1	DATA[12]	I/O
A10	TESTM	Input	AB2	DATA[10]	I/O
A11	XVER_1	Output	AB23	V_{DD}	2.5 Volts
A12	SOE_L	Input	AB24	DQ[37]	I/O
A13	SDATA[61]	I/O	AB25	DQ[39]	I/O
A14	SDATA[60]	I/O	AB26	DQ[40]	I/O
A15	SDATA[57]	I/O	AB3	DATA[08]	I/O
A16	SDATA[54]	I/O	AB4	V_{DD}	2.5 Volts
A17	SDATA[51]	I/O	AC1	DATA[09]	I/O
A18	SDATA[48]	I/O	AC10	V_{DDQ}	3.3 Volts
A19	SDATA[46]	I/O	AC11	V_{DDQ}	3.3 Volts
A2	DATA[44]	I/O	AC12	V_{DDQ}	3.3 Volts
A20	SDATA[43]	I/O	AC13	V_{SS}	Ground
A21	SDATA[40]	I/O	AC14	V_{SS}	Ground
A22	SDATA[37]	I/O	AC15	V_{DDQ}	3.3 Volts
A23	SDATA[34]	I/O	AC16	V_{DDQ}	3.3 Volts
A24	SDATA[31]	I/O	AC17	V_{DDQ}	3.3 Volts
A25	SDATA[30]	I/O	AC18	V_{DDQ}	3.3 Volts
A26	SDATA[27]	I/O	AC19	V_{DDQ}	3.3 Volts
A3	DATA[47]	I/O	AC2	DATA[07]	I/O
A4	DATA[50]	I/O	AC20	V_{DD}	2.5 Volts
A5	DATA[53]	I/O	AC21	V_{DD}	2.5 Volts
A6	DATA[56]	I/O	AC22	V_{DD}	2.5 Volts
A7	DATA[59]	I/O	AC23	V_{SS}	Ground
A8	DATA[61]	I/O	AC24	DQ[32]	I/O
A9	INTR	Output	AC25	DQ[36]	I/O
AA1	DATA[15]	I/O	AC26	DQ[38]	I/O
AA2	DATA[13]	I/O	AC3	DATA[04]	I/O
AA23	V_{DD}	2.5 Volts	AC4	V_{SS}	Ground
AA24	FULL	Input	AC5	V_{DD}	2.5 Volts
AA25	DQ[41]	I/O	AC6	V_{DD}	2.5 Volts
AA26	DQ[43]	I/O	AC7	V_{DD}	2.5 Volts
AA3	DATA[11]	I/O	AC8	V_{DDQ}	3.3 Volts
AA4	V_{DD}	2.5 Volts	AC9	V_{DDQ}	3.3 Volts
AD1	DATA[06]	I/O	AE19	DQ[14]	I/O

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
AD10	PHS_L	Output	AE2	DATA[01]	I/O
AD11	ORST_L	Output	AE20	DQ[17]	I/O
AD12	CMD[2]	Output	AE21	DQ[20]	I/O
AD13	CMD[5]	Output	AE22	DQ[23]	I/O
AD14	DQ[00]	I/O	AE23	XVER_0	Output
AD15	DQ[03]	I/O	AE24	DQ[27]	I/O
AD16	DQ[06]	I/O	AE25	DQ[30]	I/O
AD17	DQ[09]	I/O	AE26	DQ[34]	I/O
AD18	DQ[12]	I/O	AE3	CPID[0]	Output
AD19	DQ[16]	I/O	AE4	CPID[2]	Output
AD2	DATA[03]	I/O	AE5	IFC_CFG[0]	Input
AD20	DQ[19]	I/O	AE6	CPID[5]	Output
AD21	DQ[22]	I/O	AE7	TDI	Input
AD22	DQ[25]	I/O	AE8	CPID[6]	Output
AD23	DQ[26]	I/O	AE9	CAM_FULL	Ouput
AD24	DQ[29]	I/O	AF1	DATA[02]	I/O
AD25	DQ[33]	I/O	AF10	TDO	Output
AD26	DQ[35]	I/O	AF11	CMD[1]	Output
AD3	DATA[00]	I/O	AF12	CMD[4]	Output
AD4	IRST_L	Input	AF13	CMD[7]	Output
AD5	IWIDTH	Input	AF14	CMD[8]	Output
AD6	CPID[3]	Output	AF15	DQ[01]	I/O
AD7	IFC_CFG[1]	Input	AF16	DQ[4]	I/O
AD8	TMS	Input	AF17	DQ[07]	I/O
AD9	TRST_L	Input	AF18	DQ[10]	I/O
AE1	DATA[05]	I/O	AF19	DQ[13]	I/O
AE10	CLK2X	Output	AF2	STRB	Output
AE11	CMD[0]	Output	AF20	DQ[15]	I/O
AE12	CMD[3]	Output	AF21	DQ[18]	I/O
AE13	CMD[6]	Output	AF22	DQ[21]	I/O
AE14	CMDV	Output	AF23	DQ[24]	I/O
AE15	DQ[02]	I/O	AF24	XVER_0_L	Output
AE16	DQ[05]	I/O	AF25	DQ[28]	I/O
AE17	DQ[08]	I/O	AF26	DQ[31]	I/O
AE18	DQ[11]	I/O	AF3	CPID[1]	Output
AF4	BIG_LTL_L	Input	C13	SDATA[63]	I/O

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
AF5	CPID[4]	Output	C14	SDATA[58]	I/O
AF6	IFC_CFG[2]	Input	C15	SDATA[55]	I/O
AF7	TCK	Input	C16	SDATA[52]	I/O
AF8	CPID[7]	Output	C17	SDATA[49]	I/O
AF9	DESC_AFULL	Output	C18	SDATA[45]	I/O
B1	DATA[42]	I/O	C19	SDATA[42]	I/O
B10	SCANM	Input	C2	DATA[41]	I/O
B11	XVER_1_L	Output	C20	SDATA[39]	I/O
B12	SCLK	Output	C21	SDATA[36]	I/O
B13	SDATA[62]	I/O	C22	SDATA[33]	I/O
B14	SDATA[59]	I/O	C23	SDATA[28]	I/O
B15	SDATA[56]	I/O	C24	SDATA[25]	I/O
B16	SDATA[53]	I/O	C25	SDATA[23]	I/O
B17	SDATA[50]	I/O	C26	SDATA[21]	I/O
B18	SDATA[47]	I/O	C3	V_{SS}	Ground
B19	SDATA[44]	I/O	C4	DATA[46]	I/O
B2	V_{SS}	Ground	C5	DATA[49]	I/O
B20	SDATA[41]	I/O	C6	DATA[52]	I/O
B21	SDATA[38]	I/O	C7	DATA[55]	I/O
B22	SDATA[35]	I/O	C8	DATA[58]	I/O
B23	SDATA[32]	I/O	C9	DATA[62]	I/O
B24	SDATA[29]	I/O	D1	DATA[36]	I/O
B25	SDATA[26]	I/O	D10	V_{DDQ}	3.3 Volts
B26	SDATA[24]	I/O	D11	V_{DDQ}	3.3 Volts
B3	DATA[45]	I/O	D12	V_{DDQ}	3.3 Volts
B4	DATA[48]	I/O	D13	V_{SS}	Ground
B5	DATA[51]	I/O	D14	V_{SS}	Ground
B6	DATA[54]	I/O	D15	V_{DDQ}	3.3 Volts
B7	DATA[57]	I/O	D16	V_{DDQ}	3.3 Volts
B8	DATA[60]	I/O	D17	V_{DDQ}	3.3 Volts
B9	DATA[63]	I/O	D18	V_{DDQ}	3.3 Volts
C1	DATA[39]	I/O	D19	V_{DDQ}	3.3 Volts
C10	SCANE	Input	D2	DATA[38]	I/O
C11	XVER_2	Output	D20	V_{DD}	2.5 Volts
C12	DQ_72	I/O	D21	V_{DD}	2.5 Volts
D22	V_{DD}	2.5 Volts	H1	RW_L	Input

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
D23	V_{SS}	Ground	H2	OE_L	Input
D24	SDATA[22]	I/O	H23	V_{DD}	2.5 Volts
D25	SDATA[20]	I/O	H24	SDATA[10]	I/O
D26	SDATA[18]	I/O	H25	SDATA[08]	I/O
D3	DATA[40]	I/O	H26	SDATA[07]	I/O
D4	V_{SS}	Ground	H3	DATA[28]	I/O
D5	V_{DD}	2.5 Volts	H4	V_{DD}	2.5 Volts
D6	V_{DD}	2.5 Volts	J1	CE2	Input
D7	V_{DD}	2.5 Volts	J2	CE_L	Input
D8	V_{DDQ}	3.3 Volts	J23	V_{DDQ}	3.3 Volts
D9	V_{DDQ}	3.3 Volts	J24	SDATA[06]	I/O
E1	DATA[33]	I/O	J25	SDATA[05]	I/O
E2	DATA[35]	I/O	J26	SDATA[04]	I/O
E23	V_{DD}	2.5 Volts	J3	CE2_L	Input
E24	SDATA[19]	I/O	J4	V_{DDQ}	3.3 Volts
E25	SDATA[17]	I/O	K1	ADR[7]	Input
E26	SDATA[15]	I/O	K2	ADR[8]	Input
E3	DATA[37]	I/O	K23	V_{DDQ}	3.3 Volts
E4	V_{DD}	2.5 Volts	K24	SDATA[03]	I/O
F1	DATA[30]	I/O	K25	SDATA[02]	I/O
F2	DATA[32]	I/O	K26	SDATA[01]	I/O
F23	V_{DD}	2.5 Volts	K3	ADR[9]	Input
F24	SDATA[16]	I/O	K4	V_{DDQ}	3.3 Volts
F25	SDATA[14]	I/O	L1	ADR[4]	Input
F26	SDATA[12]	I/O	L11	V_{DD}	2.5 Volts
F3	DATA[34]	I/O	L12	V_{DD}	2.5 Volts
F4	V_{DD}	2.5 Volts	L13	V_{SS}	Ground
G1	BWE_L	Input	L14	V_{SS}	Ground
G2	DATA[29]	I/O	L15	V_{DD}	2.5 Volts
G23	V_{DD}	2.5 Volts	L16	V_{DD}	2.5 Volts
G24	SDATA[13]	I/O	L2	ADR[5]	Input
G25	SDATA[11]	I/O	L23	V_{DDQ}	3.3 Volts
G26	SDATA[09]	I/O	L24	SDATA[00]	I/O
G3	DATA[31]	I/O	L25	DQ[67]	I/O
G4	V_{DD}	2.5 Volts	L26	DQ[66]	I/O
L3	ADR[6]	Input	P16	V_{SS}	Ground

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
L4	V_{DDQ}	3.3 Volts	P2	CLK	Input
M1	ADR[1]	Input	P23	V_{SS}	Ground
M11	V_{DD}	2.5 Volts	P24	DQ[58]	I/O
M12	V_{SS}	Ground	P25	DQ[59]	I/O
M13	V_{SS}	Ground	P26	ACK	Input
M14	V_{SS}	Ground	P3	XVER_2_L	Output
M15	V_{SS}	Ground	P4	V_{SS}	Ground
M16	V_{DD}	2.5 Volts	R1	BW_L[3]	Input
M2	ADR[2]	Input	R11	V_{DD}	2.5 Volts
M23	V_{DDQ}	3.3 Volts	R12	V_{SS}	Ground
M24	DQ[65]	I/O	R13	V_{SS}	Ground
M25	DQ[64]	I/O	R14	V_{SS}	Ground
M26	DQ[63]	I/O	R15	V_{SS}	Ground
M3	ADR[3]	Input	R16	V_{DD}	2.5 Volts
M4	V_{DDQ}	3.3 Volts	R2	BW_L[4]	Input
N1	BW_L[1]	Input	R23	V_{DDQ}	3.3 Volts
N11	V_{SS}	Ground	R24	DQ[55]	I/O
N12	V_{SS}	Ground	R25	DQ[56]	I/O
N13	V_{SS}	Ground	R26	DQ[57]	I/O
N14	V_{SS}	Ground	R3	BW_L[5]	Input
N15	V_{SS}	Ground	R4	V_{DDQ}	3.3 Volts
N16	V_{SS}	Ground	T1	BW_L[6]	Input
N2	BW_L[0]	Input	T11	V_{DD}	2.5 Volts
N23	V_{SS}	Ground	T12	V_{DD}	2.5 Volts
N24	DQ[61]	I/O	T13	V_{SS}	Ground
N25	DQ[62]	I/O	T14	V_{SS}	Ground
N26	DQ[60]	I/O	T15	V_{DD}	2.5 Volts
N3	ADR[0]	Input	T16	V_{DD}	2.5 Volts
N4	V_{SS}	Ground	T2	BW_L[7]	Input
P1	BW_L[2]	Input	T23	V_{DDQ}	3.3 Volts
P11	V_{SS}	Ground	T24	DQ[53]	I/O
P12	V_{SS}	Ground	T25	DQ[54]	I/O
P13	V_{SS}	Ground	T26	EOT	Input
P14	V_{SS}	Ground	T3	DATA[27]	I/O
P15	V_{SS}	Ground	T4	V_{DDQ}	3.3 Volts
U1	DATA[26]	I/O	W1	DATA[21]	I/O

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
U2	DATA[25]	I/O	W2	DATA[19]	I/O
U23	V_{DDQ}	3.3 Volts	W23	V_{DDQ}	3.3 Volts
U24	DQ[50]	I/O	W24	SSV	Input
U25	DQ[51]	I/O	W25	DQ[46]	I/O
U26	DQ[52]	I/O	W26	DQ[48]	I/O
U3	DATA[24]	I/O	W3	DATA[17]	I/O
U4	V_{DDQ}	3.3 Volts	W4	V_{DDQ}	3.3 Volts
V1	DATA[23]	I/O	Y1	DATA[18]	I/O
V2	DATA[22]	I/O	Y2	DATA[16]	I/O
V23	V_{DDQ}	3.3 Volts	Y23	V_{DD}	2.5 Volts
V24	DQ[47]	I/O	Y24	DQ[42]	I/O
V25	DQ[49]	I/O	Y25	DQ[44]	I/O
V26	SSF	Input	Y26	DQ[45]	I/O
V3	DATA[20]	I/O	Y3	DATA[14]	I/O
V4	V_{DDQ}	3.3 Volts	Y4	V_{DD}	2.5 Volts

17.0 Ordering Information

Table 17-1 provides ordering information for the CYNCP80192 device.

Table 17-1. Ordering Information

Part Number	Description	Frequency	Temperature Range
CYNPC80192-100	Network Database Coprocessor	100 MHz	Commercial

18.0 Package Drawings

In the following figures the NDC package diagrams are shown from various views. Figure 18-1 shows the package from a bottom view, Figure 18-2 from a side view, and Figure 18-3 from a top view.

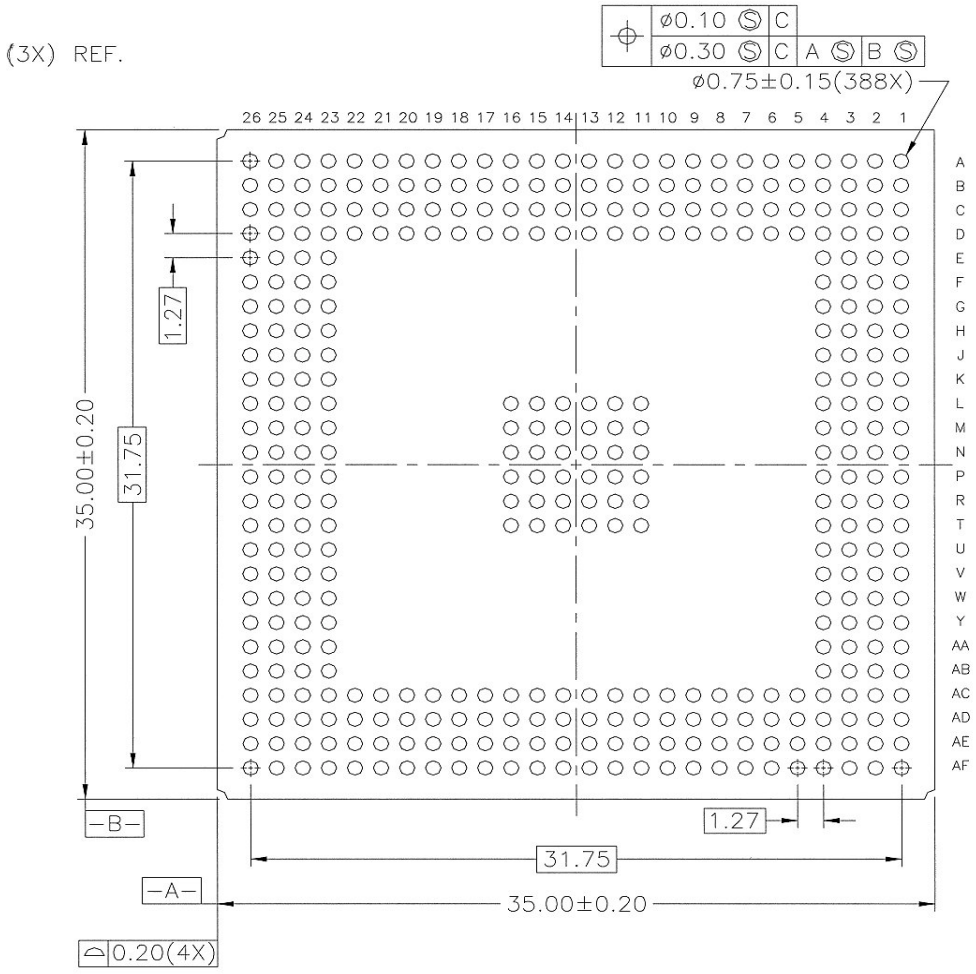


Figure 18-1. Package Bottom View

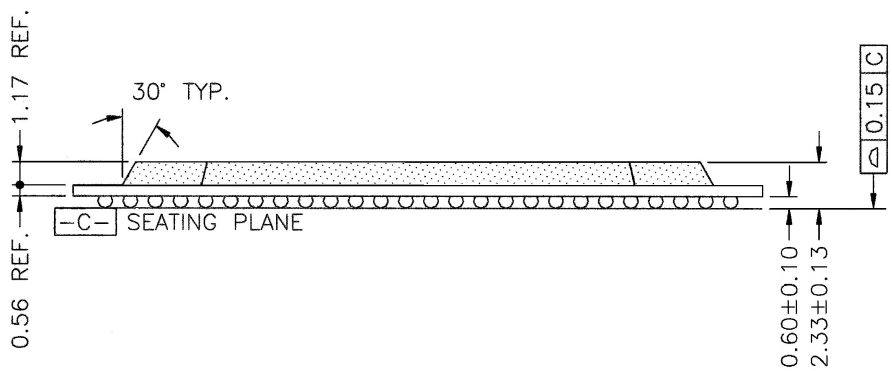


Figure 18-2. Package Side View

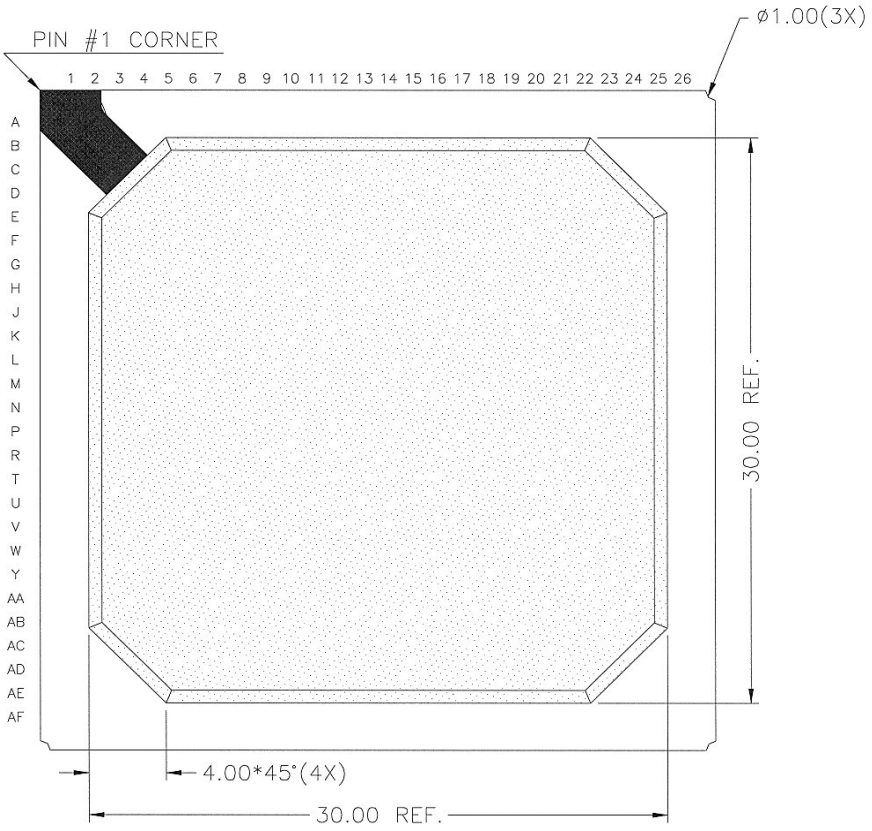


Figure 18-3. Package Top View