SONY

Ultra-High Linearity SP4T Switch

CXM3599UR

Description

The CXM3599UR is a high power and ultra-high linearity SP4T switch for wireless communication systems.
The CXM3599UR can be used for SVLTE and carrier aggregation requiring very high linearity.
This IC has a 1.8 V CMOS compatible decoder.
The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and ultra-high linearity.
(Application: LTE/CDMA/GSM/UMTS Handsets and mini base-stations)

Features

- Low Insertion loss: 0.27 dB (Typ.) (Cellular Band)
  0.45 dB (Typ.) (IMT2000)
- Ultra-high linearity: IMD3 = -104 dBm (Max.), IIP3 = 82 dBm (Min.)
  at LTE Band 13, PTx = +23 dBm, PBlocker = +14 dBm
- Low voltage operation: V_{DD} = 2.5 V
- No DC blocking capacitors required on RF ports
- Small package size: UQFN-20pin (2.5 mm × 2.5 mm)
- Lead-Free and RoHS compliant

Structure

GaAs JPHEMT MMIC switch, CMOS decoder

Moisture Sensitivity

Moisture Sensitivity Level for this part is MSL = 2

Absolute Maximum Ratings

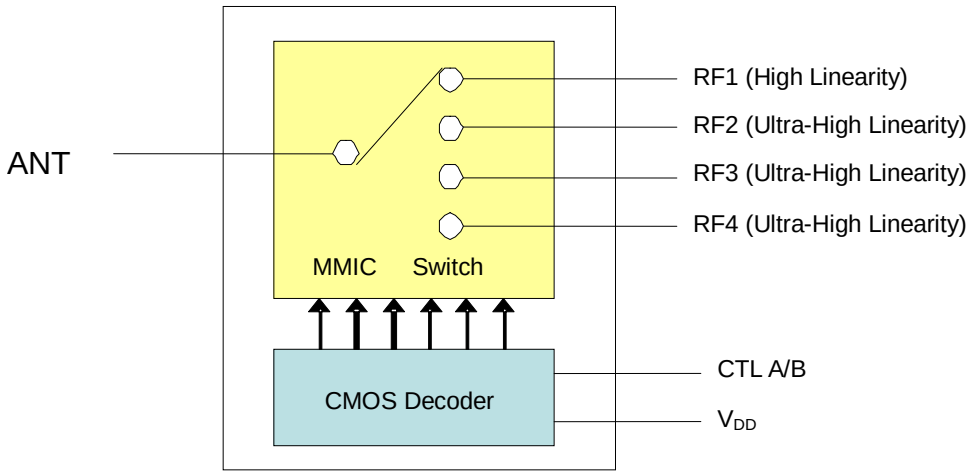
♦ Bias voltage	V_{DD}	4	V	(Ta = 25 ˚C)
♦ Control voltage	Vctl	4	V	(Ta = 25 ˚C)
♦ Maximum input power	—	36	dBm	(Duty cycle = 12.5 to 50 %, Ta = 25 ˚C)
♦ Operating temperature	Topr	–35 to +90	˚C	
♦ Storage temperature	Tstg	–65 to +150	˚C	

This IC is ESD sensitive device. Special handling precautions are required.

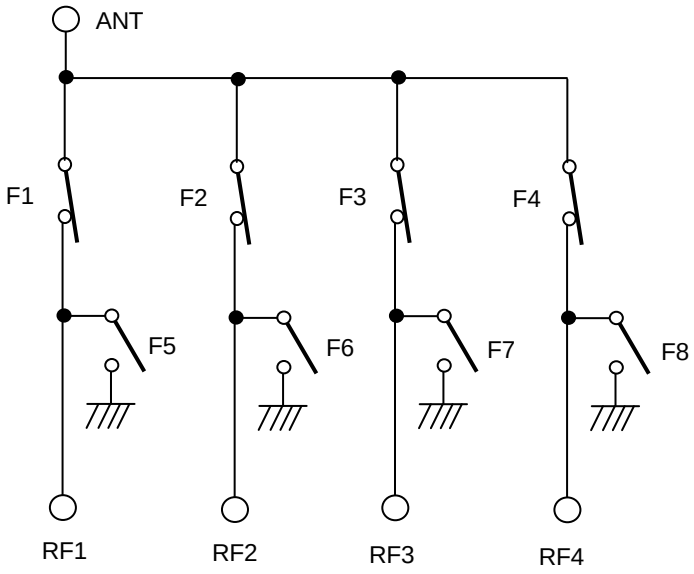
E12609A31

Block Diagram

SP4T Antenna Switch



MMIC Switch

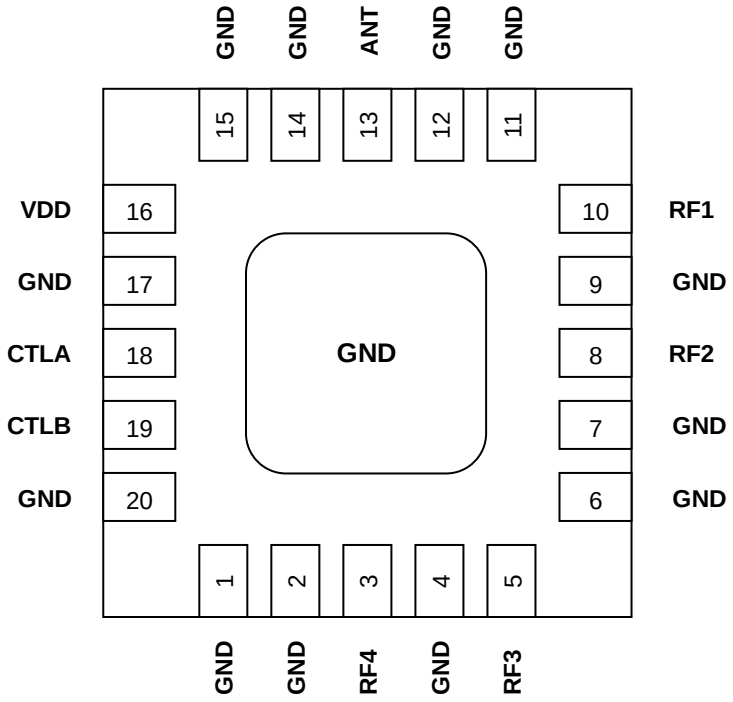


Truth Table

CTLA	CTLB	Active path	F1	F2	F3	F4	F5	F6	F7	F8
L	L	ANT-RF1	ON	OFF	OFF	OFF	OFF	ON	ON	ON
H	L	ANT-RF2	OFF	ON	OFF	OFF	ON	OFF	ON	ON
L	H	ANT-RF3	OFF	OFF	ON	OFF	ON	ON	OFF	ON
H	H	ANT-RF4	OFF	OFF	OFF	ON	ON	ON	ON	OFF

Pin Configuration

UQFN-20P PKG(2.5m x 2.5mm)
(Top View)



DC Bias Condition

Parameter	Min.	Typ.	Max.	Unit
V_{DD}	2.5	2.7	3.3	V
Vctl (H)	1.35	1.8	3.3	
Vctl (L)	0	—	0.45	

Electrical Characteristics

(Ta = 25 °C, V_{DD} = 2.5 V, Vctl = 0/1.8 V)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	ANT-RF1	*1, *2, *6, *8	—	0.32	0.42	dB
			*3, *7, *9	—	0.60	0.75	
			*4	—	0.65	0.80	
		ANT-RF2,RF3, RF4	*1, *2, *6, *8	—	0.27	0.37	
			*3, *4, *7, *9	—	0.45	0.60	
			*5	—	0.50	0.65	
Isolation	ISO.	RF1-RF2,RF3, RF4 (RF1 Active)	*1, *2, *6, *8	37	42	—	dB
			*7	33	35	—	
			*3,*4,*9	28	33	—	
		RF2-RF1,RF3, RF4 (RF2 Active)	*1, *2, *6, *8	36	41	—	
			*3, *4, *7, *9	27	32	—	
			*5	25	30	—	
		RF3-RF1,RF2, RF4 (RF3 Active)	*1, *2, *6, *8	33	38	—	
			*3, *4, *7, *9	25	30	—	
			*5	22	27	—	
		RF4-RF1,RF2, RF3 (RF4 Active)	*1, *2, *6, *8	30	35	—	
			*3, *4, *7, *9	22	27	—	
			*5	20	25	—	
VSWR	VSWR	ANT-RF1	704 to 2170 MHz	—	—	1.8	—
		ANT-RF2,RF3, RF4	704 to 2690 MHz	—	—	1.7	
Harmonics	2fo	ANT-RF1	*6	—	-55	-41	dBm
	3fo			—	-53	-41	
	2fo		*7	—	-63	-50	
	3fo			—	-62	-50	
	2fo		*2, *3	—	-73	-60	
	3fo			—	-80	-60	
	2fo	ANT-RF2,RF3, RF4	*6	—	-60	-45	
	3fo			—	-64	-45	
	2fo		*7	—	-67	-55	
	3fo			—	-68	-55	
	2fo		*2,*3,*5	—	-80	-65	
	3fo			—	-86	-65	
	2fo		*1	—	-82	-78	
Inter modulation distortion in Rx Band	IMD2	ANT-RF1	*10, *11, *12, *15, *16, *19, *20, *23, *24	—	—	-105	dBm
	IMD3		*10, *13, *14, *17, *18, *21, *22, *25, *26	—	—	-105	

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Inter modulation distortion in Rx Band	IMD2	ANT-RF2,RF3, RF4	*10, *11, *12, *15, *16, *19 ,*20, *23, *24	—	—	-110	dBm
	IMD3		*10, *13, *14, *17, *18, *21, *22, *25, *26	—	—	-110	
			*10, *27	—	—	-104	
			*10, *28	—	—	-110	
			*10, *29	—	—	-111	
Switching speed	Ts	ANT-RF1	50 % Ctl to 90 % RF	—	6	9	µs
		ANT-RF2,RF3, RF4		—	9	13	
Wakeup time	Twu	—	V_{DD} = 2.5 V to 90 % RF, Pin = 0 dBm	—	—	20	µs
Control current	Ictl	—	Vctl = 1.8 V	—	1	5	µA
Supply current	Idd	—	V_{DD} = 2.7 V	—	0.14	0.35	mA

Electrical characteristics are measured with all RF ports terminated in 50 Ω.

*1 Pin = 25 dBm, 704 to 787 MHz (Band 13, Band 17)
*2 Pin = 26 dBm, 824 to 960 MHz (Band 5, Band 8)
*3 Pin = 26 dBm, 1710 to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 3 Tx, Band 4 Tx)
*4 Pin = 10 dBm, 2110 to 2170 MHz (Band 1 Rx, Band 4 Rx)
*5 Pin = 26 dBm, 2500 to 2690 MHz (Band 7)
*6 Pin = 35 dBm, 824 to 915 MHz (GSM850/900 Tx)
*7 Pin = 32 dBm, 1710 to 1910 MHz (GSM1800/1900 Tx)
*8 Pin = 10 dBm, 869 to 960 MHz (GSM850/900 Rx)
*9 Pin = 10 dBm, 1805 to 1990 MHz (GSM1800/1900 Rx)
*10 Measured with the recommended circuit.

IMD Condition (1)

Band	fRx on RF [MHz]	fTx +20 dBm on RF [MHz]	fBlocker –15 dBm on ANT [MHz]		IMD condition
Band 1	2140	1950	IMD2 (fRx – fTx)	190	*11
			IMD2 (fRx + fTx)	4090	*12
			IMD3 (2fTx – fRx)	1760	*13
			IMD3 (2fTx + fRx)	6040	*14
Band 2	1960	1880	IMD2 (fRx – fTx)	80	*15
			IMD2 (fRx + fTx)	3840	*16
			IMD3 (2fTx – fRx)	1800	*17
			IMD3 (2fTx + fRx)	5720	*18
Band 5	880	835	IMD2 (fRx – fTx)	45	*19
			IMD2 (fRx + fTx)	1715	*20
			IMD3 (2fTx – fRx)	790	*21
			IMD3 (2fTx + fRx)	2550	*22
Band 7	2655	2535	IMD2 (fRx – fTx)	120	*23
			IMD2 (fRx + fTx)	5190	*24
			IMD3 (2fTx – fRx)	2415	*25
			IMD3 (2fTx + fRx)	7725	*26

IMD Condition (2)

Band	fRx on RF [MHz]	fTx PTx = +23 dBm on RF [MHz]	fBlocker PBlocker = +14 dBm on ANT [MHz]		IMD condition
Band 13	747	786	IMD3 (2fTx – fRx)	825	*27
BC0	872	782	IMD3 (fTx + fRx)/2	827	*28

IMD Condition (3)

Band	f1 +13 dBm on ANT [MHz]	f2 +13 dBm on ANT [MHz]	IMD3 Product on RF [MHz]		IMD condition
Band 25	1912.5	1872.5	IMD3 (2f1 – f2)	1952.5	*29

Triple Beat Ratio

(V_{DD} = 2.5 V, Ta = 25 °C)

Item	Symbol	Path	Condition					Min.	Typ.	Max.	Unit
			Input power at RF [dBm]	Tx1 at RF [MHz]	Tx2 at RF [MHz]	Jammer at ANT –30 dBm [MHz]	Triple beat product at RF [MHz]				
Triple beat ratio	TBR	ANT-RF1	21.5	835.5	836.5	881.5	881.5 ± 1	81	—	—	dBc
			21.5	1880	1881	1960	1960 ± 1	81	—	—	
			13.5	1732	1733	2132	2132 ± 1	81	—	—	
		ANT- RF2, RF3,RF4	21.5	835.5	836.5	881.5	881.5 ± 1	88	—	—	
			21.5	1880	1881	1960	1960 ± 1	88	—	—	
			13.5	1732	1733	2132	2132 ± 1	88	—	—	

* Electrical characteristics are measured with all RF ports terminated in 50 Ω.
  Measured with the recommended circuit.

IIP2

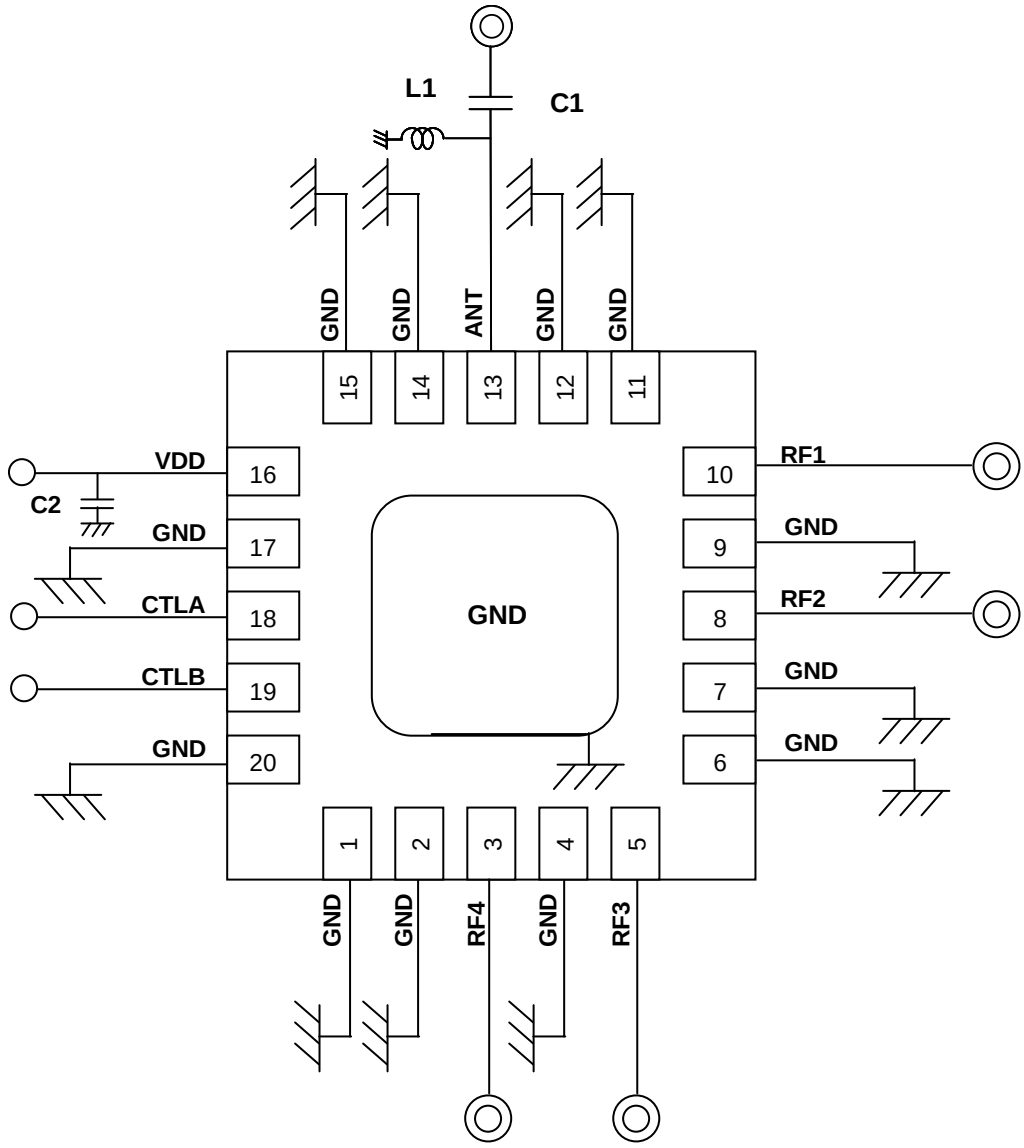
(V_{DD} = 2.5 V, Ta = 25 °C)

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
			Tx at RF 24 dBm [MHz]	Jammer at ANT –20 dBm [MHz]	IM2 product at RF [MHz]				
Input IP2	IIP2	ANT- RF1, RF2, RF3,RF4	836.61	1718.61	881.61	113.5	—	—	dBm
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
			1732.5	400	2132.5	95.5	—	—	

* Electrical characteristics are measured with all RF ports terminated in 50 Ω.
  Measured with the recommended circuit.

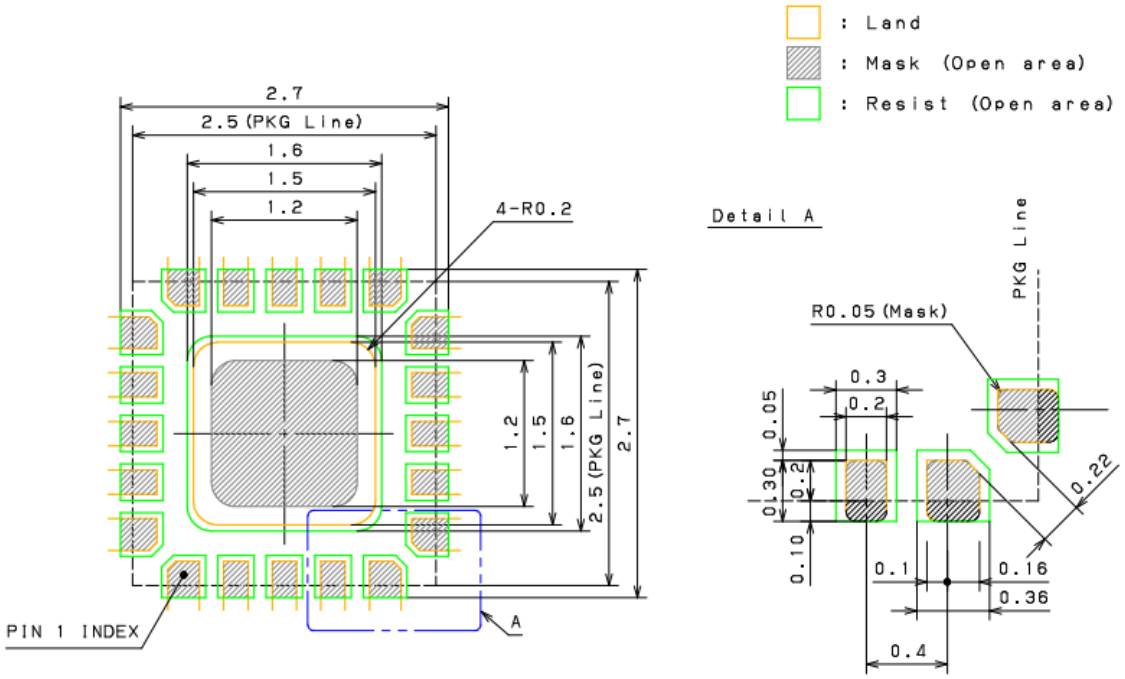
Recommended Circuit

UQFN-20P PKG(2.5m x 2.5mm)



*1 No DC blocking capacitors are required on all RF ports. (Except sourcing DC bias)
*2 The DC levels of all RF ports are GND.
*3 L1 (27 nH) and C1(12 pF) are recommended on Ant port for ESD protection.
*4 C2(100 pF) is recommended on VDD pin for Decoupling Capacitor.

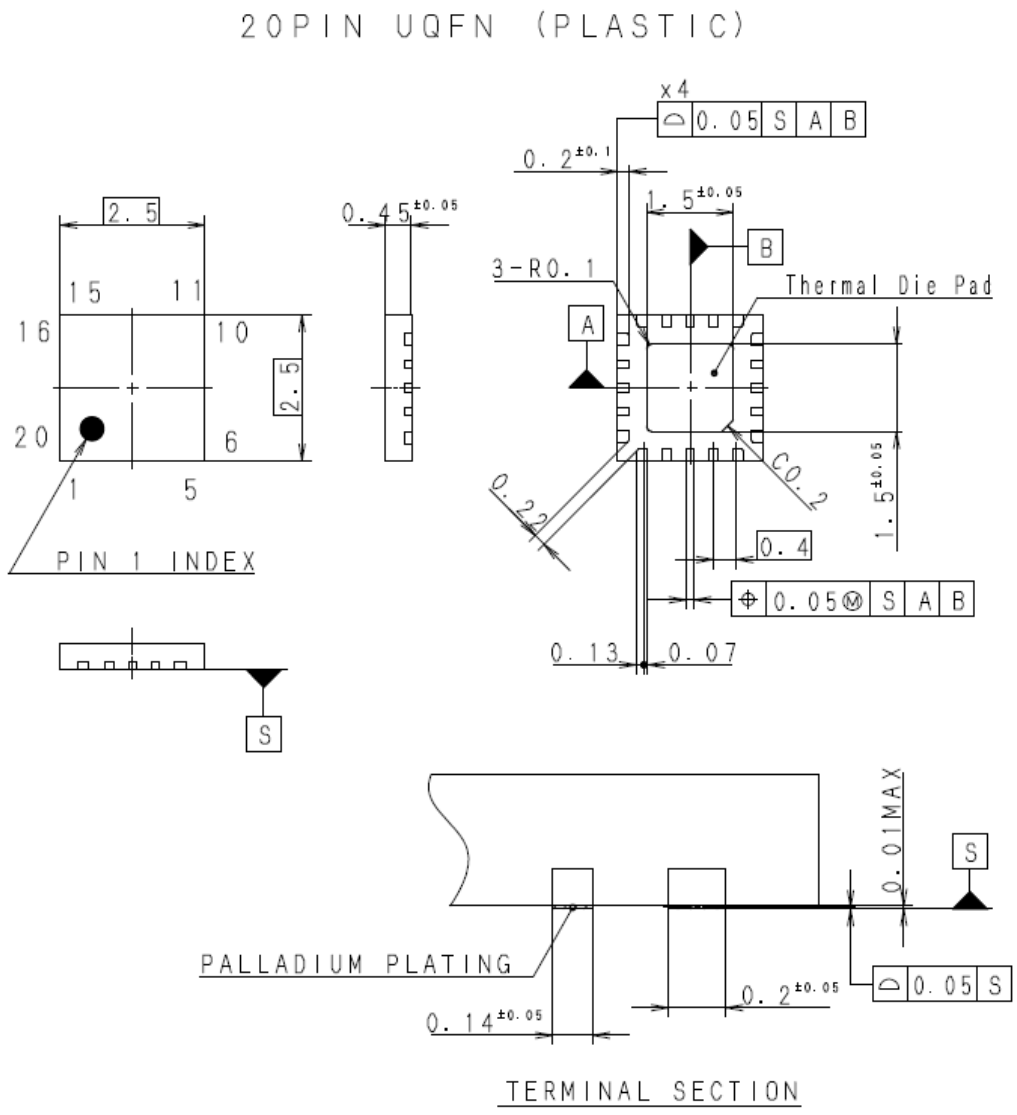
Recommended Land Pattern



Package Outline

(Unit: mm)

Product Code：875342357



Note:Terminal burr height 0.05mm MAX.

SONY CODE	UQFN-20P-052
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.010g

PART No. AP-2000-20QND2	Rev. 0
ISSUED '11.12.19	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:UR-20-ED	

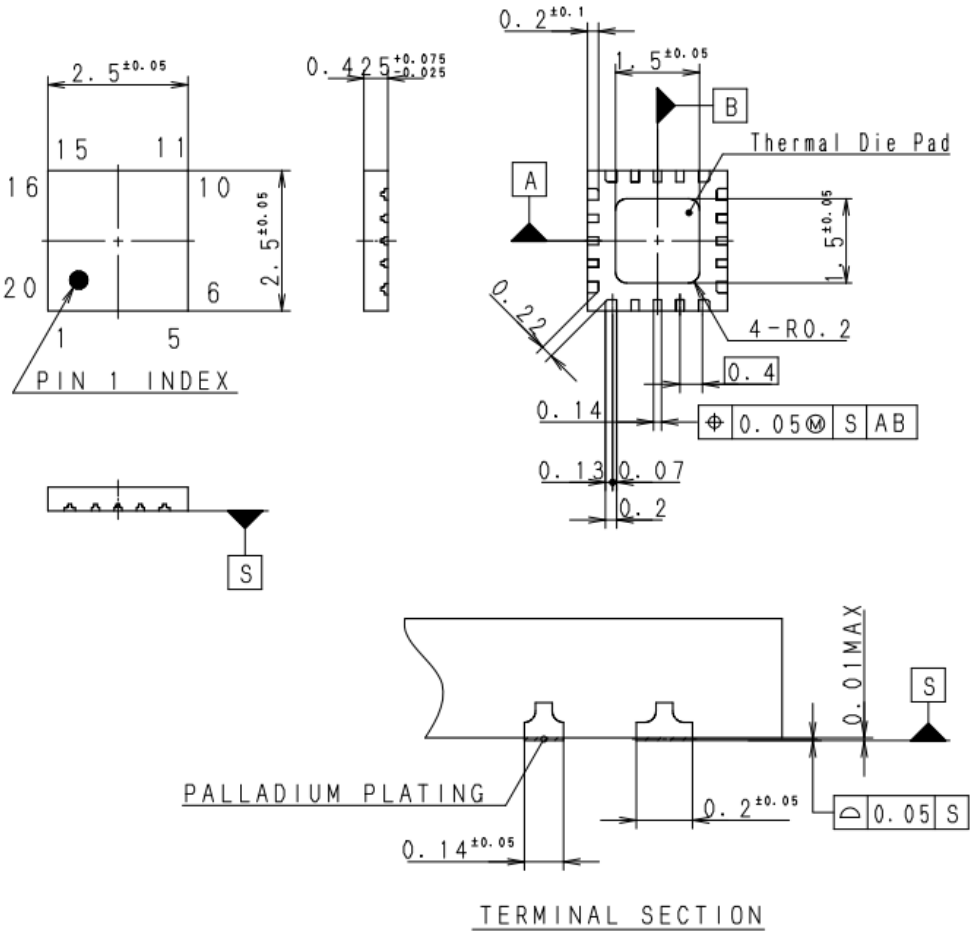
SONY

Package Outline

(Unit: mm)

Product Code：875342698

20PIN UQFN (PLASTIC)



TERMINAL SECTION

Note:Terminal burr height 0.05mm MAX.

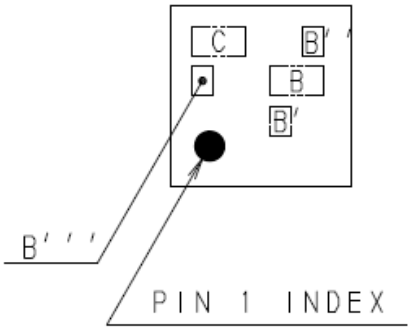
SONY CODE	UQFN-20P-04
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.0089g

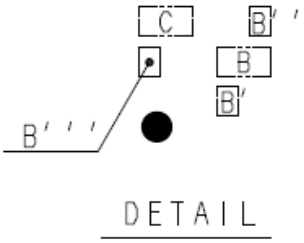
PART No. AP-4000-20026S	Rev. 0
ISSUED '12.10.02	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR
REMARKS PKG CODE:UR-20-D	

Marking



MARKING C: GP

注1) B部, B'部, B''はロット番号 (Max4文字) を配置する。
(B部, B'は通し記号, B''は製造年を配置する。)
注2) B'''は組立場所表記を配置する。
注3) C部は製品名 (Max2文字) を配置する。
(2文字を超える場合は製品名省略標示規定に従う。)
注4) マーク深さは, Max0.05mmの事。



< INSTRUCTIONS >
1) LOT NO. (MAX 4 CHARACTERS) IN SECTION B, B', B''.
(B, B' : SERIAL CODE, B'' : YEAR OF MANUFACTURE.
2) ASSEMBLY PLACE IN SECTION B'''.
3) TYPE NO. (MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
4) MARK DEPTH MAX 0.05 mm.

SONY

Tape and Reel Size

CXM3599UR-T9

Product Code：875342357

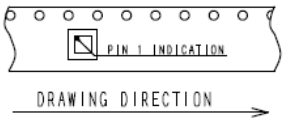
8mm WIDTH EMBOSSED TAPING

PACKAGE CODE	EMBOSSED TAPING CODE
UQFN-20P-052	R020XN25-08-N-1

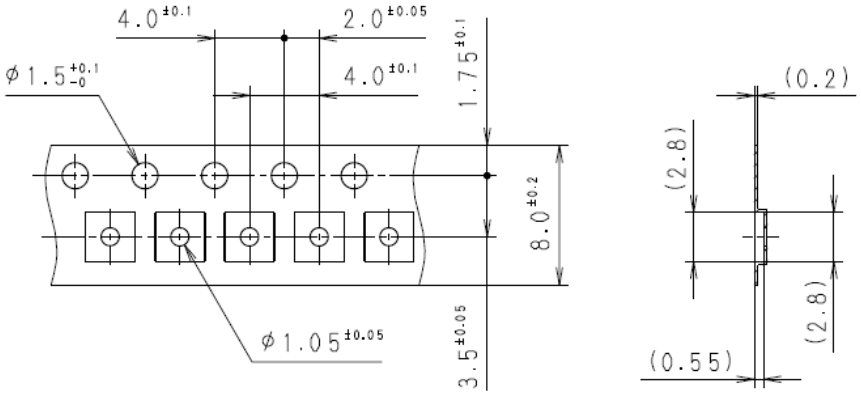
1. SCOPE

THIS SPECIFICATION DESCRIBES THE EMBOSSED TAPING FOR SMD(SURFACE MOUNTED DEVICE) IC'S. FOR SHIPMENT. THIS SPECIFICATION IS BASED ON THE STIPULATIONS OF JAPAN ELECTRONICS AND INFORMATION TECHNOLOGY INDUSTRIES ASSOCIATION(JEITA), JIS C0806-3, AND ELECTRONIC INDUSTRIES ASSOCIATION EIA-481.

2. PRODUCT INDICATION



3. TAPING SPECIFICATIONS

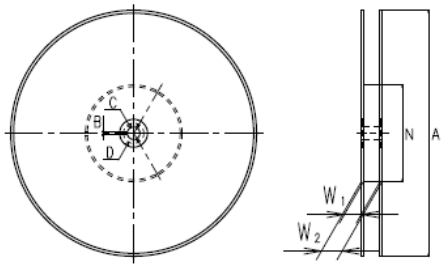


NOTE)1. THE R MEASUREMENT WITHOUT INDICATION IS ASSUMED TO BE 0.3mm MAX. GENERAL TOLERANCE: ±0.2

2. THE FEED HOLE CUMULATIVE PITCH ERROR IS ASSUMED AT±0.2mm/10PITCH. UNIT:mm

4. REEL DIMENSIONS

φ254mm PLASTIC REEL



UNIT:mm

SYMBOL	A	N	C	D
DIMENSION	φ254±2	φ100±1	φ13±0.2	φ21±0.8
SYMBOL	B	W_1	W_2	
DIMENSION	2±0.5	9.4±1.0	13.4±1.0	

MATERIAL:POLYSTYRENE CONTAINING CARBON(ANTISTATIC)

※INTRODUCTION OF REUSE REEL

(REEL THAT IS USED AGAIN AFTER COLLECTION)

WE USE THE REUSE REEL OF JEITA SPECIFICATION.

SONY

Tape and Reel Size

CXM3599UR-T9

Product Code：875342698

8mm WIDTH EMBOSSED TAPING

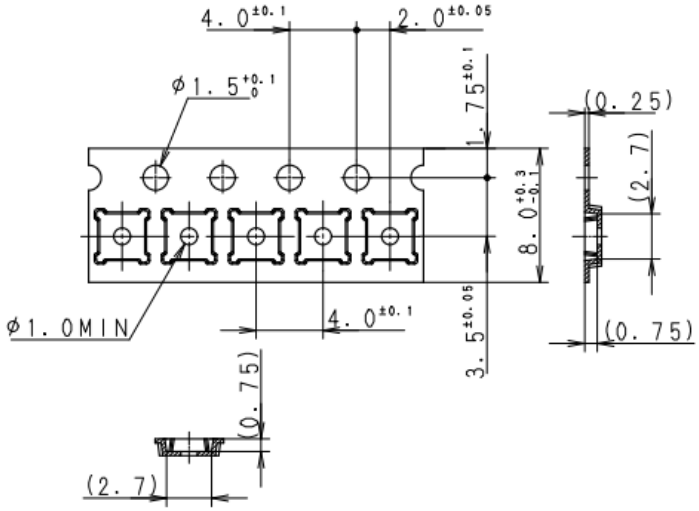
PACKAGE CODE	EMBOSSED TAPING CODE
UQFN-16P-02 UQFN-20P-04	R016UN25-08-N-1

1. SCOPE

THIS SPECIFICATION DESCRIBES THE EMBOSSED TAPING FOR SMD(SURFACE MOUNTED DEVICE) IC'S. FOR SHIPMENT. THIS SPECIFICATION IS BASED ON THE STIPULATIONS OF JAPAN ELECTRONICS AND INFORMATION TECHNOLOGY INDUSTRIES ASSOCIATION(JEITA), JIS C0806-3, AND ELECTRONIC INDUSTRIES ASSOCIATION EIA-481.

2. PRODUCT INDICATION

3. TAPING SPECIFICATIONS



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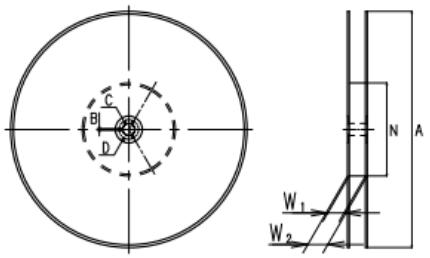
φ254mm PLASTIC REEL



UNIT:mm

SYMBOL	A	N	C	D
DIMENSION	φ254±2	φ100*±0	φ13±0.2	φ21±0.8
SYMBOL	B	W_1	W_2	
DIMENSION	2±0.5	9.4±1.0	13.4±1.0	

MATERIAL:POLYSTYRENE CONTAINING CARBON(ANTISTATIC)

*INTRODUCTION OF REUSE REEL
(REEL THAT IS USED AGAIN AFTER COLLECTION)
WE USE THE REUSE REEL OF JEITA SPECIFICATION.

SONY

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.