

Timing Generator for Progressive Scan CCD Image Sensor

Description

The CXD2452R is a timing generator which generates the timing pulses for performing progressive scan readout for digital still cameras and personal computer image input applications using the ICX098AK CCD image sensor.

Features

- Base oscillation frequency 2340f_H
- Monitoring readout allowed
- High-speed/low-speed electronic shutter function
- Horizontal driver for CCD image sensor
- Signal processor IC system clock generation 1170f_H, 780f_H
- Vertical/horizontal sync (SSG) timing generation

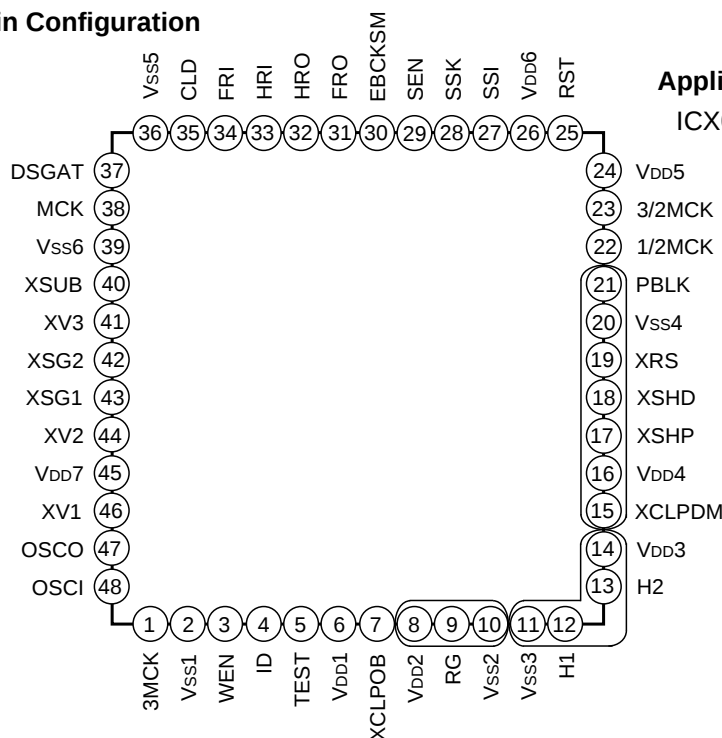
Applications

- Digital still cameras
- Personal computer image input

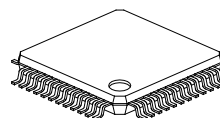
Structure

Silicon gate CMOS IC

Pin Configuration



48 pin LQFP (Plastic)



Absolute Maximum Ratings

- Supply voltage V_{DD} $V_{SS} - 0.5$ to $+7.0$ V
- Input voltage V_I $V_{SS} - 0.5$ to $V_{DD} + 0.5$ V
- Output voltage V_O $V_{SS} - 0.5$ to $V_{DD} + 0.5$ V
- Operating temperature

T_{opr}	-20 to +75	°C
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- Storage temperature

T_{stg}	-55 to +150	°C
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Recommended Operating Conditions

- Supply voltage

$V_{DDA}, V_{DDb}, V_{DDC}, V_{DDd}$	3.0 to 3.6	V
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- Operating temperature

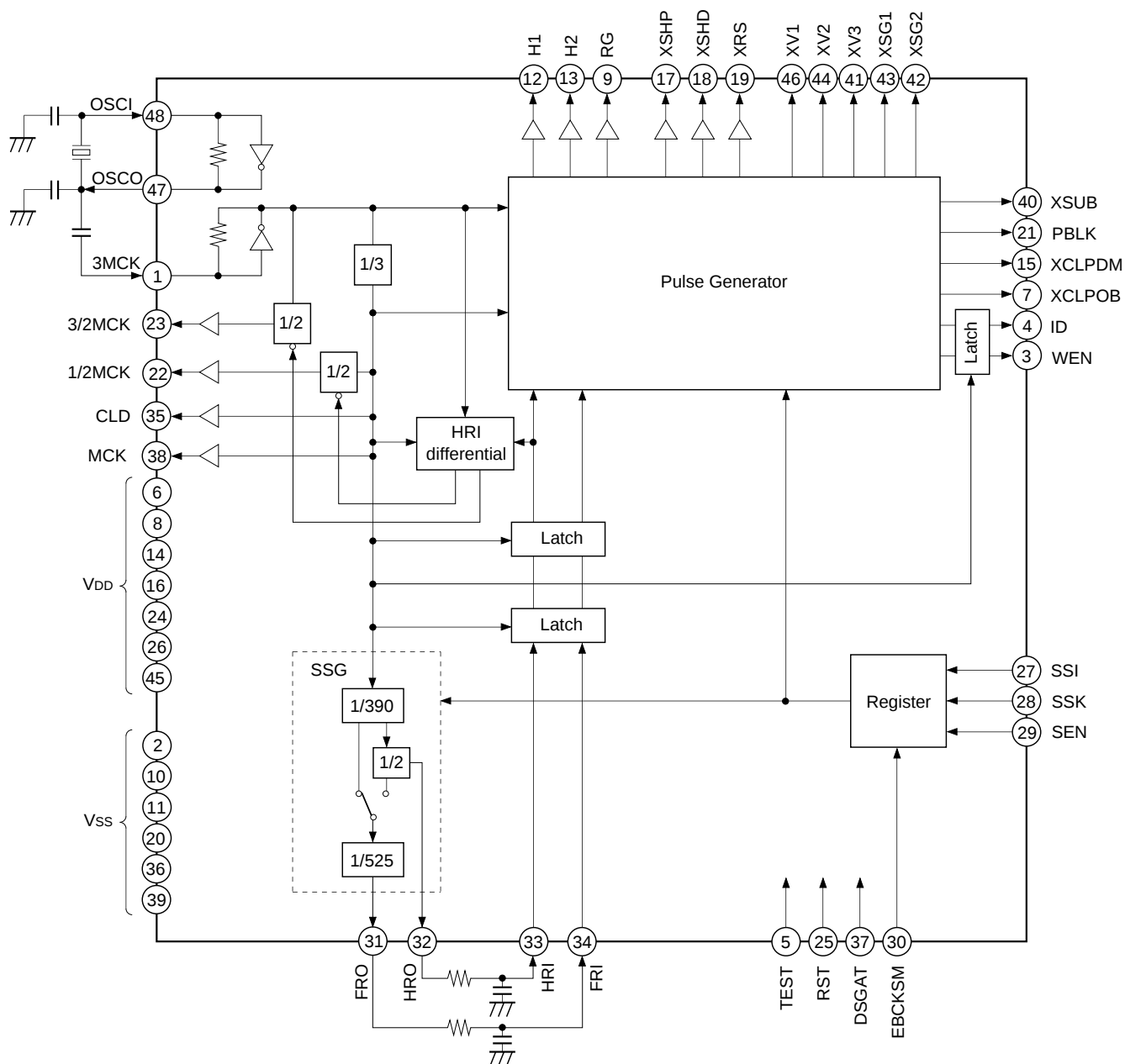
T_{opr}	-20 to +75	°C
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Applicable CCD Image Sensors

ICX098AK (1/4" CCD)

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Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	3MCK	I	Internal main clock. (2340f _H)
2	Vss1	—	GND
3	WEN	O	Memory write timing. Stop control possible using the serial interface data.
4	ID	O	Vertical direction line identification pulse output. Stop control possible using the serial interface data.
5	TEST	I	IC test pin; normally fixed to GND. (With pull-down resistor)
6	V _{DD} 1	—	3.3V power supply. (Power supply for common logic block)
7	XCLPOB	O	Pulse output for optical black bit block clamp. Stop control possible using the serial interface data.
8	V _{DD} 2	—	3.3V power supply. (Power supply for RG)
9	RG	O	CCD reset gate pulse output. (780f _H)
10	Vss2	—	GND
11	Vss3	—	GND
12	H1	O	CCD horizontal register drive clock output. (780f _H)
13	H2	O	CCD horizontal register drive clock output. (780f _H)
14	V _{DD} 3	—	3.3V power supply. (Power supply for H1/H2)
15	XCLPDM	O	Pulse output for dummy bit block clamp .
16	V _{DD} 4	—	3.3V power supply. (Power supply for XSHP/XSHD/XRS)
17	XSHP	O	Precharge level sample-and-hold pulse output. (780f _H)
18	XSHD	O	Data level sample-and-hold pulse output. (780f _H)
19	XRS	O	Sample-and-hold pulse output for analog/digital conversion phase alignment. (780f _H)
20	Vss4	—	GND
21	PBLK	O	Pulse output for horizontal and vertical blanking interval pulse cleaning.
22	1/2MCK	O	Horizontal direction pixel identification pulse output. Stop control possible using the serial interface data.
23	3/2MCK	—	System clock output for signal processing IC (1170f _H). Stop control possible using the serial interface data.
24	V _{DD} 5	—	3.3V power supply. (Power supply for common logic block)
25	RST	I	Internal system reset input.
26	V _{DD} 6	—	3.3V power supply. (Power supply for common logic block)
27	SSI	I	Serial interface data input for internal mode settings.
28	SSK	I	Serial interface clock input for internal mode settings.
29	SEN	I	Serial interface strobe input for internal mode settings.
30	EBCKSM	I	CHKSUM enable. (With pull-down resistor)
31	FRO	O	Vertical sync signal output. Stop control possible using the serial interface data.
32	HRO	O	Horizontal sync signal output. Stop control possible using the serial interface data.

Pin No.	Symbol	I/O	Description
33	HRI	I	Horizontal sync signal input.
34	FRI	I	Vertical sync signal input.
35	CLD	O	Clock output for analog/digital conversion IC. (780f _H) Phase adjustment in 60° units possible using the serial interface data.
36	Vss5	—	GND
37	DSGAT	I	Control input used to stop pulse generation for CCD image sensor, sample-and-hold IC and analog/digital conversion IC. Controlled pulse can be changed using the serial interface data.
38	MCK	O	System clock output for signal processor IC. (780f _H)
39	Vss6	—	GND
40	XSUB	O	Pulse output for electronic shutter.
41	XV3	O	CCD vertical register drive pulse output.
42	XSG2	O	CCD sensor readout pulse output.
43	XSG1	O	CCD sensor readout pulse output.
44	XV2	O	CCD vertical register drive pulse output.
45	V _{DD} 7	—	3.3V power supply. (Power supply for common logic block)
46	XV1	O	CCD vertical register drive pulse output.
47	OSCO	O	Inverter output for oscillation.
48	OSCI	I	Inverter input for oscillation.

Electrical Characteristics

DC Characteristics

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	V _{DD2}	V _{DDa}		3.0	3.3	3.6	V
Supply voltage 2	V _{DD3}	V _{DDb}		3.0	3.3	3.6	V
Supply voltage 3	V _{DD4}	V _{DDc}		3.0	3.3	3.6	V
Supply voltage 4	V _{DD1} , V _{DD5} , V _{DD6} , V _{DD7}	V _{DDd}		3.0	3.3	3.6	V
Input voltage 1*1	RST, DSGAT, SSI, SSK, SEN, FRI, HRI	V _{IH1}		0.8V _{DDd}			V
		V _{IL1}				0.2V _{DDd}	V
Input voltage 2*1 *2	EBCKSM	V _{IH2}		0.8V _{DDd}			V
		V _{IL2}				0.2V _{DDd}	V
Input voltage 3*2	TEST	V _{IH3}		0.7V _{DDd}			V
		V _{IL3}				0.3V _{DDd}	V
Output voltage 1	RG	V _{OH1}	Feed current where I _{OH} = -1.2mA	V _{DDa} - 0.8			V
		V _{OL1}	Pull-in current where I _{OL} = 2.4mA			0.4	V
Output voltage 2	H1, H2	V _{OH2}	Feed current where I _{OH} = -5.4mA	V _{DDb} - 0.8			V
		V _{OL2}	Pull-in current where I _{OL} = 10.8mA			0.4	V
Output voltage 3	XSHP, XSHD, XRS, PBLK, XCLPDM	V _{OH3}	Feed current where I _{OH} = -1.2mA	V _{DDc} - 0.8			V
		V _{OL3}	Pull-in current where I _{OL} = 2.4mA			0.4	V
Output voltage 4	3/2MCK, MCK, CLD	V _{OH4}	Feed current where I _{OH} = -5.4mA	V _{DDd} - 0.8			V
		V _{OL4}	Pull-in current where I _{OL} = 10.8mA			0.4	V
Output voltage 5	1/2MCK	V _{OH5}	Feed current where I _{OH} = -1.2mA	V _{DDd} - 0.8			V
		V _{OL5}	Pull-in current where I _{OL} = 2.4mA			0.4	V
Output voltage 6	XV1, XV2, XV3, XSUB, XSG1, XSG2, XCLPOB, ID, WEN	V _{OH6}	Feed current where I _{OH} = -2.4mA	V _{DDd} - 0.8			V
		V _{OL6}	Pull-in current where I _{OL} = 4.8mA			0.4	V
Output voltage 7	FRO, HRO	V _{OH7}	Feed current where I _{OH} = -3.6mA	V _{DDd} - 0.8			V
		V _{OL7}	Pull-in current where I _{OL} = 7.2mA			0.4	V

*1 These input pins do not have protective diodes on the internal power supply side.

*2 These input pins have internal pull-down resistors.

*3 The above table indicates the condition for 3.3V drive.

Inverter I/O Characteristics for Oscillation

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	OSCI	LVth			$V_{DDd}/2$		V
Input voltage	OSCI	V_{IH}		$0.7V_{DDd}$			V
		V_{IL}				$0.3V_{DDd}$	V
Output voltage	OSCO	V_{OH}	Feed current where $I_{OH} = -6.0\text{mA}$	$V_{DDd}/2$			V
		V_{OL}	Pull-in current where $I_{OL} = 6.0\text{mA}$			$V_{DDd}/2$	V
Feedback resistor	OSCI, OSCO	RFB	$V_{IN} = V_{DDd}$ or V_{SS}	500k	2M	5M	Ω
Oscillation frequency	OSCI, OSCO	f		20		50	MHz

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

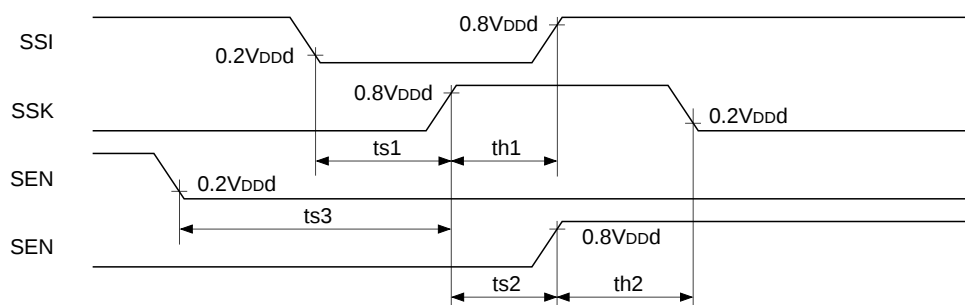
(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	3MCK	LVth			VDDd/2		V
Input voltage		VIH		0.7VDDd			V
		VIL				0.3VDDd	V
Input amplitude		VIN	fmax 50MHz sine wave	0.3			Vp-p

*1 Input voltage is the input voltage characteristics for direct input from an external source. Input amplitude is the input amplitude characteristics in the case of input through capacitor.

AC Characteristics

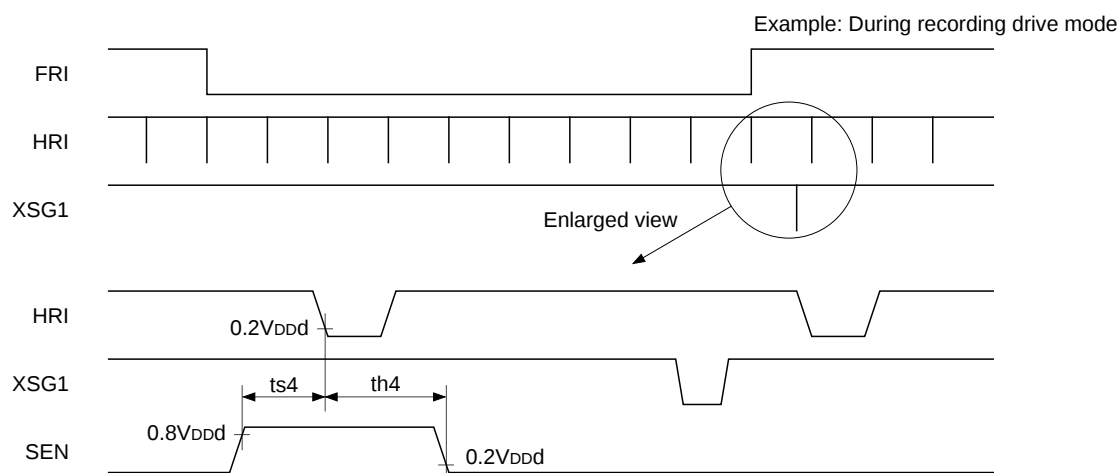
1) AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI setup time, activated by the rising edge of SSK	20			ns
th1	SSI hold time, activated by the rising edge of SSK	20			ns
ts2	SSK setup time, activated by the rising edge of SEN	20			ns
th2	SSK hold time, activated by the rising edge of SEN	20			ns
ts3	SEN setup time, activated by the rising edge of SSK	20			ns

2) Serial interface clock internal loading characteristics



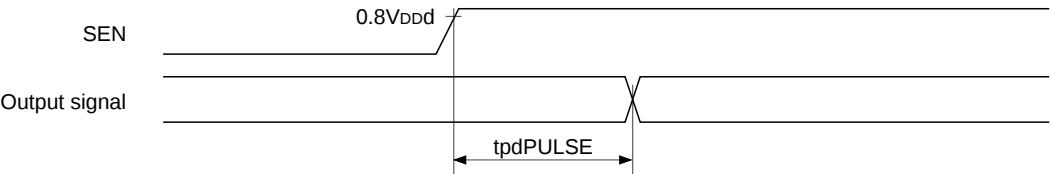
Note) Be sure to maintain a constantly high SEN logic level near the HRI fall immediately before XSG1 generation.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts4	SEN setup time, activated by the falling edge of HRI	0			ns
th4	SEN hold time, activated by the falling edge of HRI	0			ns

3) Serial interface clock output variation characteristics

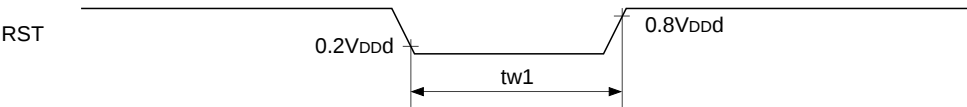
Normally, the serial interface data is loaded to the CXD2452R at the timing shown in 2) above. However, one exception to this is when the data such as SSGSEL and STB is loaded to the CXD2452R and controlled at the rising edge of SEN. For STB, see control data [D62] to [D63] STB in “Description of Operation”.



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpdPULSE	Output signal delay, activated by the rising edge of SEN	5		100	ns

4) RST loading characteristics

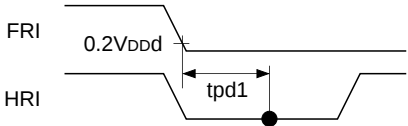


(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	RST pulse width	35			ns

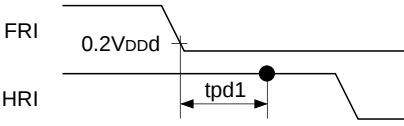
5) Phase identification characteristics using FRI and HRI input

When the HRI logic level is low tpd1 after the falling edge of FRI



The field is identified as an **ODD field**.

When the HRI logic level is high tpd1 after the falling edge of FRI

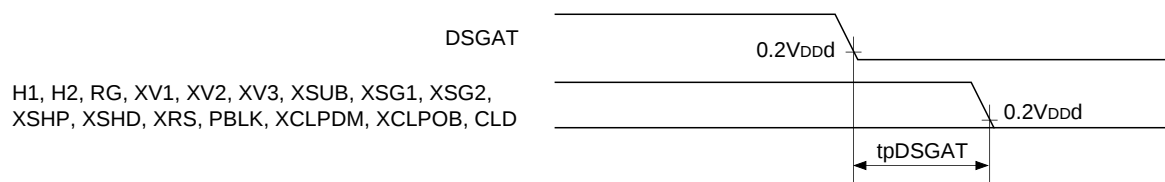


The field is identified as an **EVEN field**.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Field identification clock phase, activated by the falling edge of FRI	800		1600	ns

6) Output timing characteristics using DSGAT

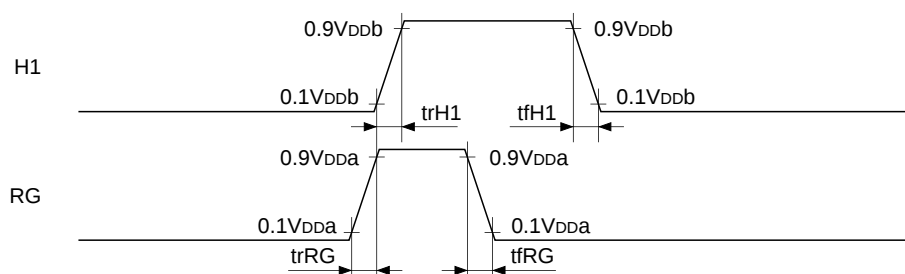


H1 and H2 load capacitance = 100pF, RG load capacitance = 20pF, XV1, XV2, XV3, XSG1, XSG2, XSUB, XSHP, XSHD, XRS, PBLK, XCLPDM, XCLPOB and CLD load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpDSGAT	Time until the above outputs go low after the fall of DSGAT			100	ns

7) H1 and RG waveform characteristics



V_{DDb} = 3.3V, Topr = 25°C, H1 and H2 load capacitance = 100pF, RG load capacitance = 20pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
trH1	H1 rise time		10		ns
tfH1	H1 fall time		10		ns
trRG	RG rise time		3		ns
tfRG	RG fall time		3		ns

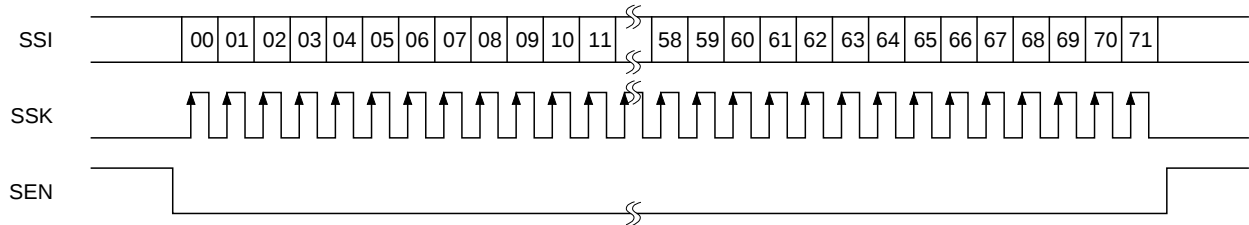
8) I/O pin capacitance

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
C _{IN}	Input pin capacitance			9	pF
C _{OUT}	Output pin capacitance			11	pF
C _{I/O}	I/O pin capacitance			11	pF

Description of Operation

All pulses output from the CXD2452R are controlled by the serial interface data shown below. The details of this control and a description of operation are as follows.



There are two types of serial interface data: drive control data and phase adjustment data. Hereafter, these data are distinguished by referring to the former as control data and the latter as adjustment data. First, an example of the initialization data for the CXD2452R control data is shown below. Assuming Application Circuit Block Diagram, care should be taken as there are some differences from the RST pin initialization data. This data shows the values when the EBCKSM pin is low and D64 to D71 CHKSUM is valid.

MSB								LSB							
D71	D70	D69	D68	D67	D66	D65	D64	D63	D62	D61	D60	D59	D58	D57	D56
1	0	1	0	1	1	0	1	0	0	0	0	0	0	1	0
MSB								LSB							
D55	D54	D53	D52	D51	D50	D49	D48	D47	D46	D45	D44	D43	D42	D41	D40
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MSB								LSB							
D39	D38	D37	D36	D35	D34	D33	D32	D31	D30	D29	D28	D27	D26	D25	D24
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSB								LSB							
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D09	D08
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MSB								LSB							
D07	D06	D05	D04	D03	D02	D01	D00								
1	0	0	0	0	0	0	1								

For the adjustment data, the data considered the most appropriate for the system at that time is used as the initialization data as required.

Control Data

Data	Symbol	Function	Data = 0	Data = 1	When a reset
D00 to D07	CHIP	Chip switching	See D00 to D07 CHIP.		All 0
D08 to D15	CTGRY	Category switching	See D08 to D15 CTGRY.		All 0
D16 to D17	SMD	Electronic shutter mode setting	See D16 to D35 Electronic shutter mode.		All 0
D18 to D25	Shut.FRM	Electronic shutter vertical interval setting	See D16 to D35 Electronic shutter mode.		All 0
D26 to D35	Shut.HD	Electronic shutter horizontal interval setting	See D16 to D35 Electronic shutter mode.		All 0
D36 to D47	—	—	—	—	All 0
D48	EXPOSE	Recording exposure setting switching	OFF	ON	0
D49 to D50	—	—	—	—	All 0
D51	PSMT	Drive mode switching	Monitoring	Recording	0
D52	SSGSEL	Internal SSG operation switching	OFF	ON	0
D53	WENSEL	WEN pulse operation switching	ON	OFF	0
D54	CLPSEL	XCLPOB pulse operation switching	OFF	ON	0
D55	IDSEL	ID pulse operation switching	OFF	ON	0
D56	HMCKSEL	1/2MCK pulse operation switching	OFF	ON	0
D57	TMCKSEL	3/2MCK pulse operation switching	ON	OFF	0
D58	HMCKREV	1/2MCK pulse reset polarity switching	Positive polarity	Negative polarity	0
D59	TMCKREV	2/3MCK pulse reset polarity switching	Negative polarity	Positive polarity	0
D60 to D61	DSG	Pulse generation control	See D60 to D61 DSG table.		All 0
D62 to D63	STB	IC pin status control	See D62 to D63 STB table.		All 0
D64 to D71	CHKSUM	Check sum bit	See D64 to D71 CHKSUM.		All 0

Detailed Description of Each Data

D00 to D07 CHIP

The serial interface data is loaded to the CXD2452R when **D00** and **D07** are 1. However, this assumes that either the EBCKSM pin is low and **D64** to **D71** CHKSUM is satisfied or the EBCKSM pin is high.

MSB								LSB	Function
D07	D06	D05	D04	D03	D02	D01	D00		
1	0	0	0	0	0	0	1		Loading to the CXD2452R

D08 to D15 CTGRY

Of the data provided to the CXD2452R by the serial interface, the CXD2452R loads **D16** and subsequent data to the control register side when **D08** is 0, and to the adjustment register side when **D08** is 1. However, this assumes that the CXD2452R is selected by CHIP and that either the EBCKSM pin is low and **D64** to **D71** CHKSUM is satisfied or the EBCKSM pin is high.

MSB								LSB	Function
D15	D14	D13	D12	D11	D10	D09	D08		
0	0	0	0	0	0	0	0		Loading to the control register side
0	0	0	0	0	0	0	1		Loading to the adjustment register side

D16 to D35 Electronic shutter mode

The CXD2452R's electronic shutter mode can be switched as follows by SMD **D16** to **D17**. Handling of the data from **D18** to **D35** differs according to the mode, and is explained in detail below.

D17	D16	Description of operation
X	0	XSUB stopped mode
0	1	High-speed/low-speed shutter mode
1	1	HTSG control mode

The electronic shutter data is expressed as shown in the table below using Shut.HD as an example.

MSB						LSB			
D35	D34	D33	D32	D31	D30	D29	D28	D27	D26
0	1	1	1	0	0	0	0	1	1
↓			↓					↓	
1			C					3	

→ Shut.HD is expressed as **1C3h**.

[XSUB stopped mode]

During this mode, the data from **D18** to **D35** is invalid. The shutter speed is 1/60s during monitoring drive mode, and 1/30s during recording drive mode.

[High-speed/low-speed shutter mode]

During this mode, the data has the following meanings.

Symbol	Data	Description
Shut.FRM	D18 to D25	Shutter speed data (number of vertical intervals) specification
Shut.HD	D26 to D35	Shutter speed data (number of horizontal intervals) specification

The interval during which Shut.FRM and Shut.HD are specified together is the shutter speed. Concretely, when specifying high-speed shutter, Shut.FRM is set to 00h. (See the figure.) During low-speed shutter, or in other words when Shut.FRM is set to 01h or higher, the serial interface data is not loaded until this interval is finished.

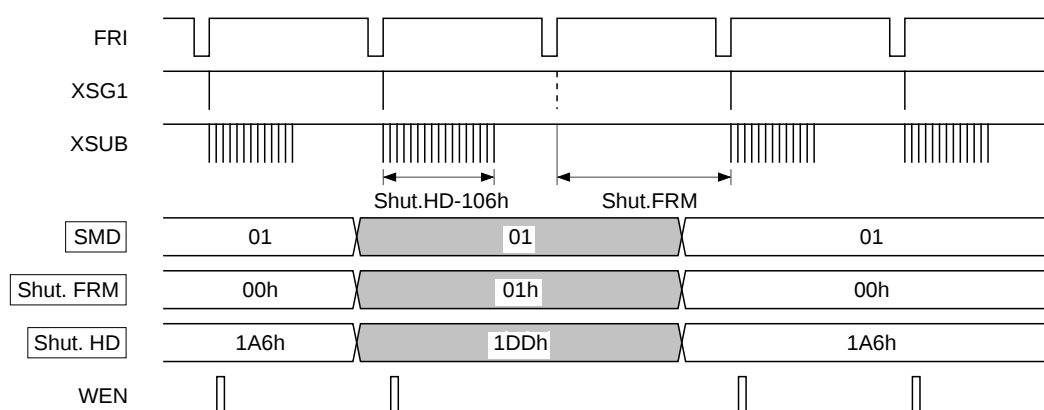
However, care should be taken as the vertical interval indicated here is set in 1/60s units when the drive mode is monitoring drive mode and 1/30s units during recording drive mode.

For monitoring drive mode, care should be taken that shut.HD value is offset. This is because the same exposure time can be obtained for the same shut.HD data without depending on drive mode basically for high-speed shutter.

Formula for calculating the electronic shutter speed: [Shut.FRM/Shut.HD] (unit: μs)

Monitoring drive mode:

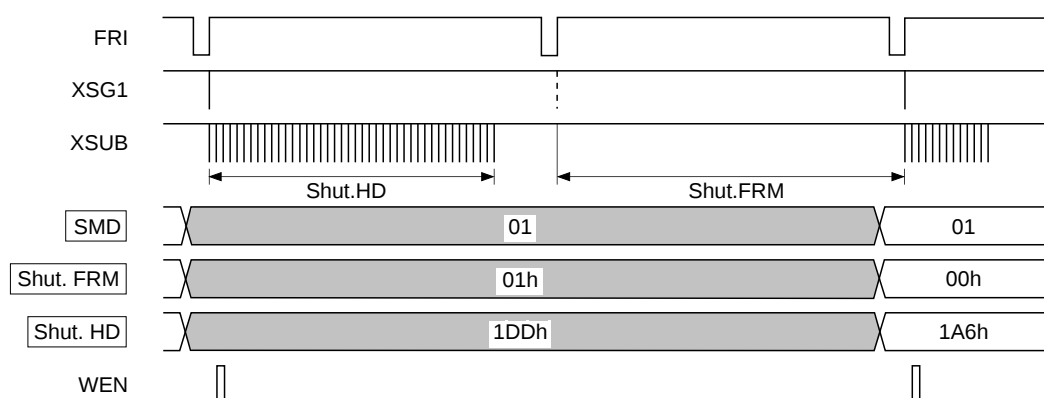
$$T = \text{Shut.FRM} \times 1.66834 \times 10^4 + \{(20\text{Ch} - \text{Shut.HD}) \times 780 + 447\} \times 81.5 \times 10^{-3} \quad (107\text{h} \leq \text{Shut.HD} \leq 20\text{Ch})$$



During monitoring drive mode/low-speed shutter mode

Recording drive mode:

$$T = \text{Shut.FRM} \times 3.33667 \times 10^4 + \{(20\text{Ch} - \text{Shut.HD}) \times 780 + 447\} \times 81.5 \times 10^{-3} \quad (000\text{h} \leq \text{Shut.HD} \leq 20\text{Ch})$$



During recording drive mode/low-speed shutter mode

Electronic shutter speed table [Shut.FRM/Shut.HD]

Shut.FRM	Shut.HD	Shutter speed (s)	Calculation results (s)	Shut.FRM	Shut.HD	Shutter speed (s)	Calculation results (s)
00h	20Ch	1/27000	1/27450	00h	107h* ¹	1/60	1/60
00h	20Bh	1/10000	1/10000	01h	20Ch	1/60* ²	1/60
00h	209h	1/4500	1/4403	01h	1D8h	1/50* ²	1/50
00h	205h	1/2000	1/2077	02h	20Ch	1/30* ²	1/30
00h	1FDh	1/1000	1/1010	07h	18Bh	1/8* ²	1/8
00h	1EDh	1/500	1/498	09h	109h	1/6* ²	1/6
00h	1CEh	1/250	1/251	00h	0D2h	1/50* ³	1/50
00h	18Fh	1/125	1/125	00h	083h	1/40* ³	1/40
00h	16Fh	1/100	1/100	00h	000h	1/30* ³	1/30

*¹ One XSUB pulse is generated for odd fields and two for even fields.

*² These are the settings during monitoring drive mode.

*³ These can only be specified during recording drive mode.

Note) Input prohibited data:

Monitoring drive mode

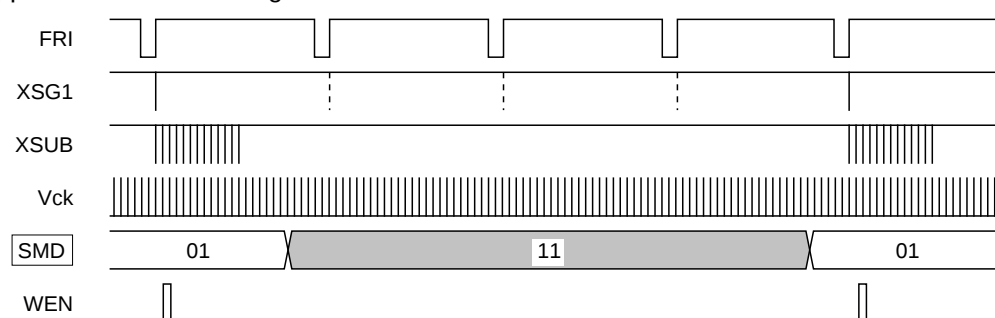
000h to 106h

Recording drive mode and monitoring drive mode

20Dh to 3FFh

[HTSG control mode]

During this mode, the data from **D18** to **D35** is invalid. The shutter speed is the value obtained by adding the shutter speed specified in the preceding vertical interval to the vertical period during which XSG1 (and XSG2) is stopped as shown in the figure.



During HTSG control mode

D51 PSMT

0: Driving is controlled in accordance with monitoring drive mode under the vertical/horizontal sync signals are input.

1: Driving is controlled in accordance with recording drive mode under the vertical/horizontal sync signals are input.

However, before starting recording drive mode, monitoring drive mode for recording exposure must be performed as shown in the figure. Therefore, control must be performed together with **D48 EXPOSE**. This control is designed so that a XSUB pulse is always generated during the horizontal interval immediately after XSG1 even if the electronic shutter speed is set to 1/60s (SMD = 00).

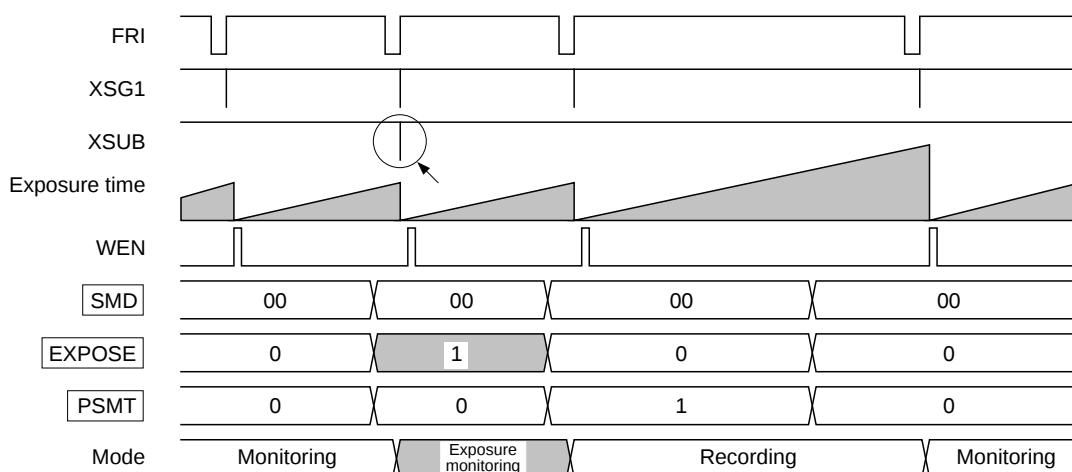


Image of switching from monitoring drive mode to recording drive mode

D60 to D61 DSG

The CXD2452R can control the generation of CCD pulses and pulses for the sample-and-hold and analog/digital conversion ICs by setting the DSGAT pin low. Conversely, when the DSGAT pin is set high, the controlled pulses can be switched as follows.

D61	D60	Operating mode
0	0	No control performed
0	1	CCD pulse control
1	0	Sample-and-hold and analog/digital conversion IC pulse control
1	1	CCD pulse and sample-and-hold and analog/digital conversion IC pulse control

Here, CCD pulses refer to the H1, H2, RG, XV1, XV2, XV3, XSUB, XSG1 and XSG2 pulses. Sample-and-hold and analog/digital conversion IC pulses refer to the XSHP, XSHD, XRS, PBLK, XCLPOB, XCLPDM and CLD pulses.

D62 to D63 STB

This switches the operating mode as shown below. However, the IC pin status control bit is loaded to the CXD2452R and controlled immediately at the rise of the SEN input.

D63	D62	Symbol	Operating mode
X	0	CAMERA	Normal operation mode
0	1	SLEEP	Sleep mode* ¹
1	1	STNBY	Standby mode

*¹ Mode for the status which does not require CCD drive when playing back recorded data within the system.

The pin status during each mode is shown in the table below.

Pin	Symbol	CAMERA	SLEEP	STNBY	Pin	Symbol	CAMERA	SLEEP	STNBY
1	3MCK	ACT	ACT	ACT	25	RST	ACT	ACT	ACT
2	Vss1	—			26	VDD6	—		
3	WEN	ACT	L	L	27	SSI	ACT	ACT	ACT
4	ID	ACT	L	L	28	SSK	ACT	ACT	ACT
5	TEST	—			29	SEN	ACT	ACT	ACT
6	VDD1	—			30	EBCKSM	ACT	ACT	ACT
7	XCLPOB	ACT	L	L	31	FRO	ACT	ACT	L
8	VDD2	—			32	HRO	ACT	ACT	L
9	RG	ACT	L	L	33	HRI	ACT	ACT	ACT
10	Vss2	—			34	FRI	ACT	ACT	ACT
11	Vss3	—			35	CLD	ACT	L	L
12	H1	ACT	L	L	36	Vss5	—		
13	H2	ACT	L	L	37	DSGAT	ACT	ACT	ACT
14	VDD3	—			38	MCK	ACT	ACT	L
15	XCLPDM	ACT	L	L	39	Vss6	—		
16	VDD4	—			40	XSUB	ACT	L	L
17	XSHP	ACT	L	L	41	XV3	ACT	L	L
18	XSHD	ACT	L	L	42	XSG2	ACT	L	L
19	XRS	ACT	L	L	43	XSG1	ACT	L	L
20	Vss4	—			44	XV2	ACT	L	L
21	PBLK	ACT	L	L	45	VDD7	—		
22	1/2MCK	ACT	L	L	46	XV1	ACT	L	L
23	3/2MCK	ACT	ACT	L	47	OSCO	ACT	ACT	ACT
24	VDD5	—			48	OSCI	ACT	ACT	ACT

Note) ACT means that the circuit is operating. L indicates a low output level in the controlled status.

D64 to D71 CHKSUM

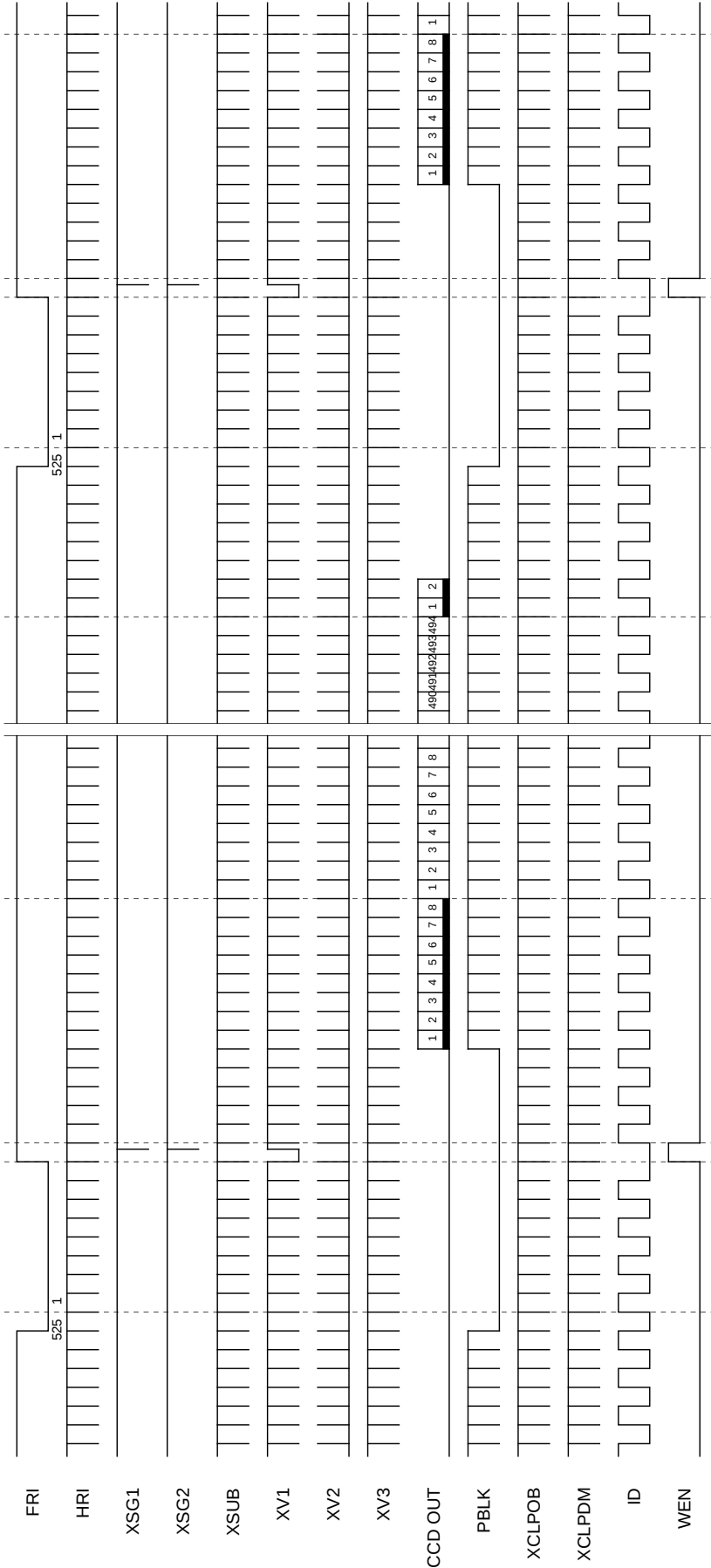
This is the check sum bit. Apply the data shown below.

	MSB				LSB				
	D07	D06	D05	D04	D03	D02	D01	D00	
	D15	D14	D13	D12	D11	D10	D09	D08	
	D23	D22	D21	D20	D19	D18	D17	D16	
	D31	D30	D29	D28	D27	D26	D25	D24	
	D39	D38	D37	D36	D35	D34	D33	D32	
	D47	D46	D45	D44	D43	D42	D41	D40	
	D55	D54	D53	D52	D51	D50	D49	D48	
	D63	D62	D61	D60	D59	D58	D57	D56	
+)	D71	D70	D69	D68	D67	D66	D65	D64	→ CHKSUM
	0	0	0	0	0	0	0	0	→ Reflected when the total is 0.

Chart-1 Vertical Direction Timing Chart

MODE (Base oscillation frequency: 2340fh)
Recording drive mode

Applicable CCD image sensor
ICX098AK

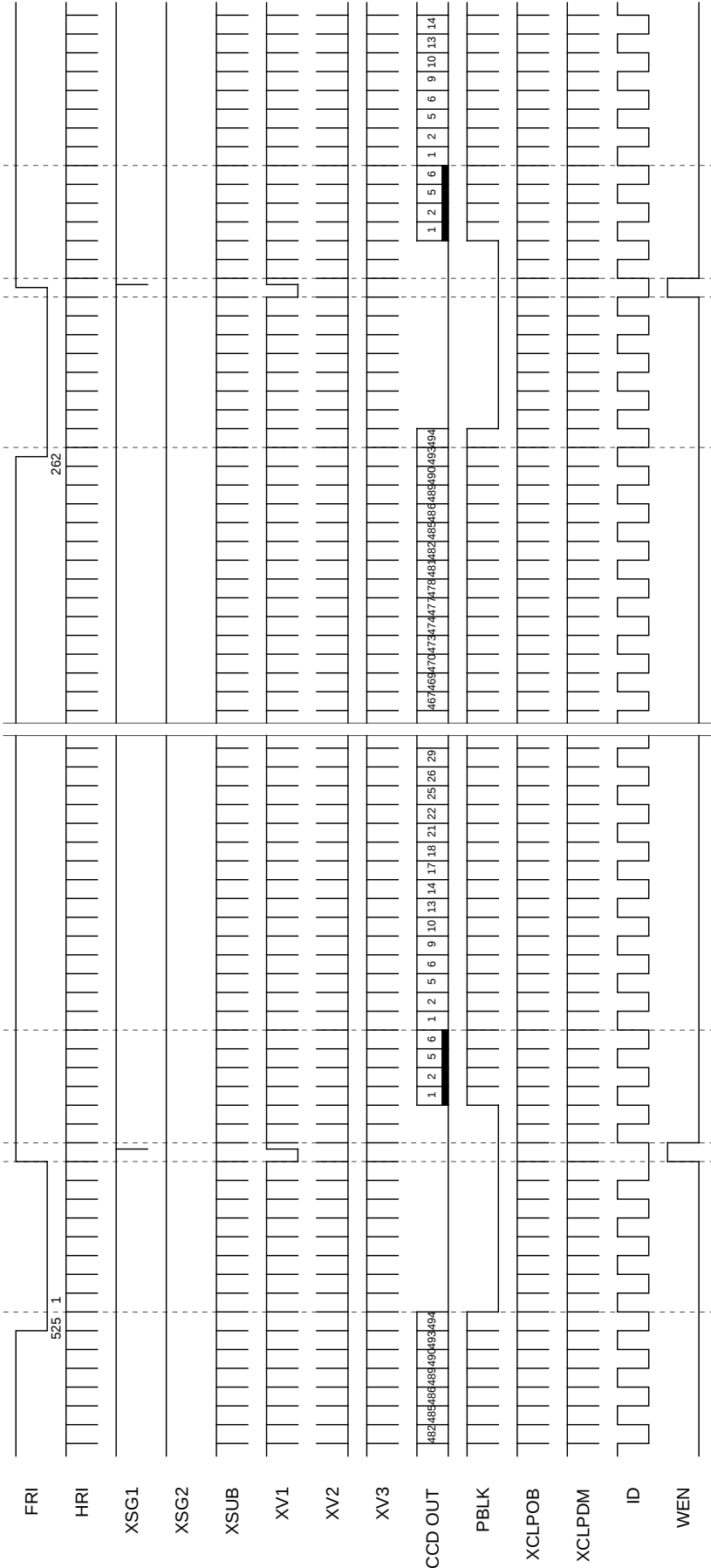


* The number of XSUB pulses is determined by the serial interface data. This chart shows the case where Shut.HD = 20Ch and XSUB pulses are generated over the entire horizontal interval.
* In addition to the phase relationship between FRI and HRI shown above, the phases may also be offset by 1/2 horizontal interval. In any case, the readout interval is the 9th HRI fall counted from the fall of FRI.

Chart-2 Vertical Direction Timing Chart

MODE (Base oscillation frequency: 2340fH)
Monitoring drive mode

Applicable CCD image sensor
ICX098AK

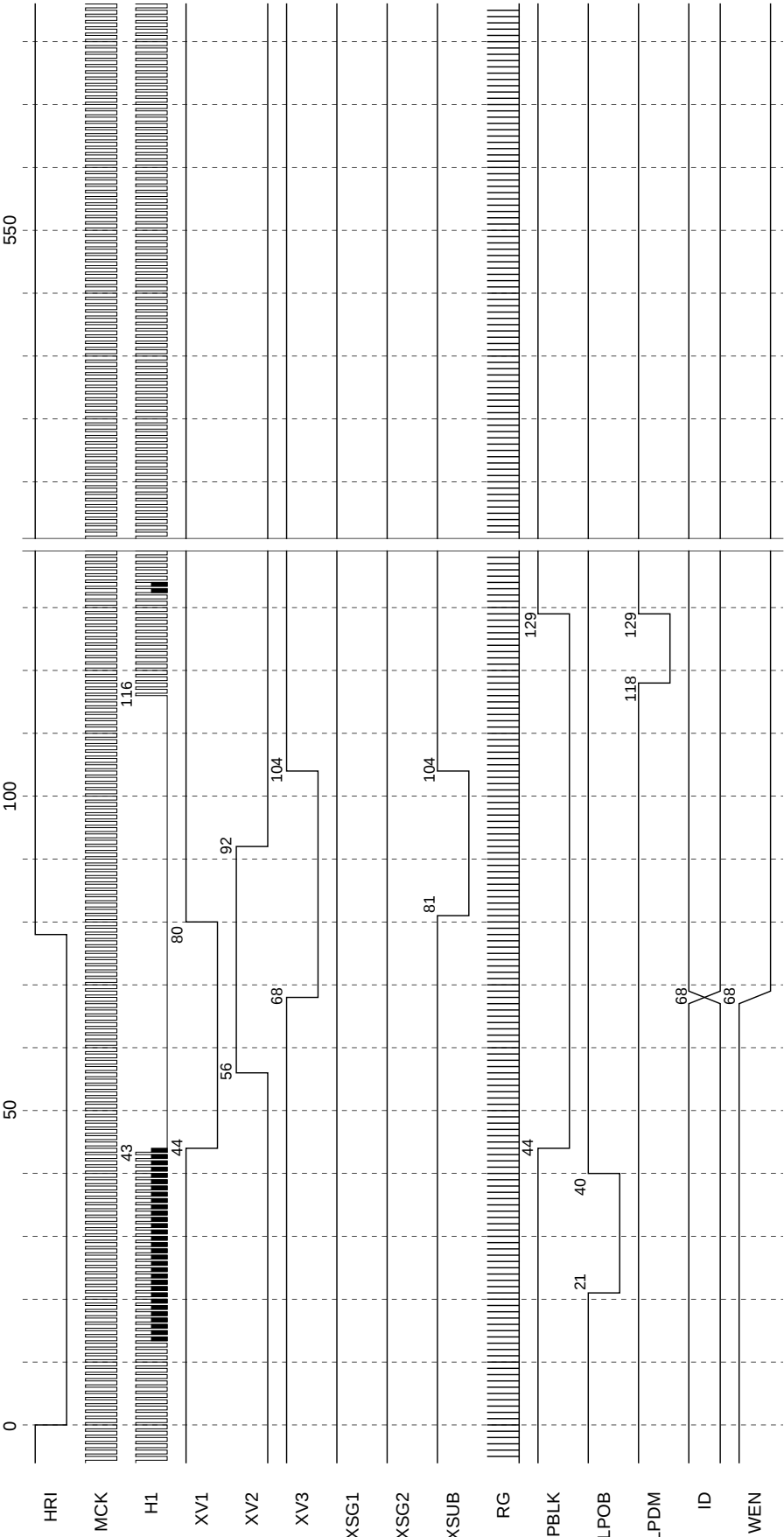


* The number of XSUB pulses is determined by the serial interface data. This chart shows the case where Shut.HD = 20Ch and XSUB pulses are generated over the entire horizontal interval.

Chart-3 Horizontal Direction Timing Chart

MODE (Base oscillation frequency: 2340fH)
Recording drive mode

Applicable CCD image sensor
ICX098AK

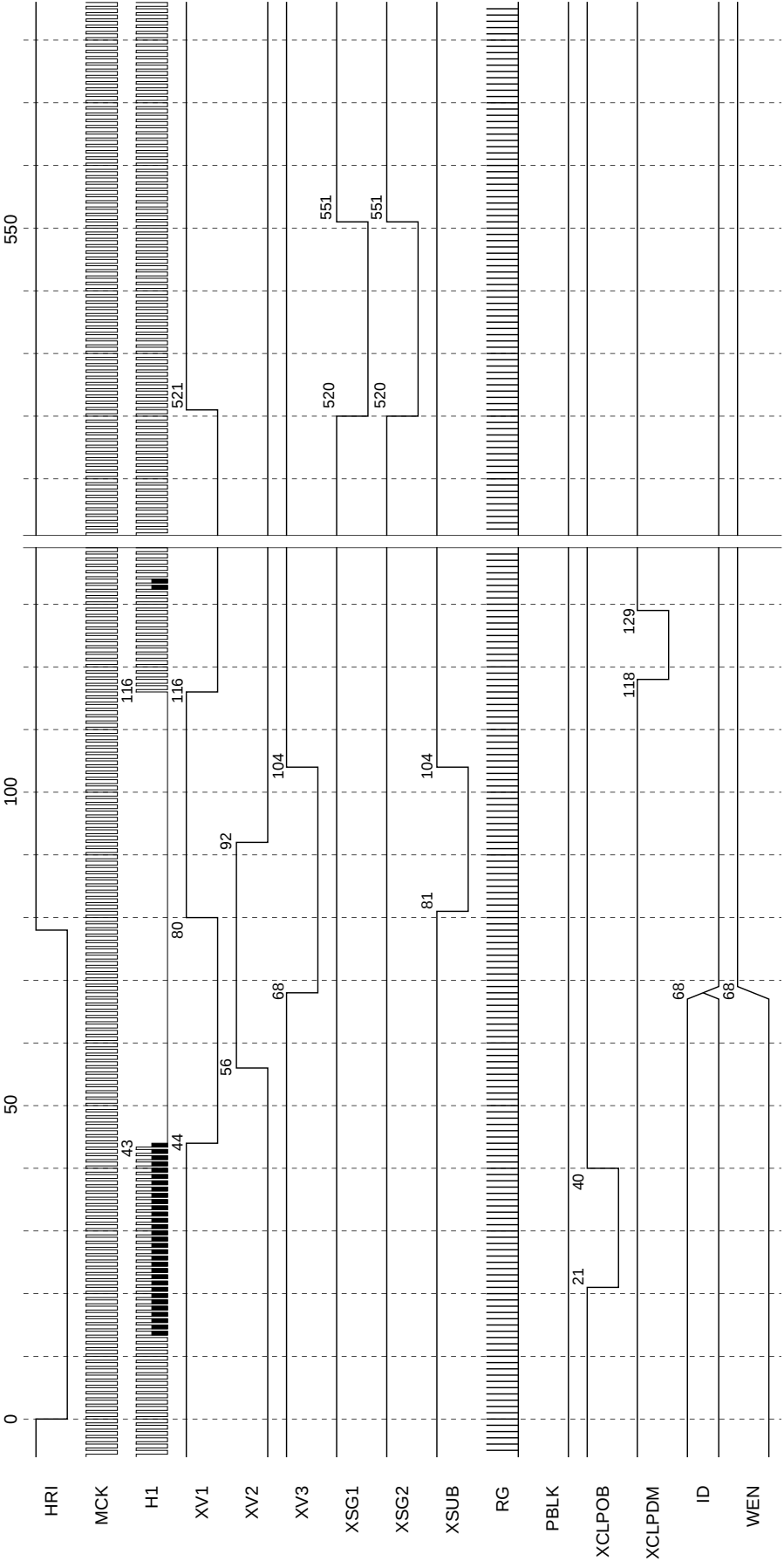


* The HRI of this chart is equivalent to HRI' of Chart-7. This HRI indicates a timing that the CXD2452R takes in actually.
* The numbers at the output pulse transition points indicate the count at the MCK (780fH) rise from the fall of HRI.
* The HRI fall interval should be between 3.6 to 9.4μs. This chart shows an interval of 78ck (6.3μs).
* XSUB is output at the timing shown above when specified by the serial interface data.
* The ID transition timing is synchronized with the fall of XV3.
* WEN is output during the horizontal interval shown in Chart-1. The transition timing is the same as that for ID.

Chart-4 Horizontal Direction Timing Chart

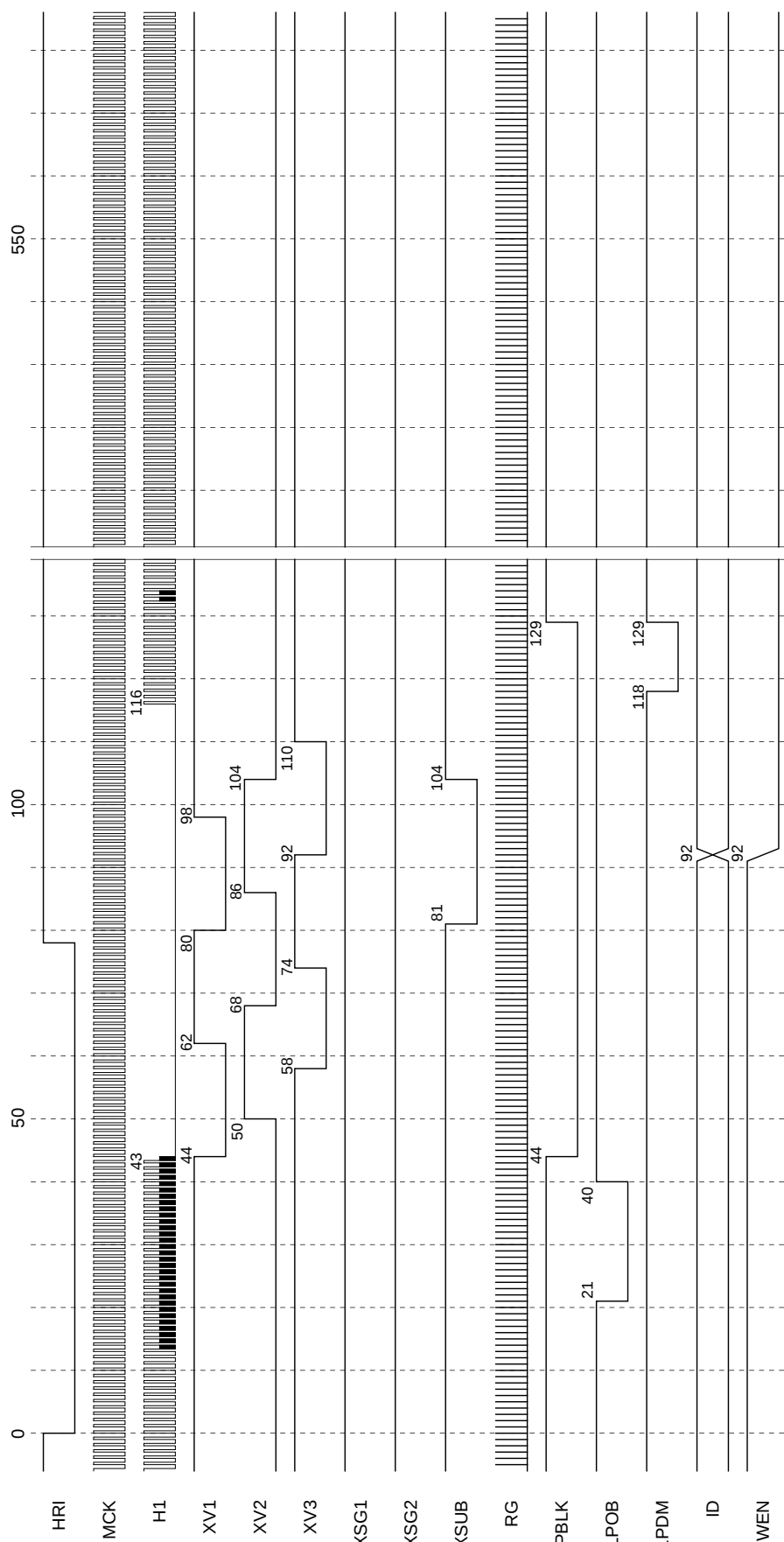
MODE (Base oscillation frequency: 2340fH)
Recording drive mode (readout portion)

Applicable CCD image sensor
ICX098AK



* The HRI of this chart is equivalent to HRI' of Chart-7. This HRI indicates a timing that the CXD2452R takes in actually.
* The numbers at the output pulse transition points indicate the count at the MCK (780fH) rise from the fall of HRI.
* The HRI fall interval should be between 3.6 to 9.4μs. This chart shows an interval of 78ck (6.3μs).
* XSUB is output at the timing shown above when specified by the serial interface data.
* The ID transition timing is synchronized with the fall of XV3. ID is reset low at this timing during the readout horizontal interval.
* WEN is output during the horizontal interval shown in Chart-1. The transition timing is the same as that for ID.

Chart-5 Horizontal Direction Timing Chart

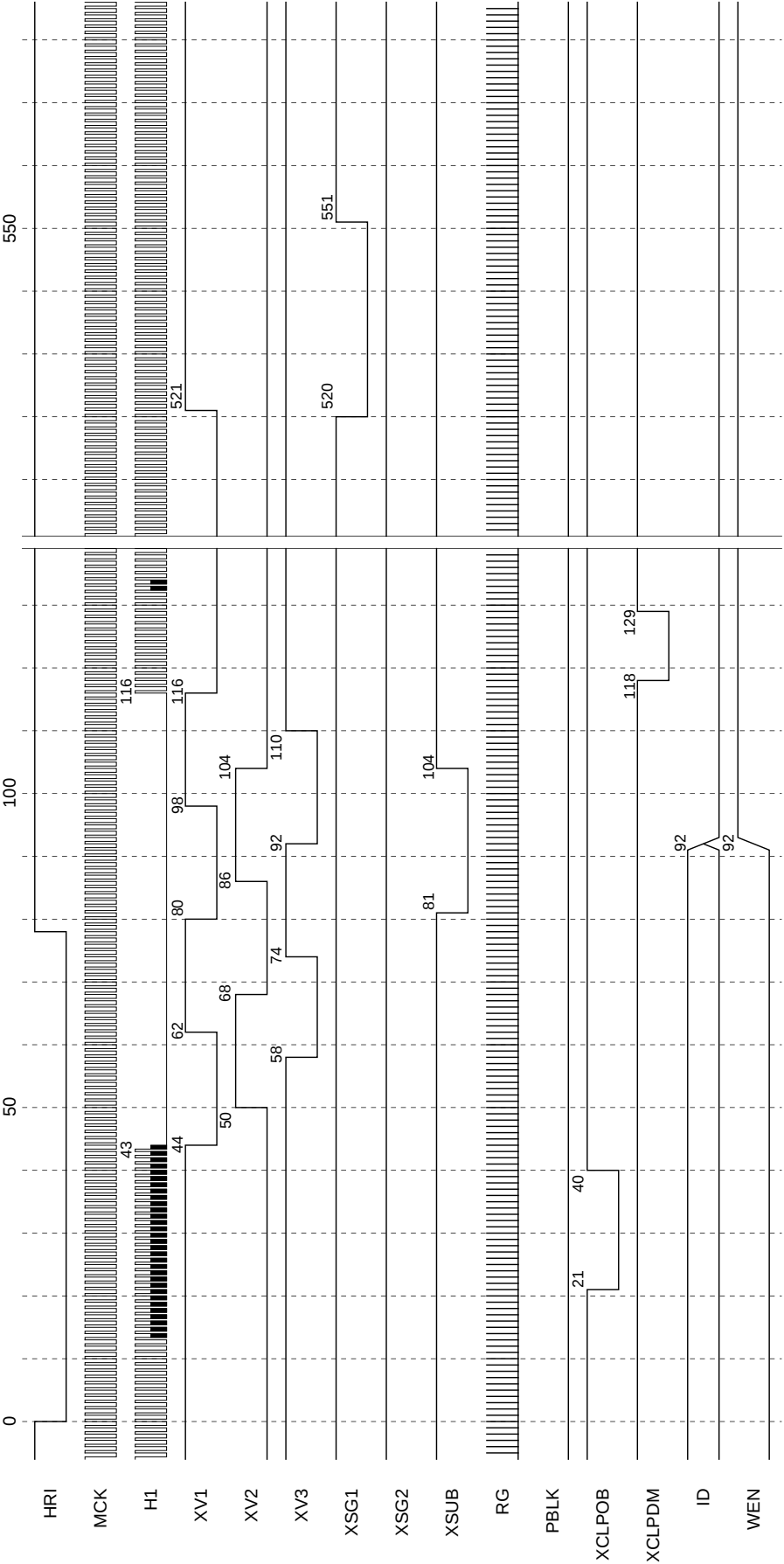


- * The HRI of this chart is equivalent to HRI¹ of Chart-7. This HRI indicates a timing that the CXD2452R takes in actually.
 - * The numbers at the output pulse transition points indicate the count at the MCK (780Hz) rise from the fall of HRI.
 - * The HRI fall interval should be between 3.6 to 9.4μs. This chart shows an interval of 780k (6.3μs).
- XSUB is output at the timing shown above when specified by the serial interface data.
- * The ID transition timing is synchronized with the fall of XV3.
 - * WEN is output during the horizontal interval shown in Chart-2. The transition timing is the same as that for ID.

Chart-6 Horizontal Direction Timing Chart

MODE (Base oscillation frequency: 2340fH)
Monitoring drive mode (readout portion)

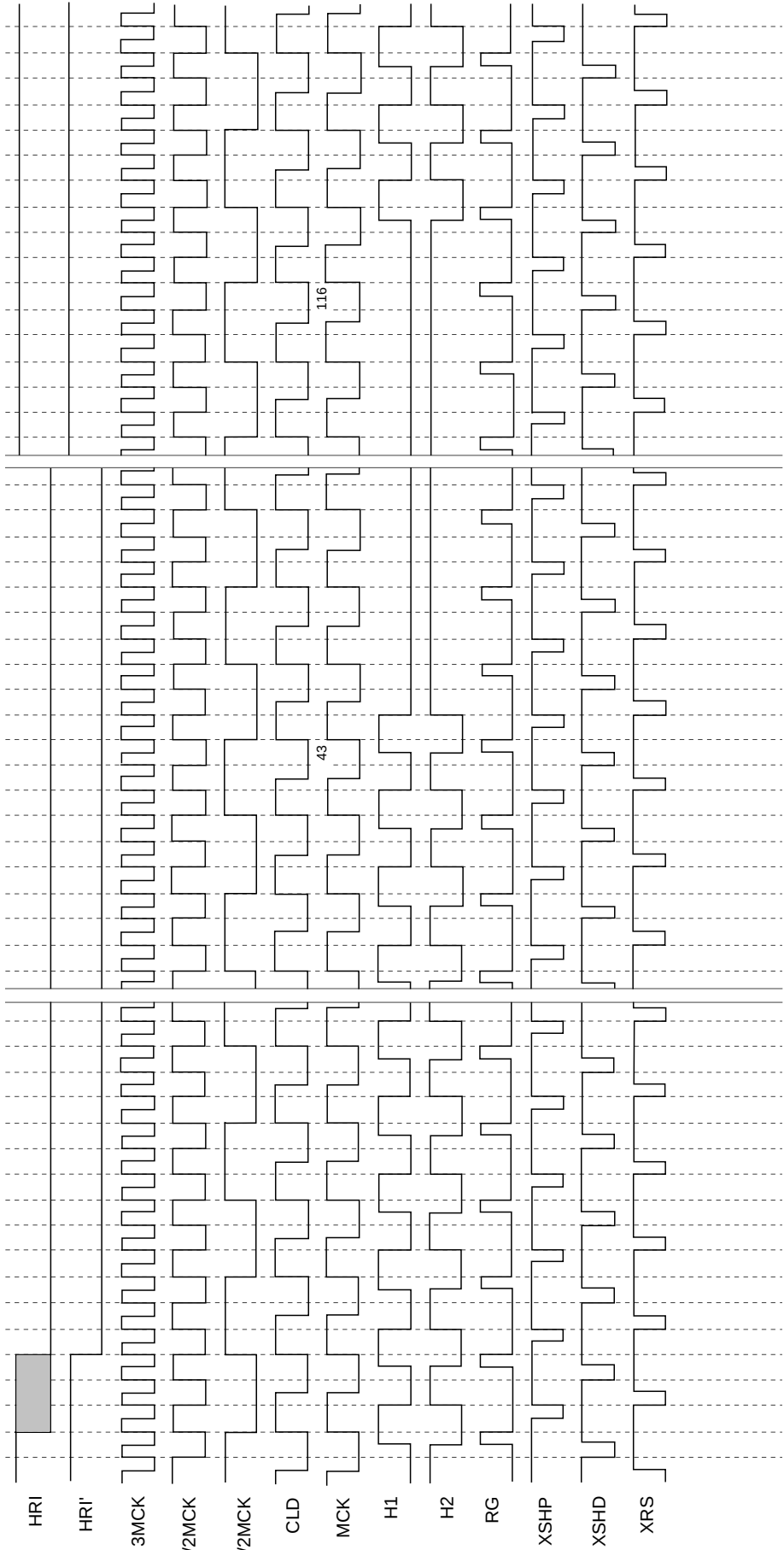
Applicable CCD image sensor
ICX098AK



* The HRI of this chart is equivalent to HRI' of Chart-7. This HRI indicates a timing that the CXD2452R takes in actually.
* The numbers at the output pulse transition points indicate the count at the MCK (780fH) rise from the fall of HRI.
* The HRI fall interval should be between 3.6 to 9.4μs. This chart shows an interval of 78ck (6.3μs).
* XSUB is output at the timing shown above when specified by the serial interface data.
* The ID transition timing is synchronized with the fall of XV3. ID is reset low at this timing during the readout horizontal interval.
* WEN is output during the horizontal interval shown in Chart-2. The transition timing is the same as that for ID.

Chart-7 High-speed Phase Timing Chart

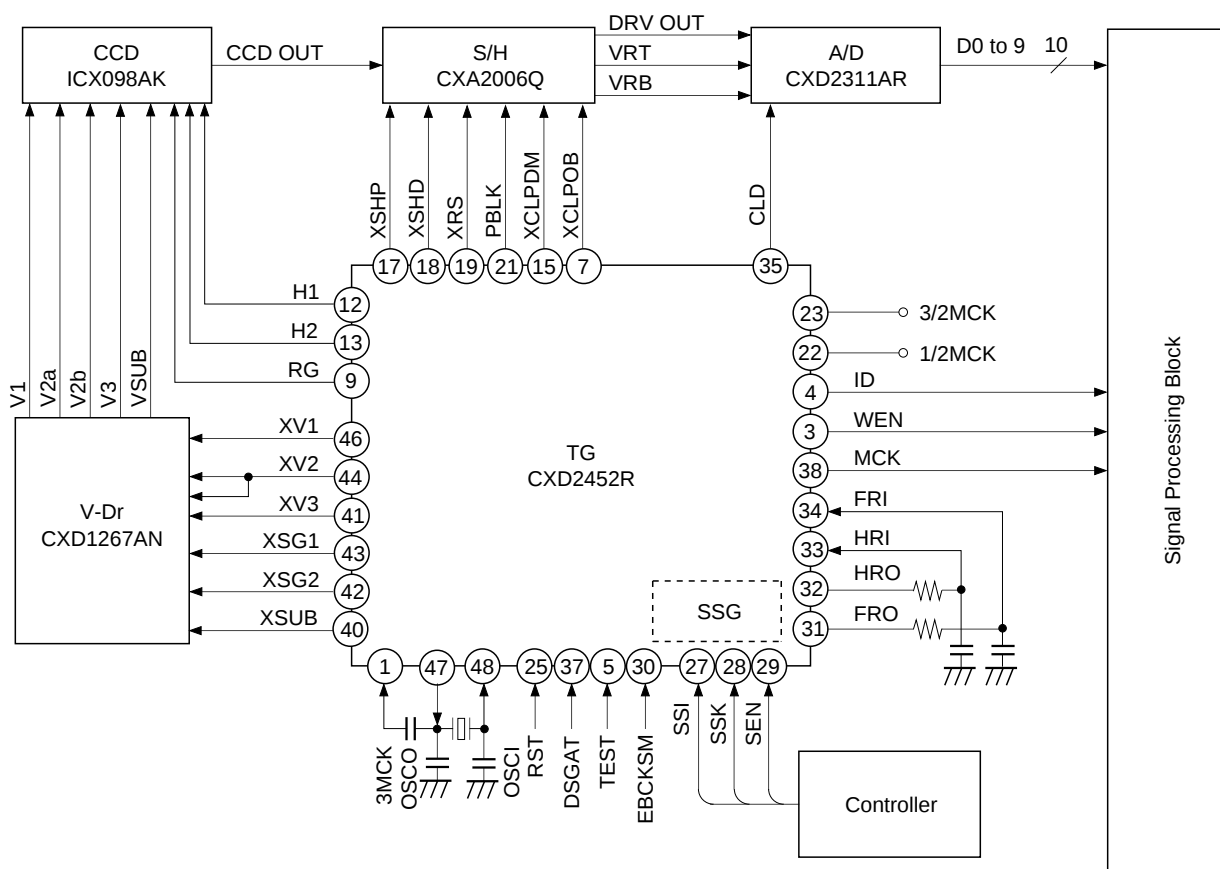
MODE (Base oscillation frequency: 2340fh)
Applicable CCD image sensor
ICX098AK



* HRI' indicates the HRI, which is a timing that taken in actually.

* 3/2MCK and 1/2MCK can inverse polarity according to each serial interface data. This chart indicates that 3/2 MCK is negative polarity; 1/2 MCK is positive polarity.

Application Circuit Block Diagram

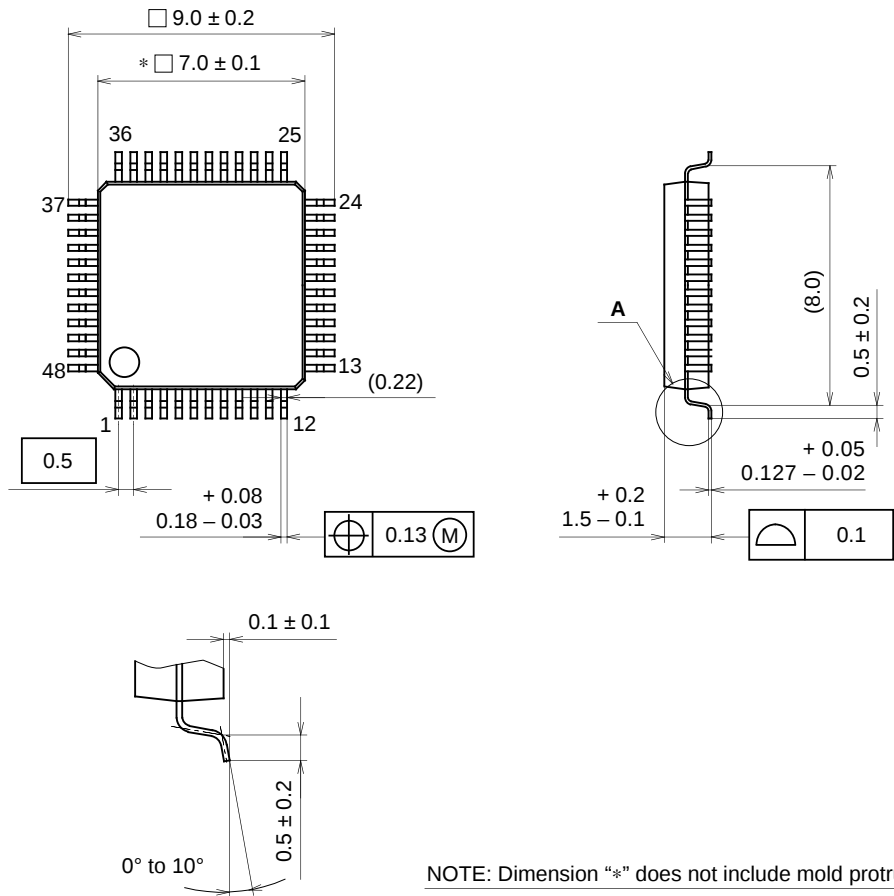


Note) When the CXD2311AR is used as A/D converter, CLD must be inverted.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	LQFP-48P-L01	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	LQFP048-P-0707	LEAD TREATMENT	SOLDER/PALLADIUM PLATING
JEDEC CODE		LEAD MATERIAL	42/COPPER ALLOY
		PACKAGE MASS	0.2g