

## Timing Generator for LCD Panels

### Description

The CXD2436Q is a timing signal generator for the VGA LCD panel LCX012 driver. This chip has a built-in serial interface circuit which allows the mode to be switched with respect to various VGA signals through direct control from an external microcomputer, etc.

### Features

- Generates the LCX012 drive pulse.
- Supports three-panel projectors.
- Built-in serial interface circuit
- Supports various VGA signals. (non-interlaced mode)
- Built-in 2-line pair drive circuits
- Supports NTSC and PAL systems.
- Supports up/down and/or right/left inversion.
- Supports line inversion and field inversion.
- Generates timing signal of external sample-and-hold circuit.

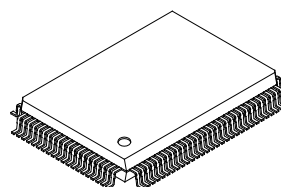
### Applications

LCD projectors, etc.

### Structure

Silicon gate CMOS IC

100 pin QFP (Plastic)



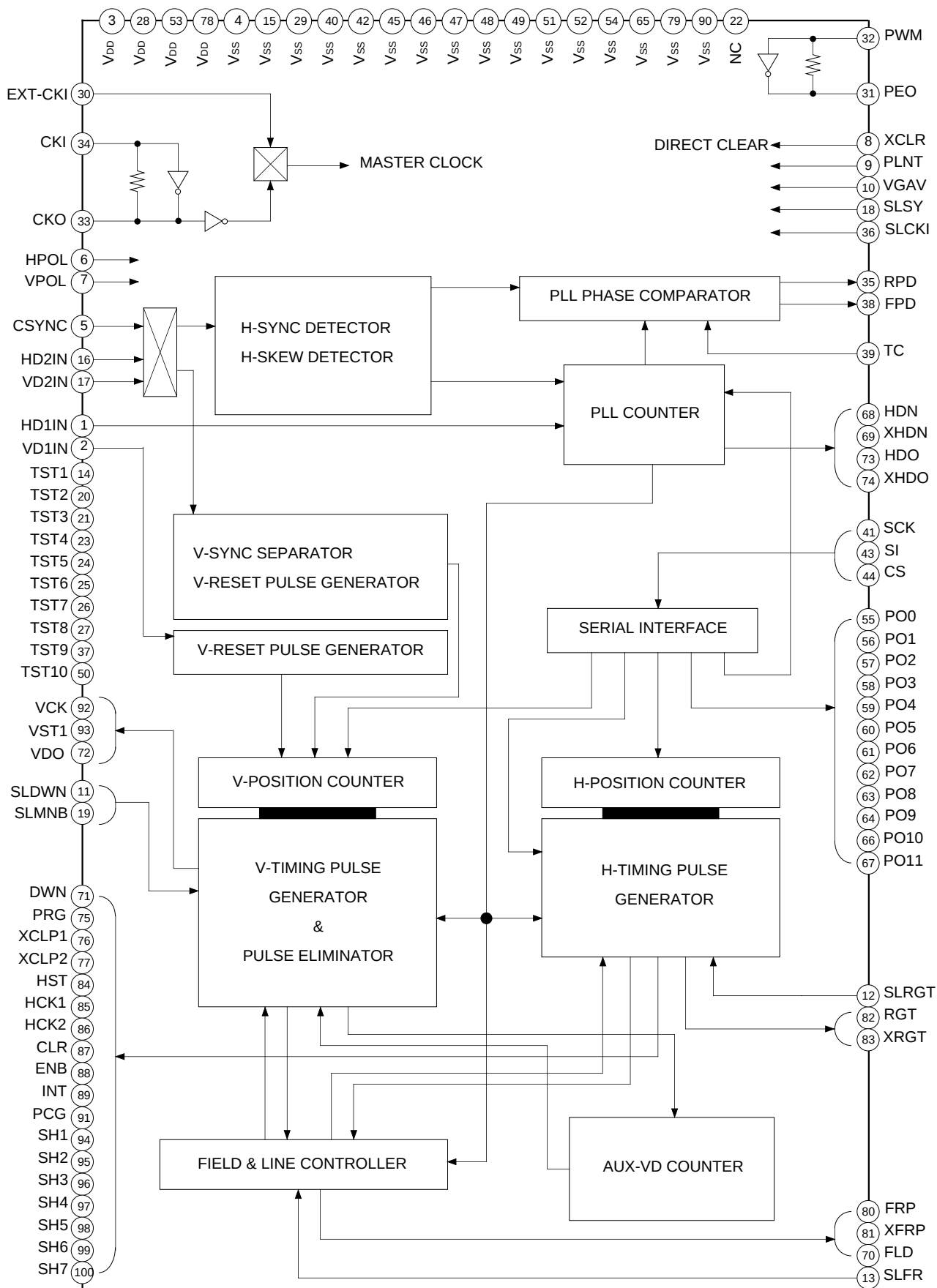
### Absolute Maximum Ratings (Ta=25 °C)

|                         |                 |                                              |    |
|-------------------------|-----------------|----------------------------------------------|----|
| • Supply voltage        | V <sub>DD</sub> | V <sub>SS</sub> −0.5 to +7.0                 | V  |
| • Input voltage         | V <sub>I</sub>  | V <sub>SS</sub> −0.5 to V <sub>DD</sub> +0.5 | V  |
| • Output voltage        | V <sub>O</sub>  | V <sub>SS</sub> −0.5 to V <sub>DD</sub> +0.5 | V  |
| • Operating temperature | Topr            | −20 to +75                                   | °C |
| • Storage temperature   | Tstg            | −55 to +150                                  | °C |

### Recommended Operating Conditions

|                  |                 |              |    |
|------------------|-----------------|--------------|----|
| • Supply voltage | V <sub>DD</sub> | +4.5 to +5.5 | V  |
| • Supply voltage | V <sub>CC</sub> | −20 to +75   | °C |

# Block Diagram



## Pin Description

| Pin No. | Symbol           | I/O | Description                                                                                  | Input pin for open status |
|---------|------------------|-----|----------------------------------------------------------------------------------------------|---------------------------|
| 1       | HD1IN            | I   | Hsync input (VGA)                                                                            | —                         |
| 2       | VD1IN            | I   | Vsync input (VGA)                                                                            | —                         |
| 3       | V <sub>DD</sub>  | —   | Power supply                                                                                 | —                         |
| 4       | V <sub>SS</sub>  | —   | GND                                                                                          | —                         |
| 5       | CSYNC            | I   | Composite sync input (NTSC/PAL)                                                              | —                         |
| 6       | HPOL             | I   | HD, CSYNC polarity identification input<br>(High: positive polarity, Low: negative polarity) | H                         |
| 7       | VPOL             | I   | VD, CSYNC polarity identification input<br>(High: positive polarity, Low: negative polarity) | H                         |
| 8       | XCLR             | I   | External clear (all clear when Low)                                                          | H                         |
| 9       | PLNT             | I   | PAL/NTSC switching (High: NTSC, Low: PAL)                                                    | H                         |
| 10      | VGA <sub>V</sub> | I   | VGA (NTSC/PAL) switching (High: VGA, Low: NTSC/PAL)                                          | H                         |
| 11      | SLDWN            | I   | Up/down inversion discrimination signal input<br>(High: Down, Low: Up)                       | H                         |
| 12      | SLRGT            | I   | Right/left inversion discrimination signal input<br>(High: Normal, Low: Reverse)             | H                         |
| 13      | SLFR             | I   | 1H/1F inversion switching (High: 1H, Low: 1F)                                                | H                         |
| 14      | TST1             | I   | Test pin (Not connected or High.)                                                            | H                         |
| 15      | V <sub>SS</sub>  | —   | GND                                                                                          | —                         |
| 16      | HD2IN            | I   | HD2 input (for NTSC/PAL separate-sync)                                                       | —                         |
| 17      | VD2IN            | I   | VD2 input (for NTSC/PAL separate-sync)                                                       | —                         |
| 18      | SLSY             | I   | SYNC input switching (High: CSYNC, Low: HD2IN and VD2IN)                                     | H                         |
| 19      | SLMNB            | I   | Switches mode (High: Nothing, Low: 400 → 480 line conversion)                                | H                         |
| 20      | TST2             | I   | Test pin (Not connected or High.)                                                            | H                         |
| 21      | TST3             | I   | Test pin (Connect to GND.)                                                                   | H                         |
| 22      | N.C.             | —   | N.C.                                                                                         | —                         |
| 23      | TST4             | —   | Test pin (Not connected or High.)                                                            | —                         |
| 24      | TST5             | —   | Test pin (Not connected or High.)                                                            | —                         |
| 25      | TST6             | —   | Test pin (Not connected or High.)                                                            | —                         |
| 26      | TST7             | —   | Test pin (Not connected.)                                                                    | —                         |
| 27      | TST8             | —   | Test pin (Connect to GND.)                                                                   | —                         |
| 28      | V <sub>DD</sub>  | —   | Power supply                                                                                 | —                         |
| 29      | V <sub>SS</sub>  | —   | GND                                                                                          | —                         |
| 30      | EXT-CKI          | I   | External clock input                                                                         | —                         |
| 31      | PEO              | I/O | Loop filter integrator output                                                                | —                         |
| 32      | PWM              | I   | Loop filter integrator input                                                                 | —                         |
| 33      | CKO              | I/O | Oscillation cell output (NTSC/PAL)                                                           | —                         |
| 34      | CKI              | I   | Oscillation cell input (NTSC/PAL)                                                            | —                         |
| 35      | RPD              | O   | Phase comparator output (NTSC/PAL)                                                           | —                         |
| 36      | SLCKI            | I   | Clock input selection (High: CKI, Low: EXT-CKI)<br>(NTSC/PAL mode only)                      | H                         |
| 37      | TST9             | I   | Test pin (Not connected or High.)                                                            | H                         |
| 38      | FPD              | O   | Phase comparator output (NTSC/PAL)                                                           | —                         |

| Pin No. | Symbol          | I/O | Description                                       | Input pin for open status |
|---------|-----------------|-----|---------------------------------------------------|---------------------------|
| 39      | TC              | I/O | FPD pin pulse width adjustment                    | —                         |
| 40      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 41      | SCK             | I   | Serial interface clock input                      | H                         |
| 42      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 43      | SI              | I   | Serial interface data input                       | L                         |
| 44      | CS              | I   | Serial interface chip select                      | H                         |
| 45      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 46      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 47      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 48      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 49      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 50      | TST10           | I   | Test pin (Not connected or High.)                 | H                         |
| 51      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 52      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 53      | V <sub>DD</sub> | —   | Power supply                                      | —                         |
| 54      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 55      | PO0             | O   | Serial I/O data output                            | —                         |
| 56      | PO1             | O   | Serial I/O data output                            | —                         |
| 57      | PO2             | O   | Serial I/O data output                            | —                         |
| 58      | PO3             | O   | Serial I/O data output                            | —                         |
| 59      | PO4             | O   | Serial I/O data output                            | —                         |
| 60      | PO5             | O   | Serial I/O data output                            | —                         |
| 61      | PO6             | O   | Serial I/O data output                            | —                         |
| 62      | PO7             | O   | Serial I/O data output                            | —                         |
| 63      | PO8             | O   | Serial I/O data output                            | —                         |
| 64      | PO9             | O   | Serial I/O data output                            | —                         |
| 65      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 66      | PO10            | O   | Serial I/O data output                            | —                         |
| 67      | PO11            | O   | Serial I/O data output                            | —                         |
| 68      | HDN             | O   | Phase comparator output (positive polarity)       | —                         |
| 69      | XHDN            | O   | Phase comparator output (negative polarity)       | —                         |
| 70      | FLD             | O   | Field discrimination signal output                | —                         |
| 71      | DWM             | O   | Up/down inversion discrimination signal output    | —                         |
| 72      | VDO             | O   | VD pulse output (positive polarity)               | —                         |
| 73      | HDO             | O   | HD pulse output (positive polarity)               | —                         |
| 74      | XHDO            | O   | HD pulse output (negative polarity)               | —                         |
| 75      | PRG             | O   | Precharge signal pulse (positive polarity)        | —                         |
| 76      | XCLP1           | O   | Pedestal clamp pulse 1                            | —                         |
| 77      | XCLP2           | O   | Pedestal clamp pulse 2                            | —                         |
| 78      | V <sub>DD</sub> | —   | Power supply                                      | —                         |
| 79      | V <sub>SS</sub> | —   | GND                                               | —                         |
| 80      | FRP             | O   | AC drive inversion timing output                  | —                         |
| 81      | XFRP            | O   | AC drive inversion timing output                  | —                         |
| 82      | RGT             | O   | Right/left inversion discrimination signal output | —                         |

| Pin No. | Symbol          | I/O | Description                                       | Input pin for open status |
|---------|-----------------|-----|---------------------------------------------------|---------------------------|
| 83      | XRGT            | O   | Right/left inversion discrimination signal output | —                         |
| 84      | HST             | O   | H start pulse output (positive polarity)          | —                         |
| 85      | HCK1            | O   | H clock pulse 1 output                            | —                         |
| 86      | HCK2            | O   | H clock pulse 2 output                            | —                         |
| 87      | CLR             | O   | CLR pin output                                    | —                         |
| 88      | ENB             | O   | ENB pin output                                    | —                         |
| 89      | INT             | O   | INT pin output                                    | —                         |
| 90      | V <sub>SS</sub> | O   | GND                                               | —                         |
| 91      | PCG             | O   | PCG pin output (positive polarity)                | —                         |
| 92      | VCK             | O   | V clock pulse output                              | —                         |
| 93      | VST1            | O   | V start pulse output                              | —                         |
| 94      | SH1             | O   | Sample-and-hold pulse 1 (positive polarity)       | —                         |
| 95      | SH2             | O   | Sample-and-hold pulse 2 (positive polarity)       | —                         |
| 96      | SH3             | O   | Sample-and-hold pulse 3 (positive polarity)       | —                         |
| 97      | SH4             | O   | Sample-and-hold pulse 4 (positive polarity)       | —                         |
| 98      | SH5             | O   | Sample-and-hold pulse 5 (positive polarity)       | —                         |
| 99      | SH6             | O   | Sample-and-hold pulse 6 (positive polarity)       | —                         |
| 100     | SH7             | O   | Sample-and-hold pulse 7 (positive polarity)       | —                         |

## Electrical Characteristics

### 1. DC characteristics

(Temperature = 25 °C, V<sub>SS</sub> = 0 V)

| Item                | Symbol          | Conditions                            | Min.                 | Typ. | Max.                | Unit | Applicable pins                                          |
|---------------------|-----------------|---------------------------------------|----------------------|------|---------------------|------|----------------------------------------------------------|
| Supply voltage      | V <sub>DD</sub> |                                       | 4.5                  | 5.0  | 5.5                 | V    |                                                          |
| Input voltage 1     | VIH1            | CMOS input cell                       | 0.7 V <sub>DD</sub>  |      |                     | V    | Input pins other than those noted below                  |
|                     | VIL1            |                                       |                      |      | 0.3 V <sub>DD</sub> |      |                                                          |
| Input voltage 2     | VIH2            | CMOS Schmitt trigger input cell       | 0.8 V <sub>DD</sub>  |      |                     | V    | HDnIN, VDnIN, CSYNC, CKI, PWM, TC, PEO, CKO, SI, SCK, CS |
|                     | VIL2            |                                       |                      |      | 0.2 V <sub>DD</sub> |      |                                                          |
|                     | VT+ -VT+        |                                       |                      | 0.6  |                     |      |                                                          |
| Output voltage 1    | VOH             | IOH=−2 mA                             | V <sub>DD</sub> −0.8 |      |                     | V    | Output pins other than those noted below                 |
|                     | VOL             | IOL=4 mA                              |                      |      | 0.4                 |      |                                                          |
| Output voltage 2    | VOH             | IOH=−4 mA                             | V <sub>DD</sub> −0.8 |      |                     | V    | VCK                                                      |
|                     | VOL             | IOL=8 mA                              |                      |      | 0.4                 |      |                                                          |
| Output voltage 3    | VOH             | IOH=−6 mA                             | V <sub>DD</sub> −0.8 |      |                     | V    | HCKn, SHn, HST                                           |
|                     | VOL             | IOL=12 mA                             |                      |      | 0.4                 |      |                                                          |
| Output voltage 4    | VOH             | IOH=−3 mA                             | V <sub>DD</sub> /2   |      |                     | V    | CKO, PEO                                                 |
|                     | VOL             | IOL=3 mA                              |                      |      | V <sub>DD</sub> /2  |      |                                                          |
| Input leak current  | IIL             | Pull-up resistor connected            | −40                  | −100 | −240                | μA   | *1                                                       |
|                     | IIH             | Pull-down resistor connected          | 40                   | 100  | 240                 |      | SI                                                       |
| Output leak current | ILZ             | High impedance status                 | −40                  |      | 40                  | μA   | RPD, FPD                                                 |
| Current consumption | IDD             | fclk=31 MHz<br>V <sub>DD</sub> =5.0 V |                      | 55   |                     | mA   | At no load                                               |

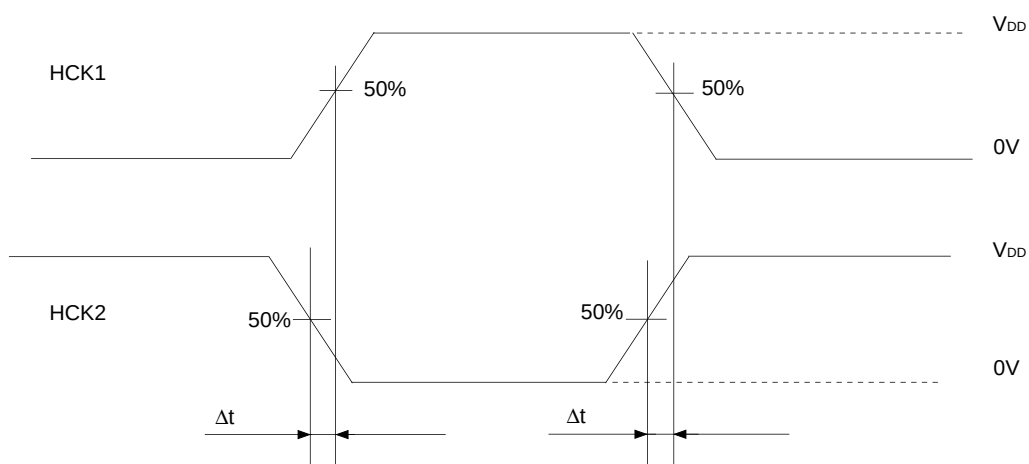
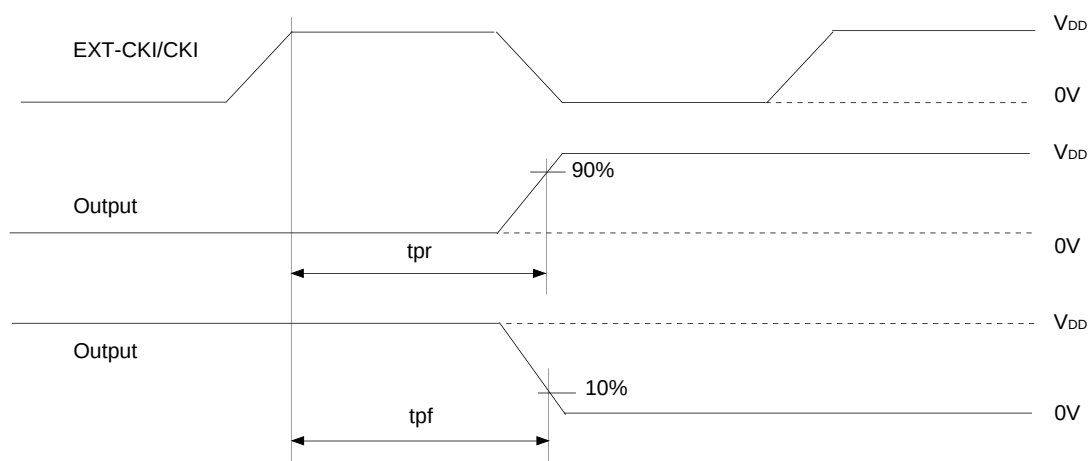
\*1 Input pins with pull-up resistors

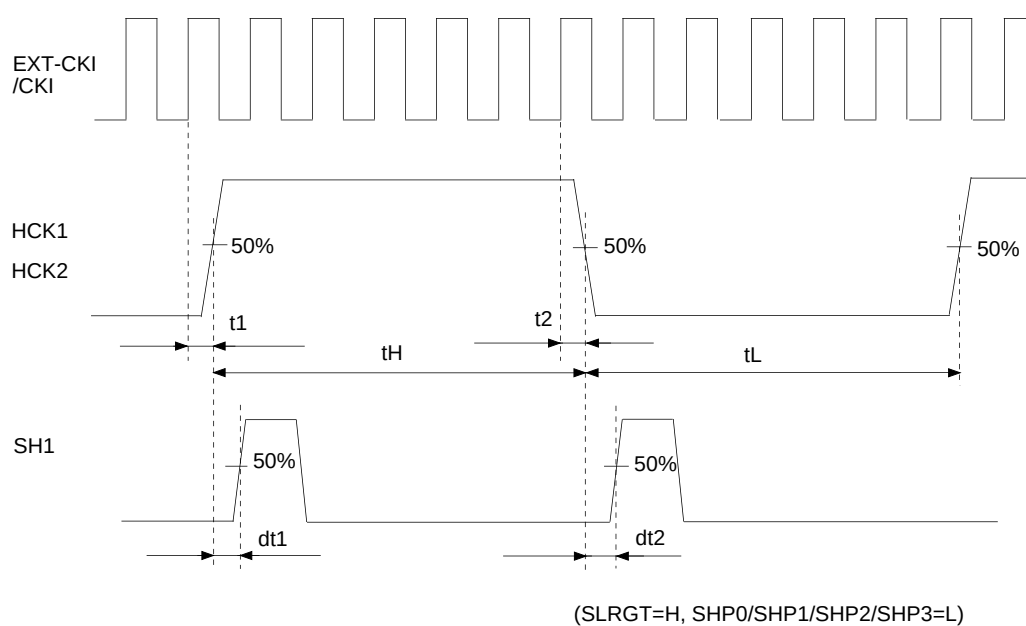
HPOL, VPOL, XCLR, PLNT, VGAV, SLDWN, SLRGT, SLFR, TST1, SLSY, TST2, TST3, SLCKI, TST9, SCK, CS

## 2. AC characteristics

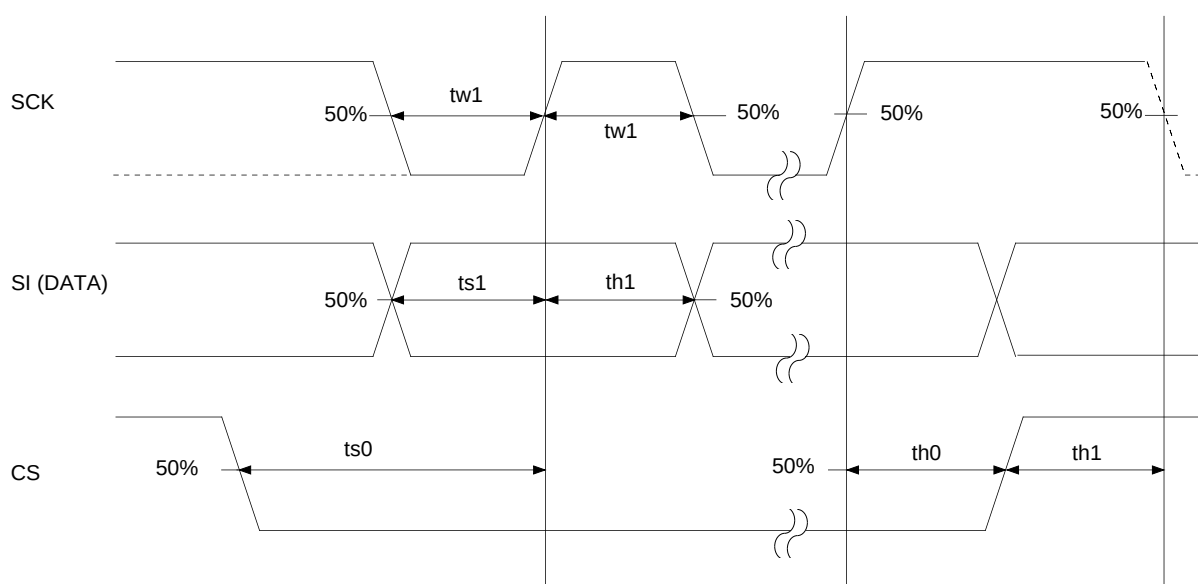
(V<sub>DD</sub>=5.0 V±0.5 V, V<sub>SS</sub>=0 V)

| Item                               | Applicable pins            | Symbol                                         | Conditions | Min. | Typ. | Max. | Unit |
|------------------------------------|----------------------------|------------------------------------------------|------------|------|------|------|------|
| Clock input cycle                  | EXT-CKI, CKI               |                                                |            | 25   |      |      | ns   |
| Cross-point time difference        | HCK1, 2                    | $\Delta t$                                     | CL=30 pF   | -10  |      | 10   | ns   |
| Output rise delay                  | HCKn, SHn                  | t <sub>pr</sub>                                | CL=30 pF   |      |      | 20   | ns   |
| Output fall delay                  | HCKn, SHn                  | t <sub>pf</sub>                                | CL=30 pF   |      |      | 20   | ns   |
| Output rise delay                  | Other than<br>HCKn and SHn | t <sub>pr</sub>                                | CL=30 pF   |      |      | 30   | ns   |
| Output fall delay                  | Other than<br>HCKn and SHn | t <sub>pf</sub>                                | CL=30 pF   |      |      | 30   | ns   |
| HCK1, SH1 delay<br>time difference | HCK1, SH1                  | dt1                                            | CL=30 pF   |      |      | 10   | ns   |
| HCK2, SH1 delay<br>time difference | HCK2, SH1                  | dt2                                            | CL=30 pF   |      |      | 10   | ns   |
| HCK1 duty                          | HCK1                       | t <sub>H</sub> /t <sub>H</sub> +t <sub>L</sub> | CL=30 pF   | 48   | 50   | 52   | %    |
| HCK2 duty                          | HCK2                       | t <sub>H</sub> /t <sub>H</sub> +t <sub>L</sub> | CL=30 pF   | 48   | 50   | 52   | %    |





### 3. Serial interface block AC characteristics



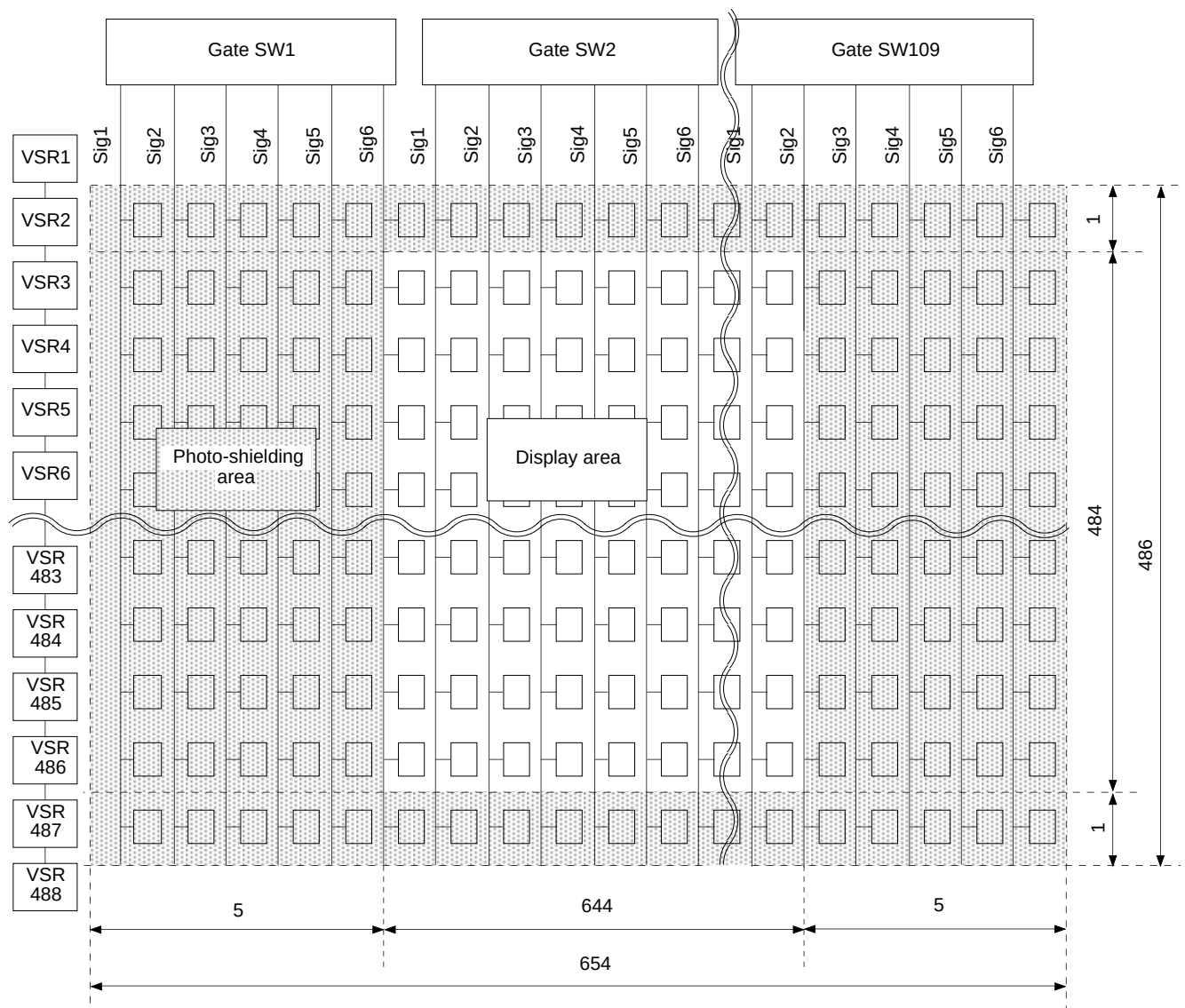
( $V_{DD}=5.0\text{ V}\pm 0.5\text{ V}$ ,  $V_{SS}=0\text{ V}$ ,  $T_{opr}=-20\text{ to }+75\text{ }^{\circ}\text{C}$ )

| Symbol | Item                                                | Min.   | Max. |
|--------|-----------------------------------------------------|--------|------|
| ts1    | SI setup time with respect to rise of SCK           | 200 ns |      |
| th1    | SI hold time with respect to rise of SCK            | 200 ns |      |
| tw1    | SCK pulse width                                     | 200 ns |      |
| ts0    | CS setup time with respect to rise of SCK           | 200 ns | 2tw1 |
| th0    | CS hold time with respect to rise of SCK            | 200 ns | 2tw1 |
| th1    | SCK high-level hold time with respect to rise of CS | 200 ns |      |

## LCD Panel Structure

The structure of LCD panels (LCX012AL) driven by this IC is shown below.

The dot arrangement is a square arrangement, and the shaded region within the diagram is not displayed.



- The effective pixels are horizontal: 644 pixels and vertical: 484 pixels.
- The horizontal pixel start position is from Sig6 of the first-stage scanner. (Sig1 to Sig5 of the first-stage scanner are the photo-shielding area and are not displayed.)
- The vertical pixel start position is from the third-stage scanner.
- These relationships are the same even during up/down and/or right/left inversion. (The entire area within the panel is inverted.)



## Description of Operation

### • Sync input pins

The CXD2436Q has three types of sync input pins.

| Pin No.  | Symbol         | SLSY setting | Application                           |
|----------|----------------|--------------|---------------------------------------|
| 1<br>2   | HD1IN<br>VD1IN | —            | SYNC input pins for VGA               |
| 5        | CSYNC          | H            | CSYNC input pin for NTSC/PAL          |
| 16<br>17 | HD2IN<br>VD2IN | L            | Separate SYNC input pins for NTSC/PAL |

### • Clock input pins

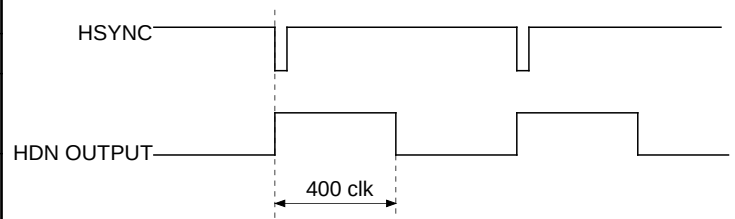
The CXD2436Q has two clock input pin systems to support two types of PLL circuits.

#### 1) When using EXT-CKI (using an external PLL IC)

The 1/N frequency divider output is output from the HDN and XHDN pins for the external PLL IC.

The used pins are shown in the following table. (SLCKI = Low)

| Pin No. | Symbol  | Application                                 |
|---------|---------|---------------------------------------------|
| 30      | EXT-CKI | Clock input                                 |
| 68      | HDN     | Phase comparison output (positive polarity) |
| 69      | XHDN    | Phase comparison output (negative polarity) |



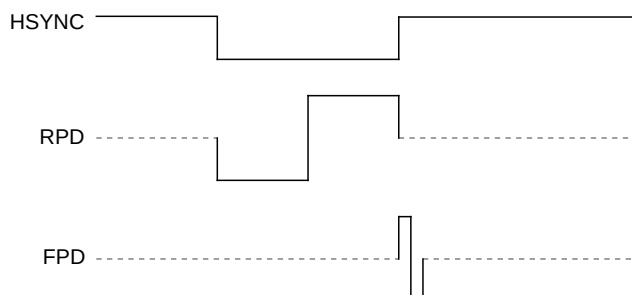
#### 2) When using CKI

This system uses the built-in phase comparator and an externally attached VCO circuit (see the Application Circuit).

This system is used during AV mode (NTSC/PAL).

The used pins are shown in the following table. (Effective when SLCKI is set to High.)

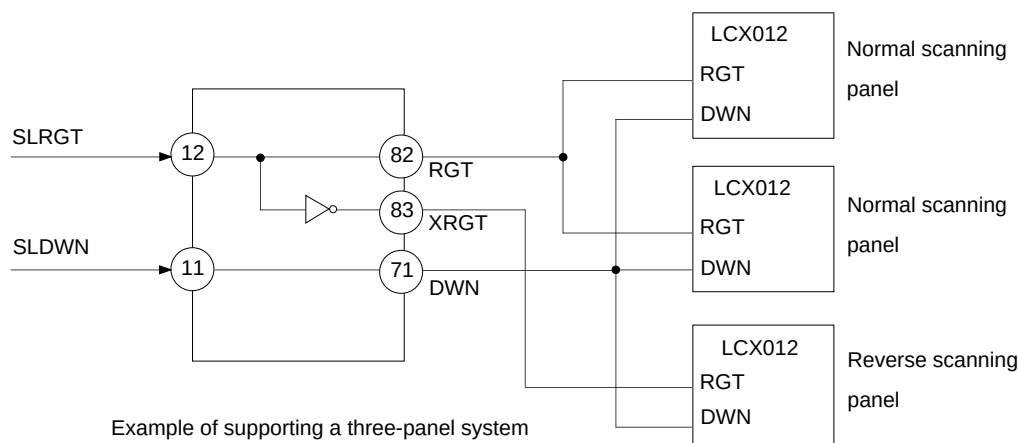
| Pin No. | Symbol | Application                            |
|---------|--------|----------------------------------------|
| 31      | PEO    | Loop filter integrator output          |
| 32      | PWM    | Loop filter integrator input           |
| 33      | CKO    | Clock output (oscillation cell output) |
| 34      | CKI    | Clock input (oscillation cell input)   |
| 35      | RPD    | Phase comparator output                |
| 38      | FPD    | Phase comparator output                |
| 39      | TC     | FPD pin pulse width adjustment         |



An outline of the output waveforms during PLL lock is shown in the figure to the left.

• **Connections supporting up/down and/or right/left inversion**

The CXD2436Q is designed for use with three-panel projectors, and has a system configuration which permits both normal and reverse scan. The RGT and XRGT output to the panel are switched according to the SLRGT input, and the DWN output is switched according to the SLDWN input in the same manner.



• **AC driving of LCD panels for no signal**

The following measures have been adopted to allow AC driving of LCD panels even when there is no signal.

- Horizontal direction pulse: The PLL is set to free running status. Therefore, the frequency of the horizontal direction pulse is dependent on the PLL free running frequency.
- Vertical direction pulse: The number of lines is counted by an internal counter and VST and FRP are output at a specified cycle.

• VST cycle for no signal

|      |      |
|------|------|
| NTSC | 269H |
| PAL  | 321H |
| VGA  | 526H |

• Free running detection timing

|      |      |
|------|------|
| NTSC | 291H |
| PAL  | 339H |
| VGA  | 873H |

Free running operates at the following cycles.

(No signal is judged if there is no VSYNC input for longer than the following periods.)

• **Description of the MODE selector switch**

- VGA/AV (NTSC/PAL) switching is performed with two pins.

| VGAV | PLNT | MODE |
|------|------|------|
| H    | H    | VGA  |
| H    | L    | VGA  |
| L    | H    | NTSC |
| L    | L    | PAL  |

- The HD1IN, HD2IN, VD1IN, VD2IN and CSYNC input polarities are supported by two pins.

| HPOL | VPOL | HD1IN<br>HD2IN    | VD1IN<br>VD2IN    | CSYNC             |
|------|------|-------------------|-------------------|-------------------|
| H    | H    | Positive polarity | Positive polarity | Positive polarity |
| H    | L    | Positive polarity | Negative polarity | —                 |
| L    | H    | Negative polarity | Positive polarity | —                 |
| L    | L    | Negative polarity | Negative polarity | Negative polarity |

- XCLR (External clear)

Reset should be performed during startup in order to initialize the serial interface. Performing external clear sets all serial interface modes to Low.

- **Serial interface specifications**

The CXD2436Q can set and switch the driving mode with the serial interface.

Set the corresponding timing data for each VGA signal according to the format in the diagram below. Be sure to make the initial mode settings. (See the AC characteristics for detailed timing specifications.)

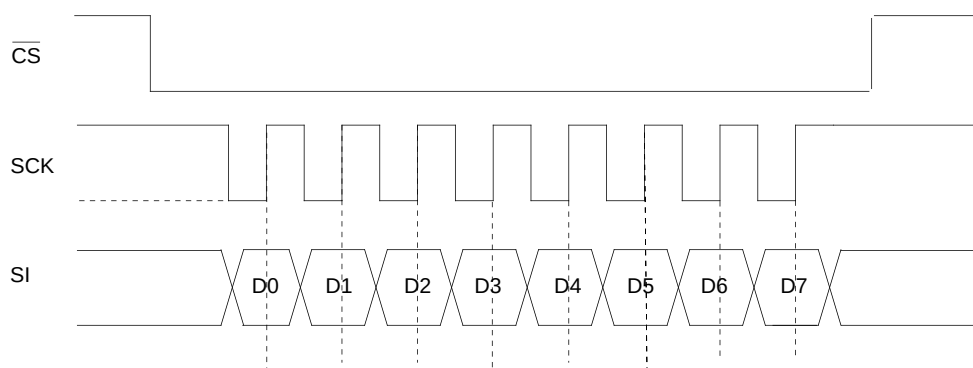


Fig. 1. Timing chart for the serial interface input block

**Note)** D0 to D7 internal transfer is completed by the  $\overline{CS}$  signal switching from a Low to High pulse. Therefore, the data should be transferred in 1-byte units with the  $\overline{CS}$  signal reset each time.

- **Description of mode switching settings using the serial interface**

The CXD2436Q can set the following six modes.

- (1) Frequency division ratio setting for the 1/N frequency divider of the master clock PLL circuit block.
- (2) H screen center adjustment. The center changes by one dot with LSB.
- (3) V screen center adjustment. The center changes by one line with LSB.
- (4) Sample-and-hold circuit phase adjustment. The phase changes by a half-dot with LSB.  
(See the Description of Sample-and-Hold Timing for details.)
- (5) Clamp pulse timing adjustment (4-way)
- (6) Data output (Serial data is held and output.)

| Upper 4-bit<br>address value<br>D7 to D4 | Lower 4-bit data |       |       |       | Functions                      |
|------------------------------------------|------------------|-------|-------|-------|--------------------------------|
|                                          | D3               | D2    | D1    | D0    |                                |
| 0H                                       | PHP3             | PHP2  | PHP1  | PHP0  | PLL 1/N frequency<br>divisions |
| 1H                                       | PHP7             | PHP6  | PHP5  | PHP4  |                                |
| 2H                                       | —                | PHP10 | PHP9  | PHP8  |                                |
| 3H                                       | HP3              | HP2   | HP1   | HP0   | H screen center<br>adjustment  |
| 4H                                       | —                | HP6   | HP5   | HP4   |                                |
| 5H                                       | VP3              | VP2   | VP1   | VP0   | V screen center<br>adjustment  |
| 6H                                       | —                | VP6   | VP5   | VP4   |                                |
| 7H                                       | SHP3             | SHP2  | SHP1  | SHP0  | S/H timing                     |
| 8H                                       | —                | —     | CLPP1 | CLPP0 | Clamp timing                   |
| 9H                                       | PO3              | PO2   | PO1   | PO0   | Data output                    |
| AH                                       | PO7              | PO6   | PO5   | PO4   |                                |
| BH                                       | PO11             | PO10  | PO9   | PO8   |                                |

\* PHP0, HP0, VP0, SHP0, CLPP0

### • PLL 1/N frequency division ratio setting

For the frequency division ratio setting during VGA mode, set the value of the number of dots for the horizontal period –1 in PHP0-10.

(Example) When the horizontal period is set to 800 dots

PHP setting value =  $800-1 \rightarrow 799$  (01100011111 LSB)

| PHP | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|---|---|---|---|---|---|---|---|---|---|
|     | 0  | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

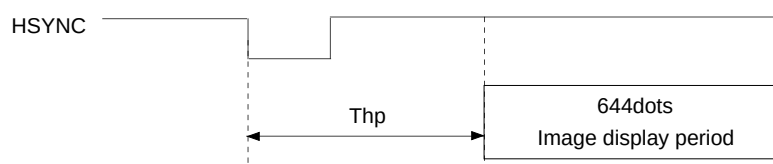
Set the value of the number of dots fixed to 816 during NTSC/PAL.

PHP setting value =  $816-1 \rightarrow 815$  (01100101111 LSB)

| PHP | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|---|---|---|---|---|---|---|---|---|---|
|     | 0  | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

### • Horizontal position setting

The horizontal display start position setting can be changed one dot at a time by the HP0 to 6 setting.

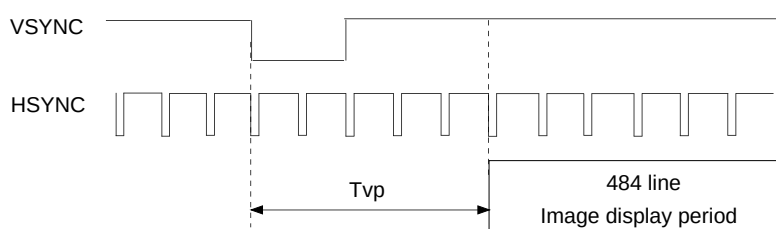


The maximum and minimum Thp values which can be set are shown in the following table.

| HP            | 6 | 5 | 4 | 3 | 2 | 1 | 0 | VGA      | NTSC         | PAL          |
|---------------|---|---|---|---|---|---|---|----------|--------------|--------------|
| Minimum value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 110 dots | 5.8 $\mu$ s  | 5.8 $\mu$ s  |
| Maximum value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 237 dots | 15.7 $\mu$ s | 15.8 $\mu$ s |

### • Vertical position setting

The vertical display start position setting can be changed one dot at a time by the VP0 to 6 setting.



The maximum and minimum Tvp values which can be set are shown in the following table.

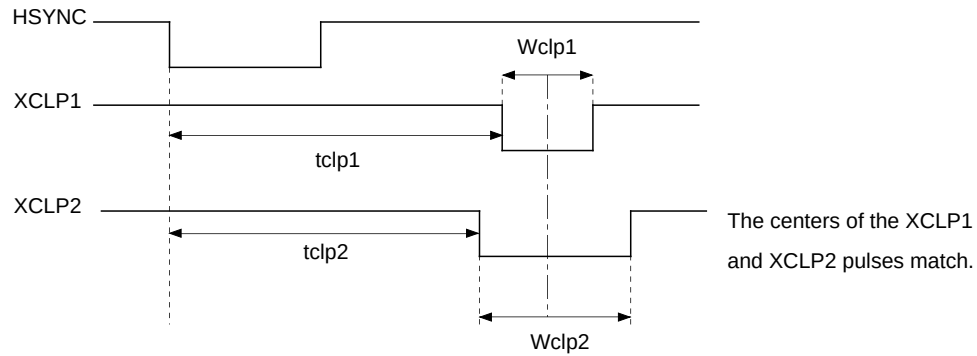
| VP            | 6 | 5 | 4 | 3 | 2 | 1 | 0 | VGA   | NTSC  | PAL   |
|---------------|---|---|---|---|---|---|---|-------|-------|-------|
| Minimum value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 5 H   | 14 H  | 14 H  |
| Maximum value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 133 H | 141 H | 141 H |

(This table shows the ODD field values for NTSC and PAL.)

### • CLP pulse position setting

The XCLP pulse position can be changed to four different positions. Each of these positions is shown below.

The XCLP pulse is linked with the horizontal position setting, and is indicated with the HP (1000000 LSB) setting.



### • VGA mode

| CLPP1 | CLPP0 | tclp1  | Wclp1  | tclp2  | Wclp2  |
|-------|-------|--------|--------|--------|--------|
| 0     | 0     | 74 dot | 40 dot | 61 dot | 67 dot |
| 0     | 1     | 81 dot | 40 dot | 68 dot | 67 dot |
| 1     | 0     | 88 dot | 40 dot | 75 dot | 67 dot |
| 1     | 1     | 95 dot | 40 dot | 82 dot | 67 dot |

### • NTSC mode

| CLPP1 | CLPP0 | tclp1        | Wclp1        | tclp2        | Wclp2        |
|-------|-------|--------------|--------------|--------------|--------------|
| 0     | 0     | 4.83 $\mu$ s | 1.17 $\mu$ s | 4.36 $\mu$ s | 2.18 $\mu$ s |
| 0     | 1     | 5.30 $\mu$ s | 1.17 $\mu$ s | 4.83 $\mu$ s | 2.18 $\mu$ s |
| 1     | 0     | 5.76 $\mu$ s | 1.17 $\mu$ s | 5.30 $\mu$ s | 2.18 $\mu$ s |
| 1     | 1     | 6.23 $\mu$ s | 1.17 $\mu$ s | 5.76 $\mu$ s | 2.18 $\mu$ s |

### • PAL mode

| CLPP1 | CLPP0 | tclp1        | Wclp1        | tclp2        | Wclp2        |
|-------|-------|--------------|--------------|--------------|--------------|
| 0     | 0     | 4.87 $\mu$ s | 1.18 $\mu$ s | 4.39 $\mu$ s | 2.20 $\mu$ s |
| 0     | 1     | 5.33 $\mu$ s | 1.18 $\mu$ s | 4.86 $\mu$ s | 2.20 $\mu$ s |
| 1     | 0     | 5.80 $\mu$ s | 1.18 $\mu$ s | 5.33 $\mu$ s | 2.20 $\mu$ s |
| 1     | 1     | 6.27 $\mu$ s | 1.18 $\mu$ s | 5.80 $\mu$ s | 2.20 $\mu$ s |

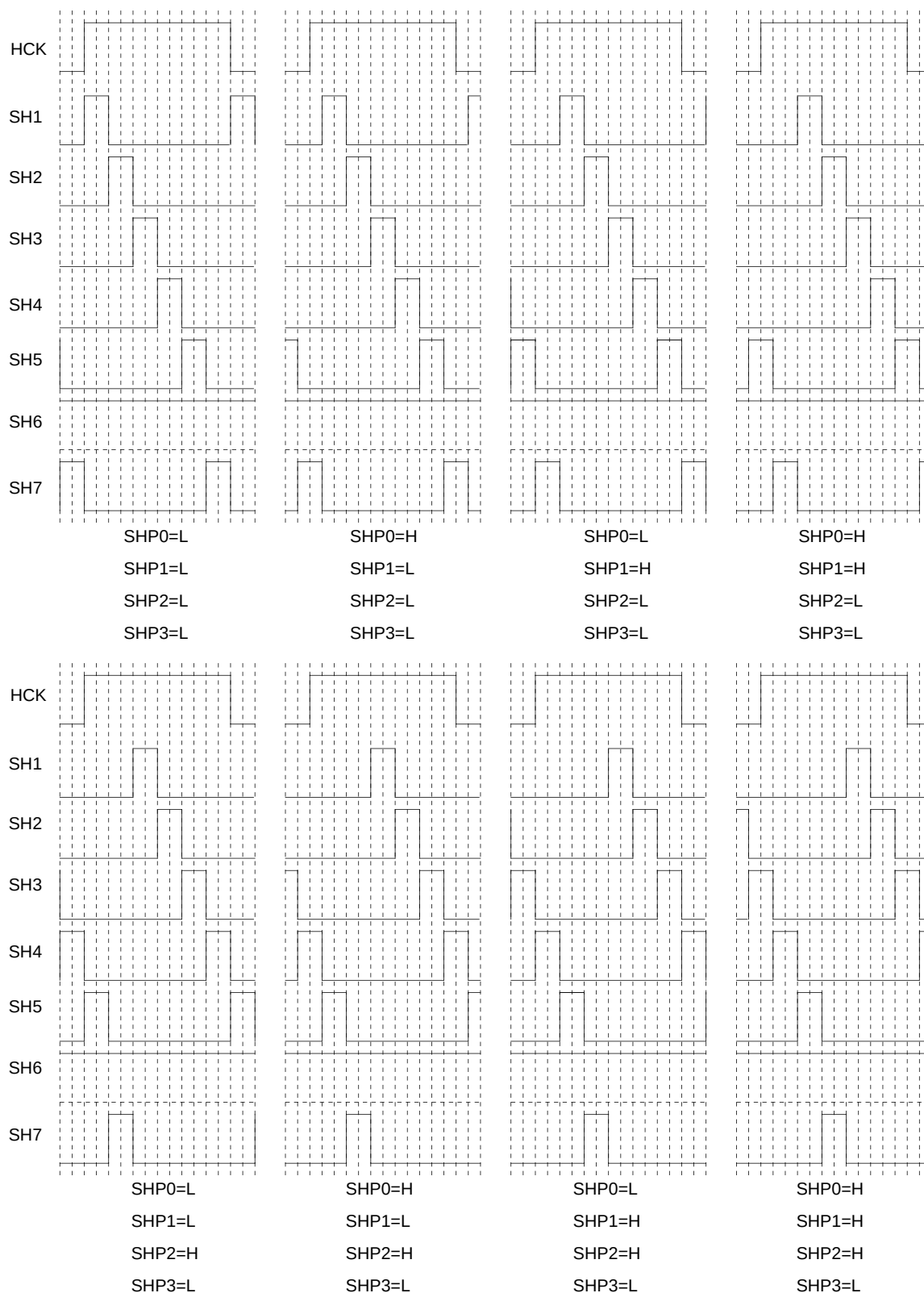
### • Switching the SH pulse timing

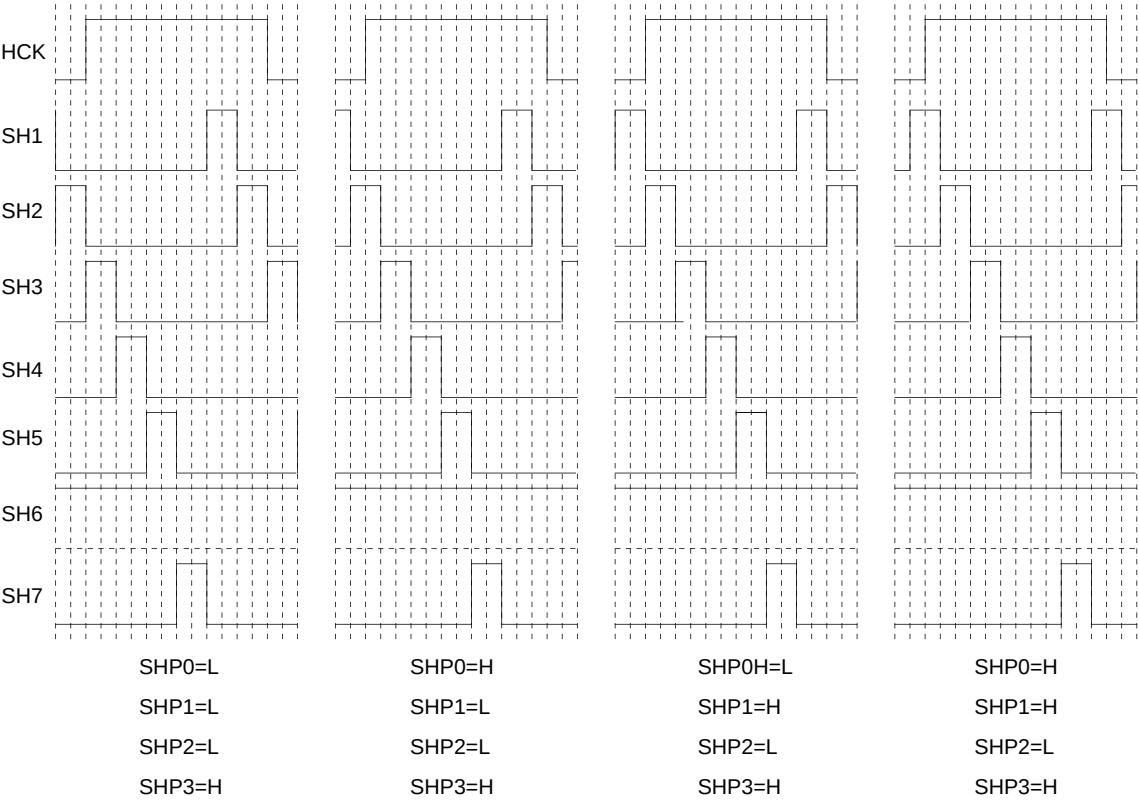
The phase relationship between the sample-and-hold pulses and HCK can be switched in 12 different ways with SHP0, SHP1, SHP2 and SHP3.

(This timing generator has a 0.5 DOT OFFSET function in order to ensure the phase margin.)

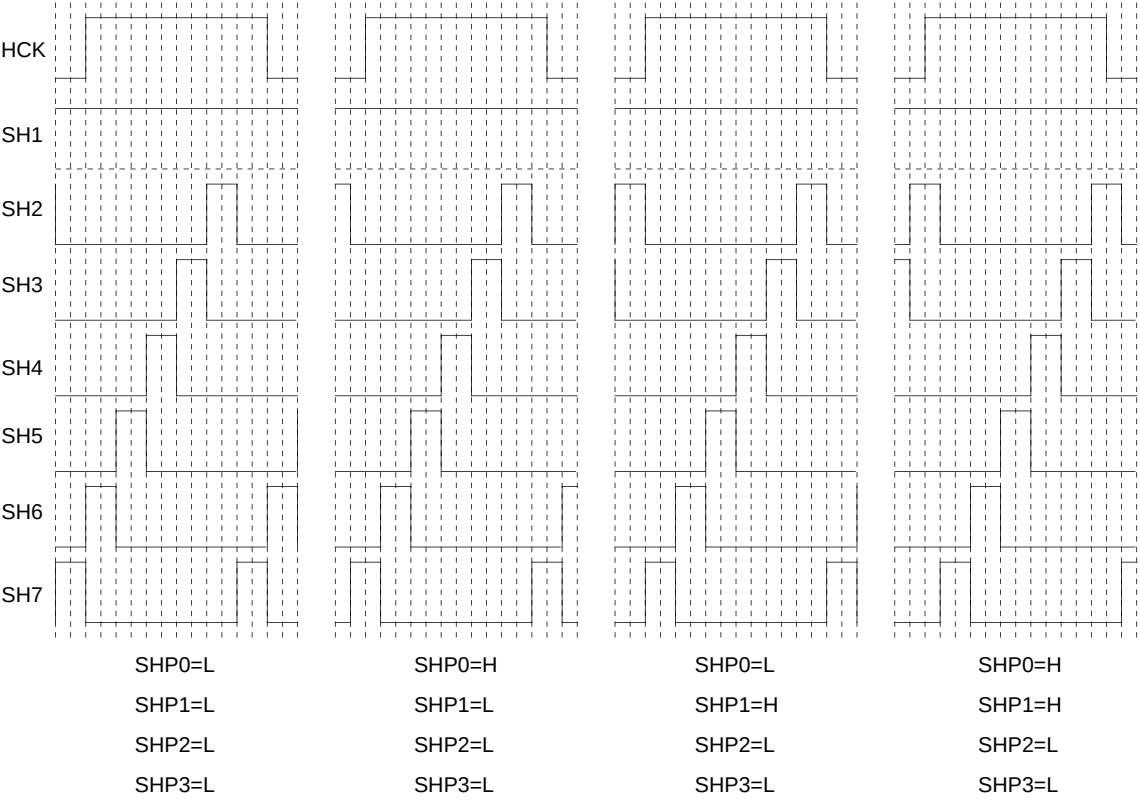
In addition, the timing differs according to the scanning direction (right/left scan).

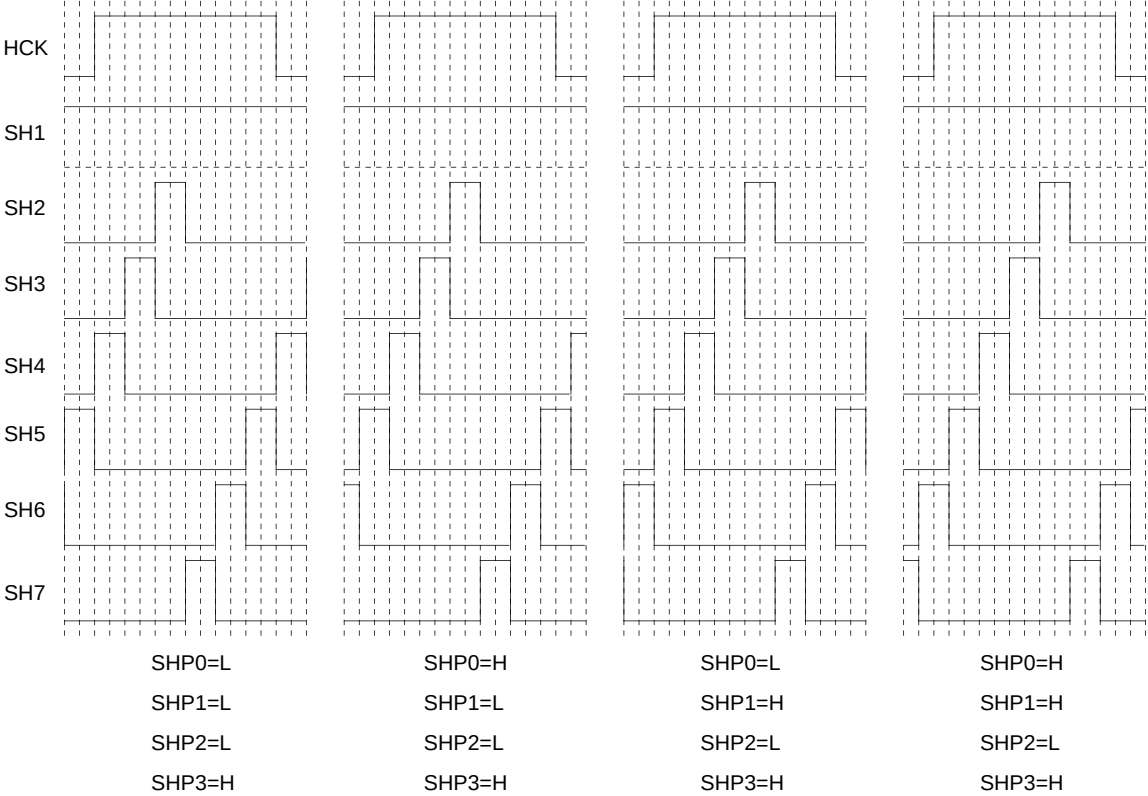
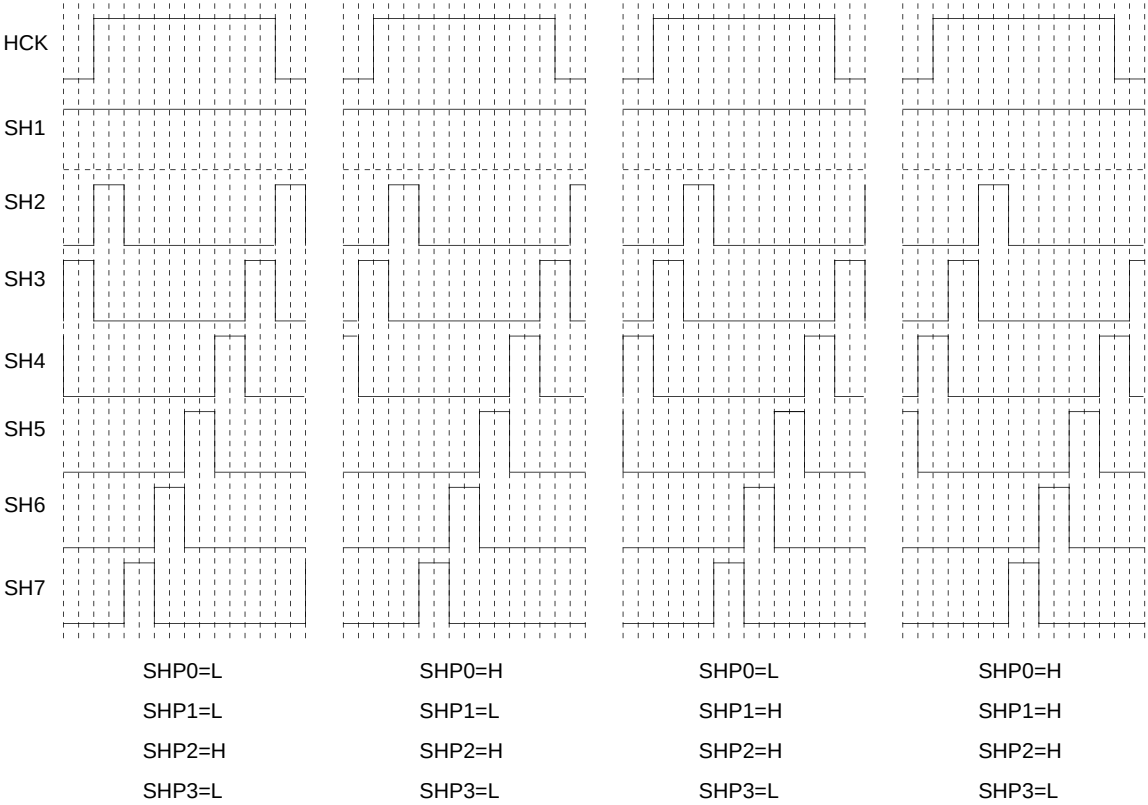
Right scanning pulse (RGT = H)





Left scanning pulse (RGT = L)



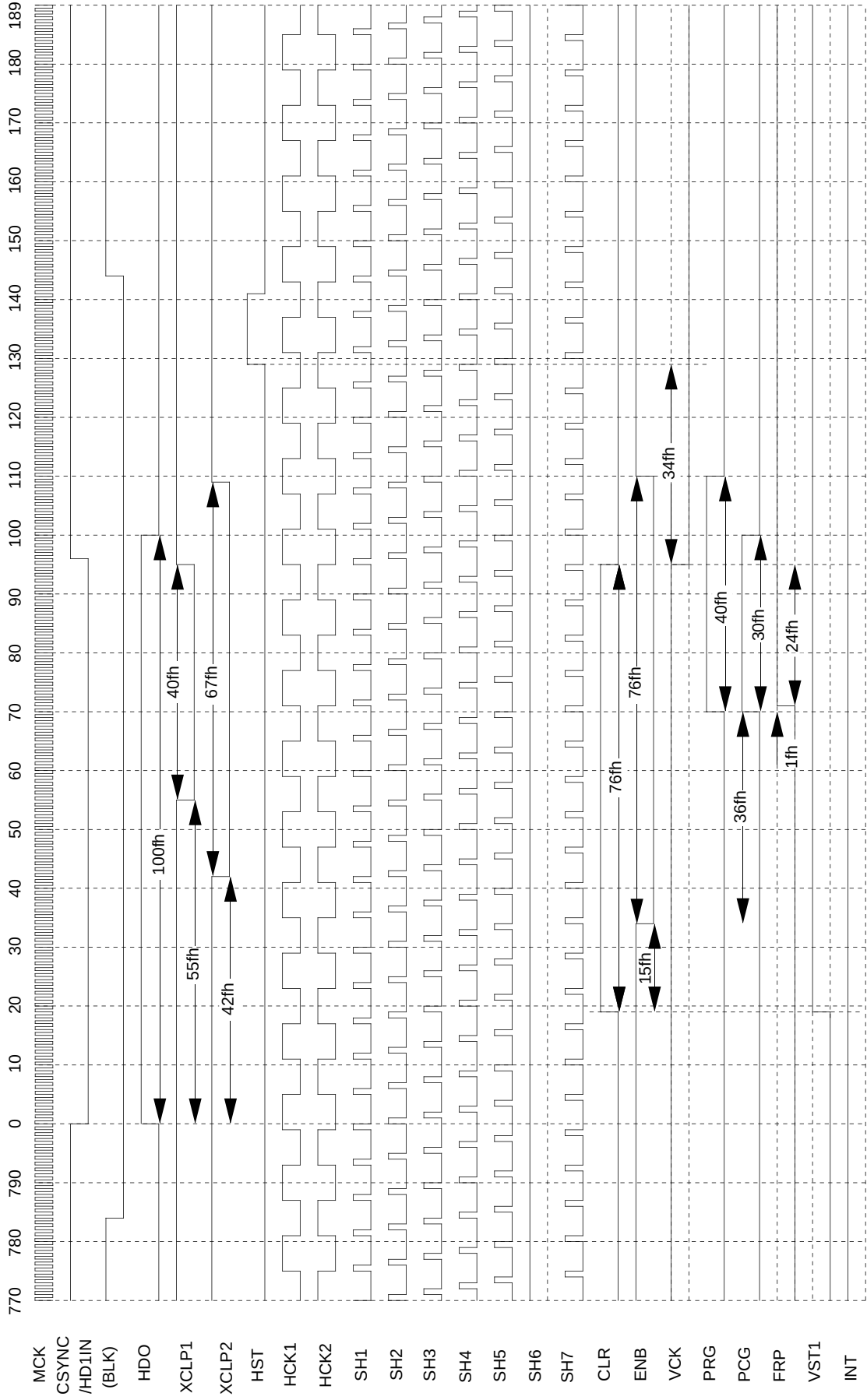




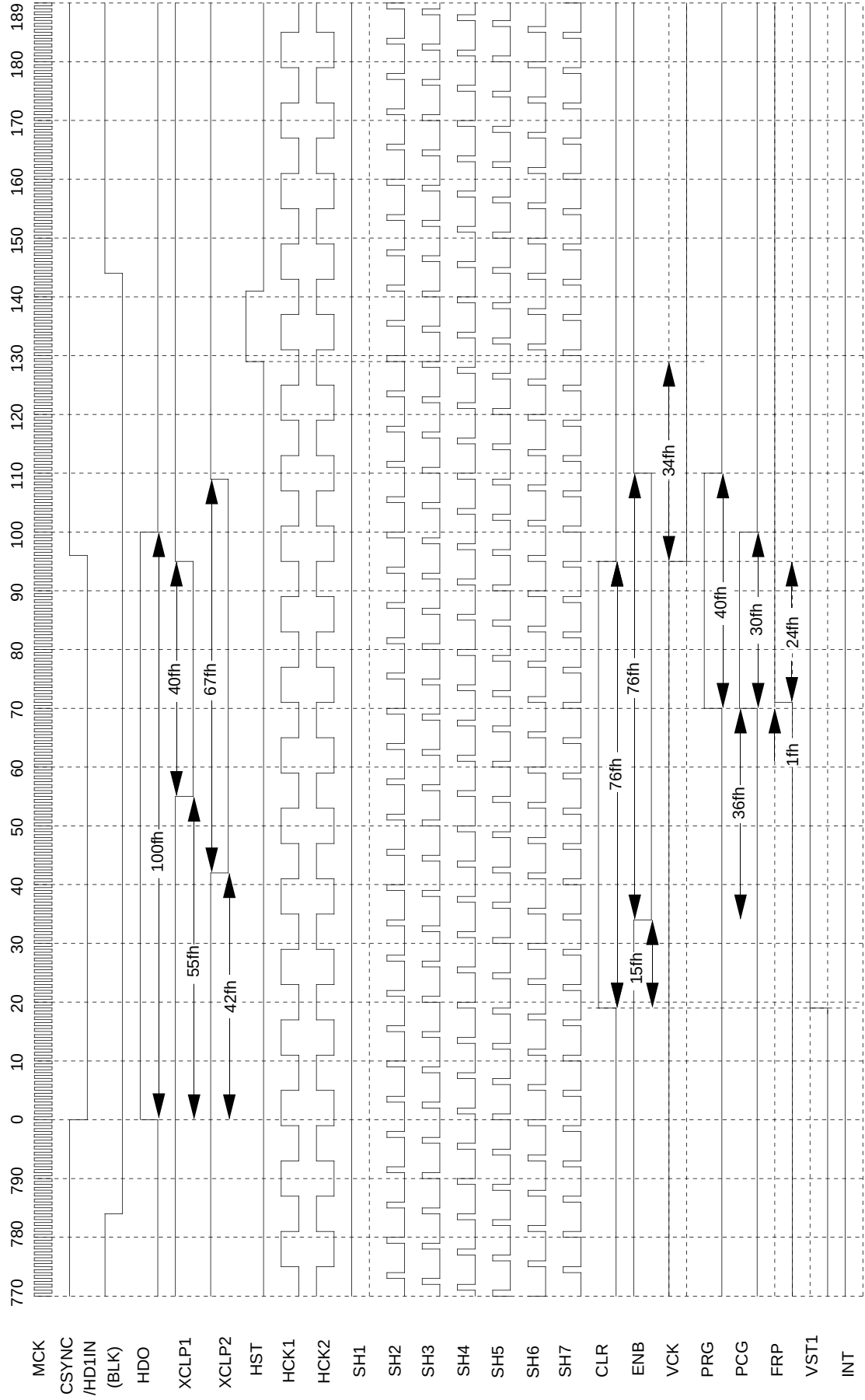
Horizontal Direction Timing Chart (IBM-VGA 640 x 480)

SLRG1: H (Normal scan)

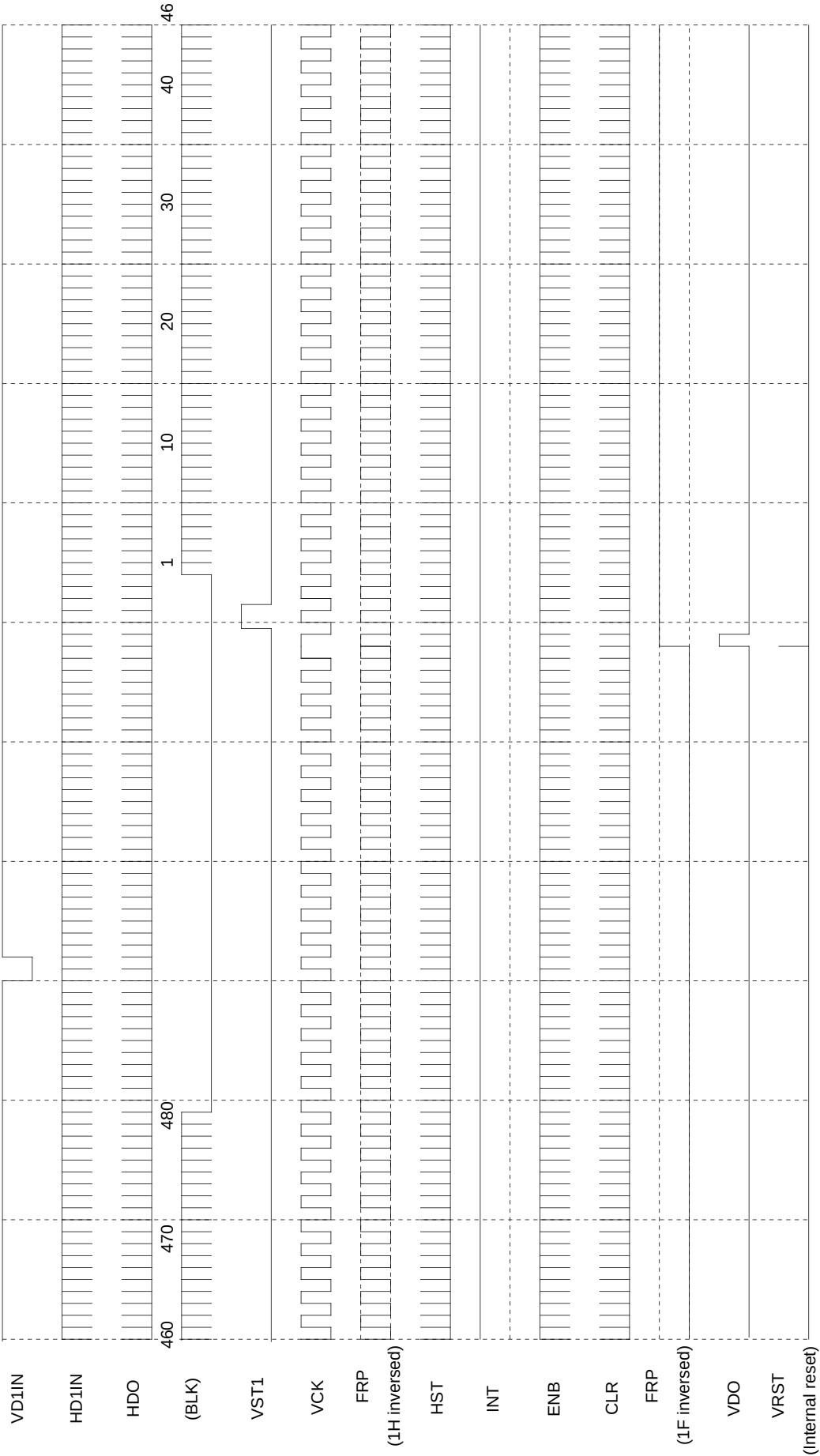
HP: 1100001 LSB CLPP: 10 LSB SHP: 0000 LSB



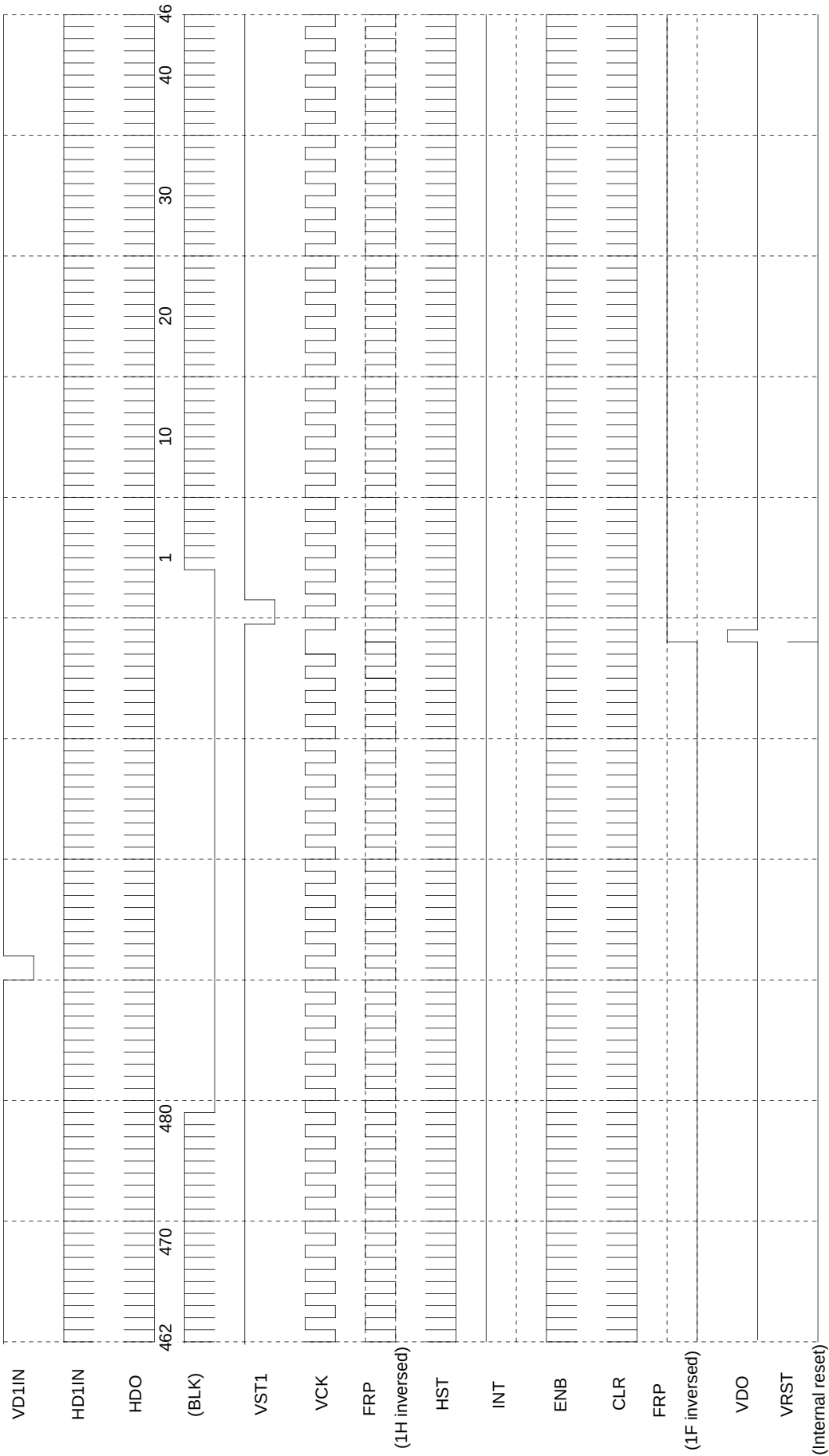
Horizontal Direction Timing Chart (IBM-VGA 640 x 480)  
SLRG T: L (Reverse scan)  
HP: 1100001 LSB CLPP: 10 LSB SHP: 0000 LSB



Vertical Direction Timing Chart (IBM-VGA 640 x 480)  
SLDWN: H (Down scan)  
VP: 1100100 LSB



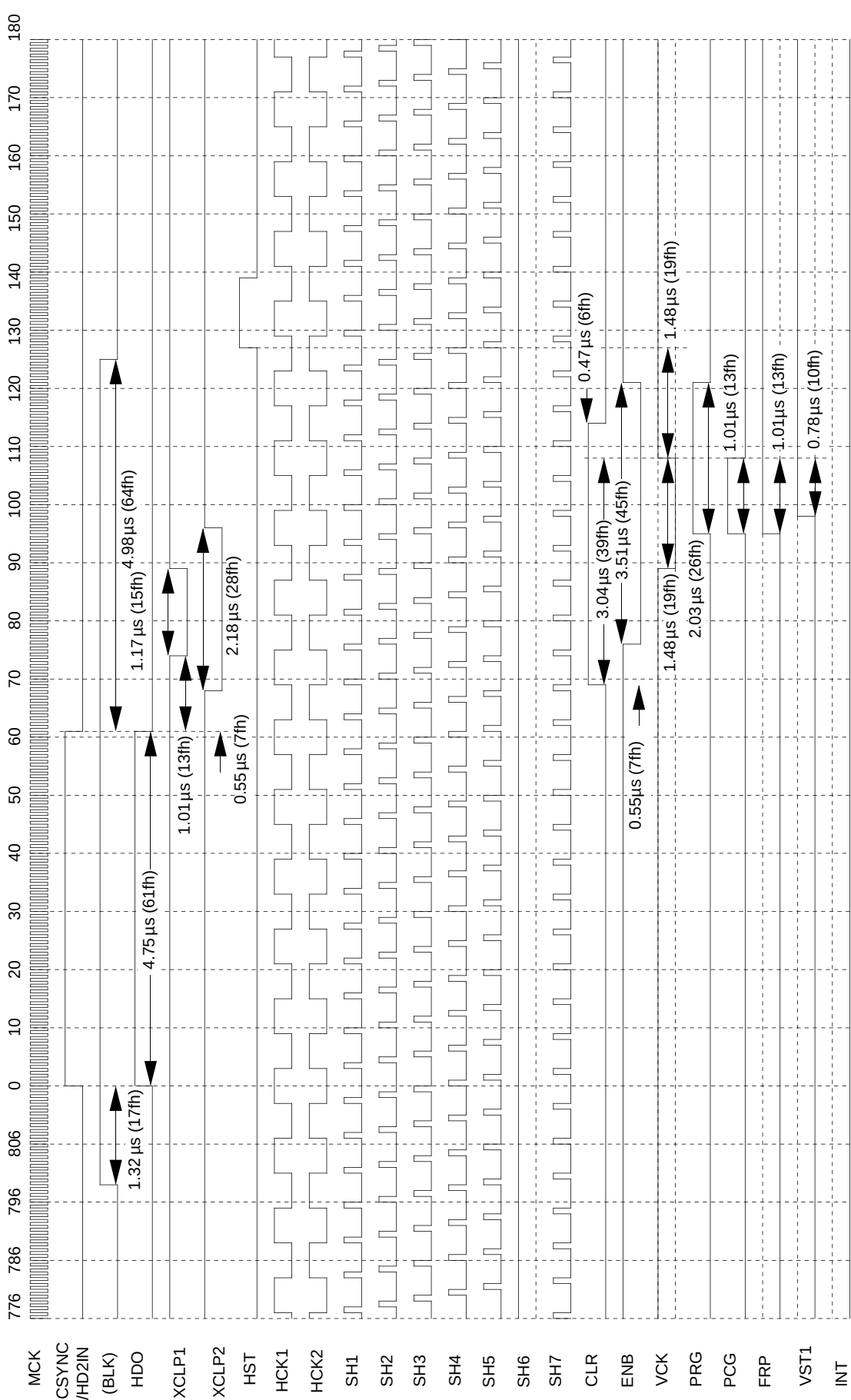
Vertical Direction Timing Chart (IBM-VGA 640 x 480)  
SLDWN: L (Up scan)  
VP: 1100100 LSB



Horizontal Direction Timing Chart (NTSC)

MCK: 12.84 MHz (77.89 ns)  
Loop Counter: 816 fh

RGT: H (Normal scan)  
HP: 1000000 LSB CLPP: 10 LSB SHP: 0000 LSB



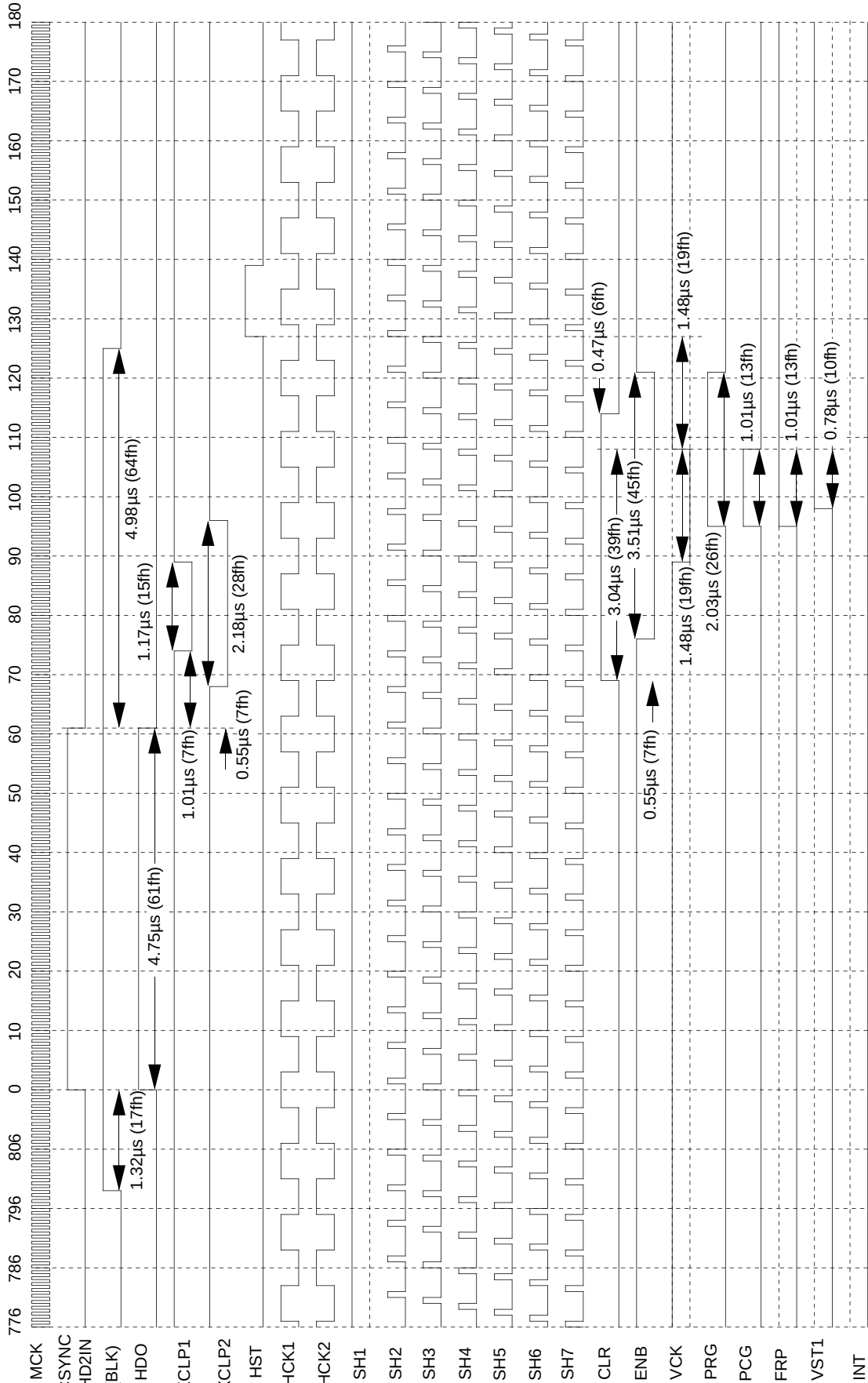
Horizontal Direction Timing Chart (NTSC)

RG T: L (Reverse scan)

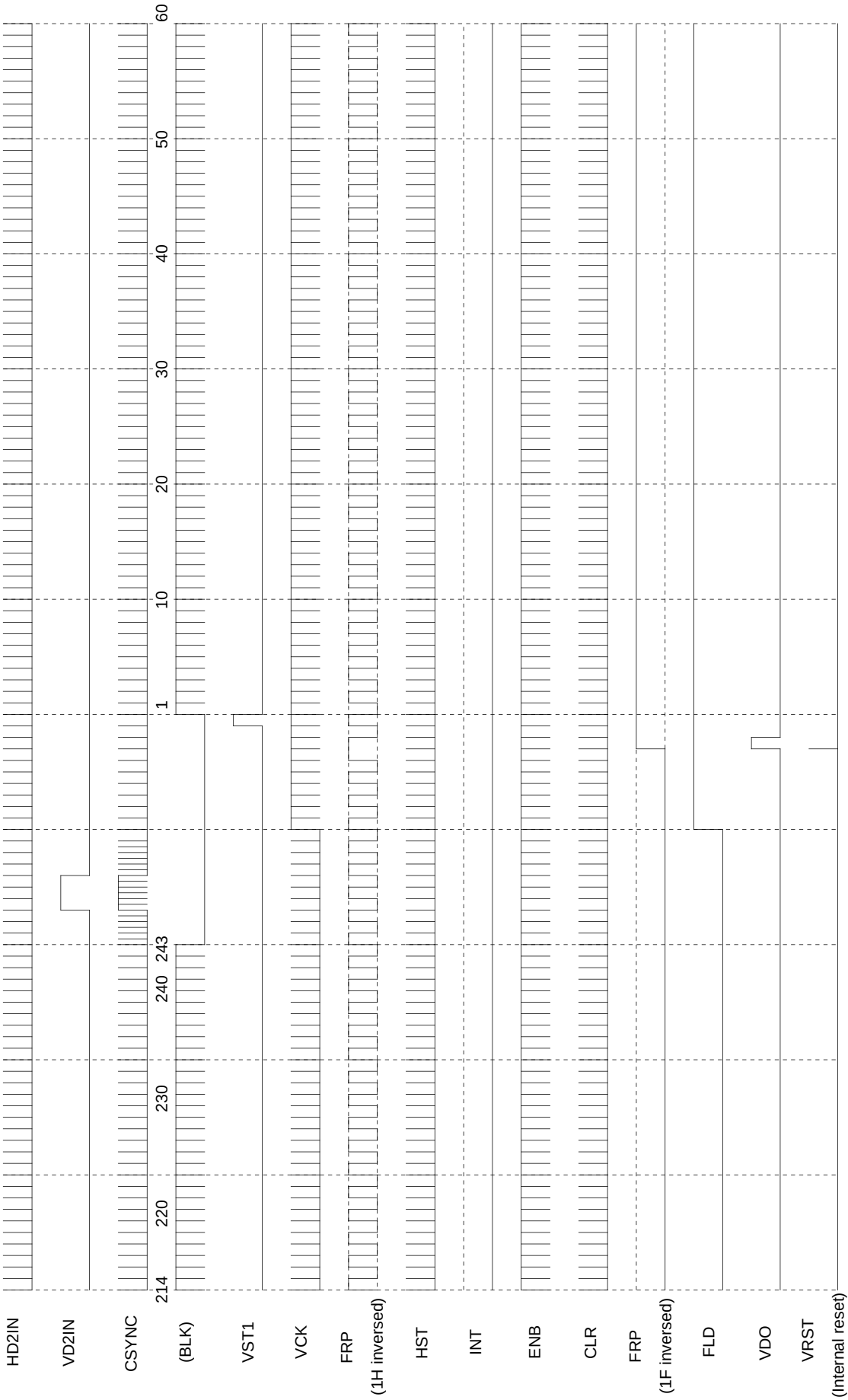
HP: 1000000 LSB CLPP: 10 LSB SHP: 0000 LSB

MCK: 12.84 MHz (77.89 ns)

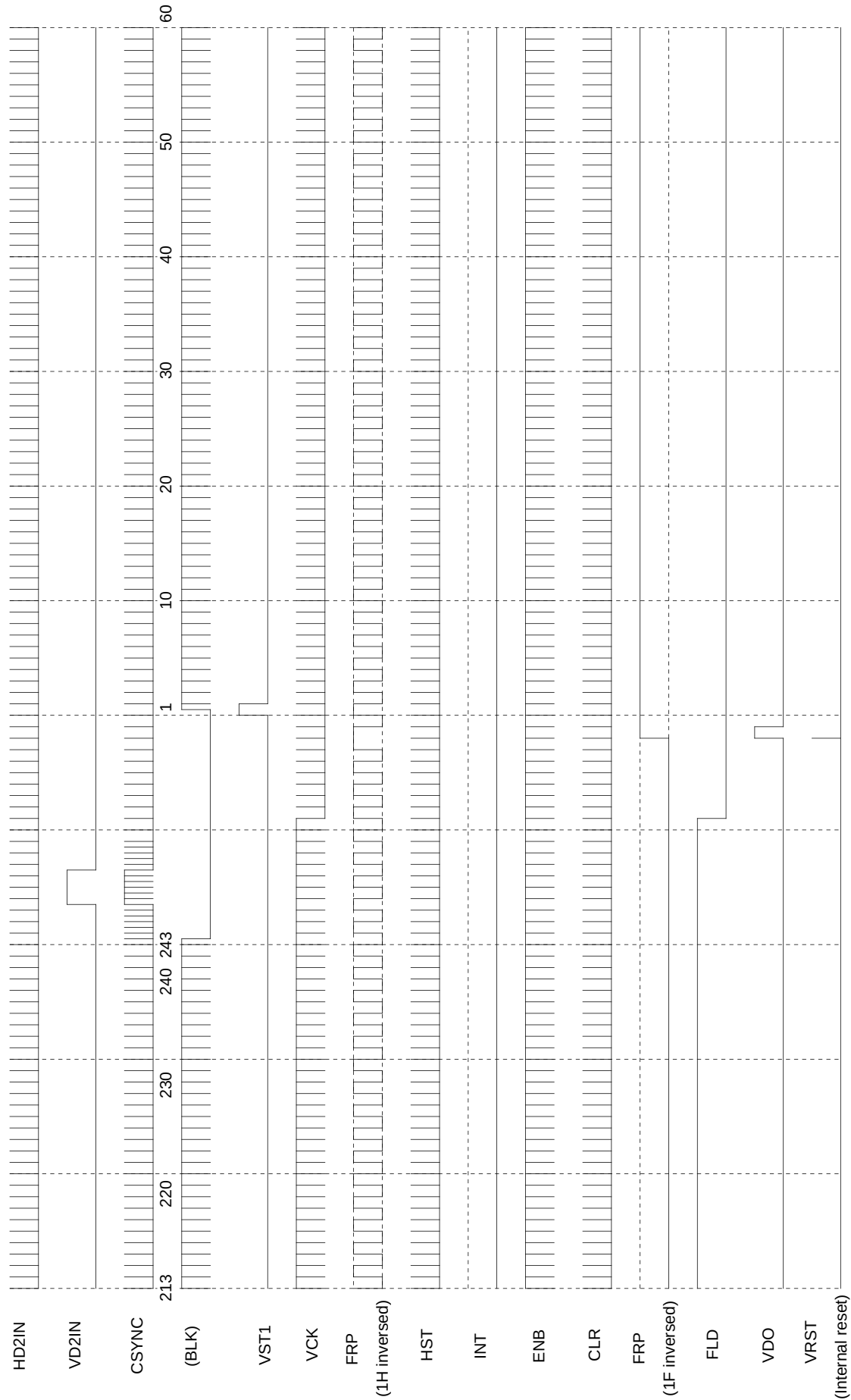
Loop Counter: 816 fh



Vertical Direction Timing Chart (NTSC, odd field)  
SLDWN: H (Down scan)  
VP: 1111010 LSB



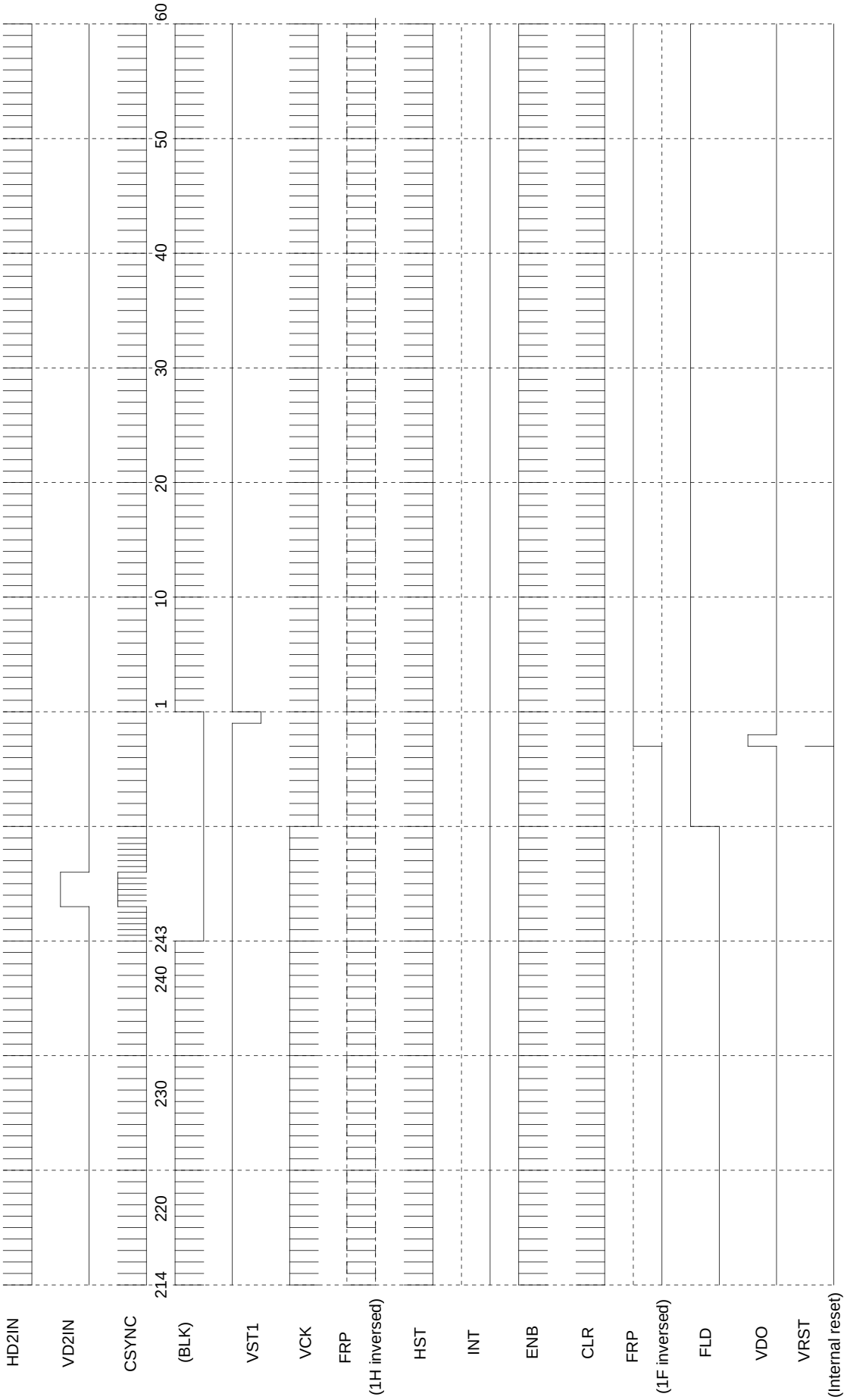
Vertical Direction Timing Chart (NTSC, even field)  
SLDWN: H (Down scan)  
VP: 1111010 LSB



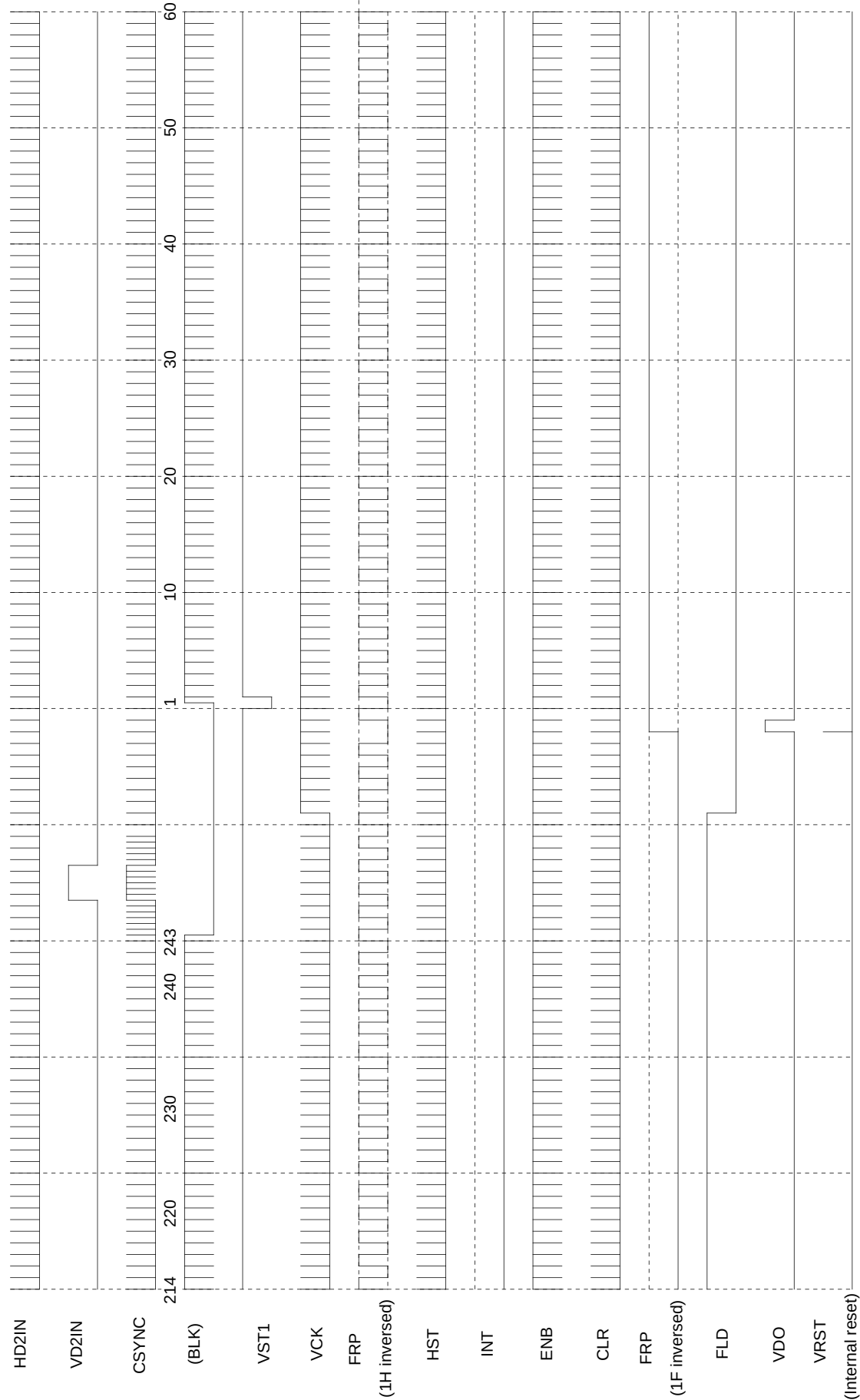


Vertical Direction Timing Chart (NTSC, odd field)

SLDWN: L (Up scan)  
VP: 1111010 LSB



Vertical Direction Timing Chart (NTSC, even field)  
SLDWN: L (Up scan)  
VP: 1111010 LSB

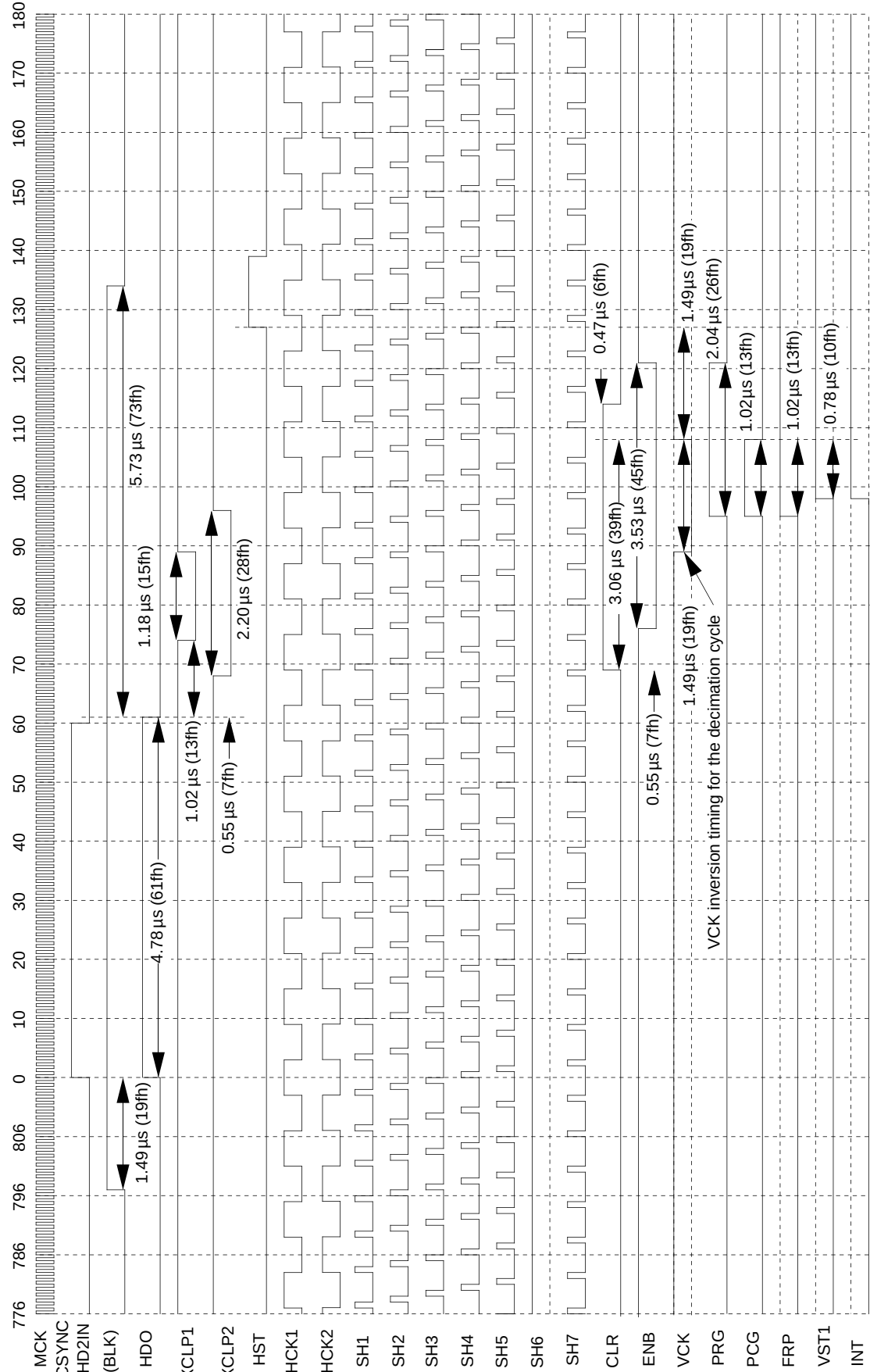


Horizontal Direction Timing Chart (PAL)

SLRGT: H (Normal scan)

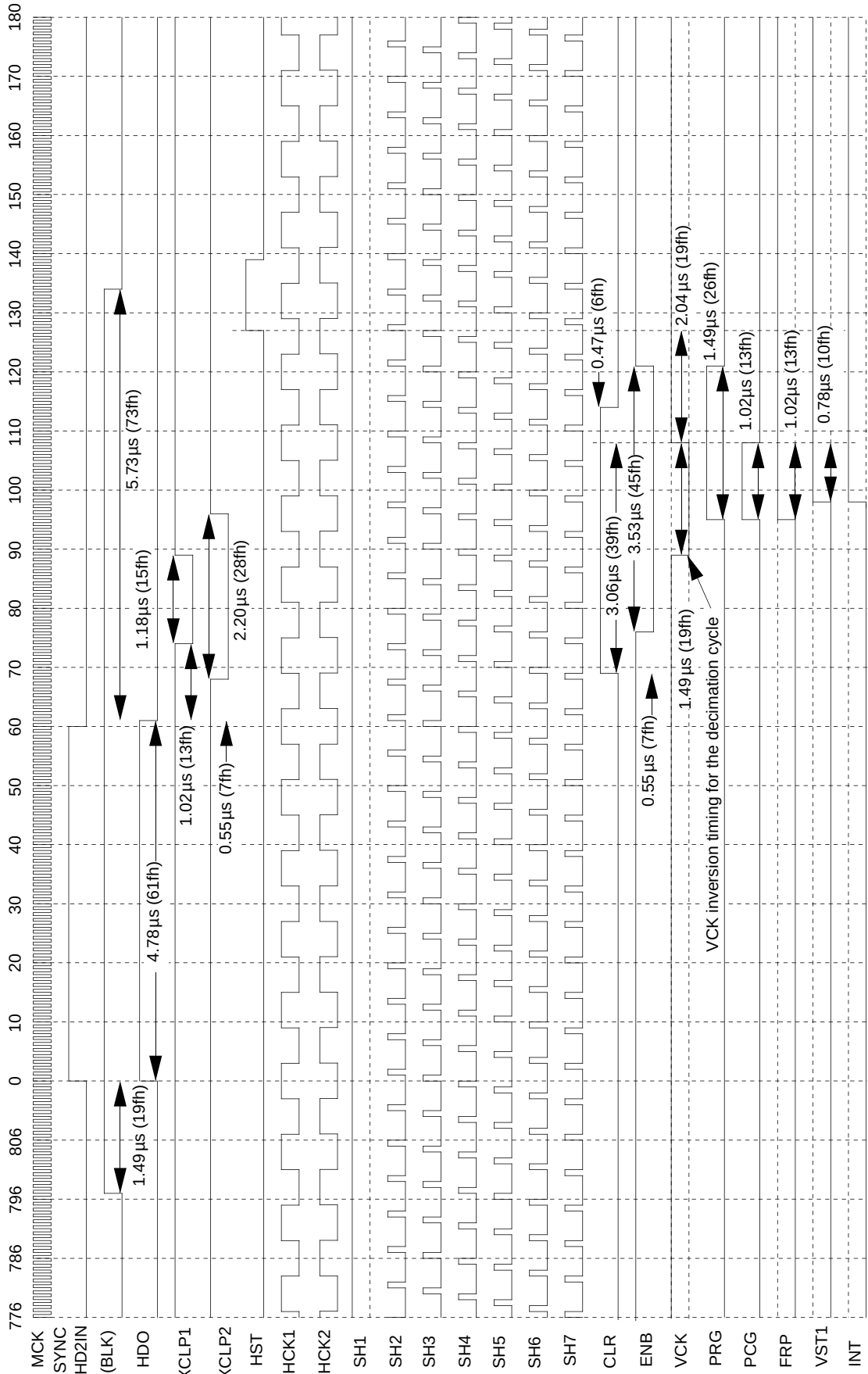
HP: 1000000 LSB CLPP: 10 LSB SHP: 0000 LSB

MCK: 12.75 MHz (78.43 ns)  
Loop Counter: 816 fh



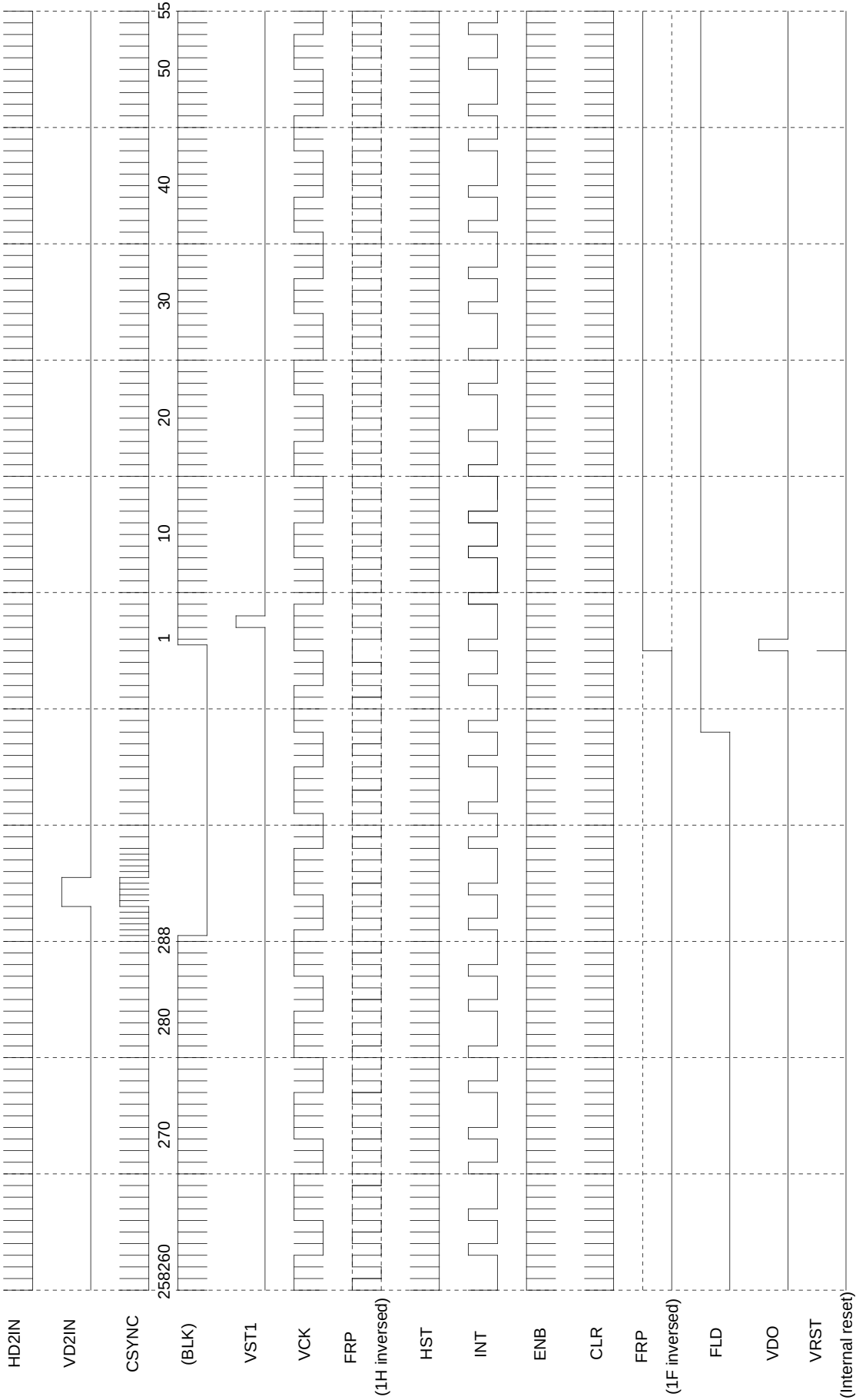
Horizontal Direction Timing Chart (PAL)

SLRG T: L (Reverse scan)      MCK: 12.75 MHz (78.43 ns)  
HP: 1000000 LSB   CLPP: 10 LSB   SHP: 0000 LSB      Loop Counter: 816fh



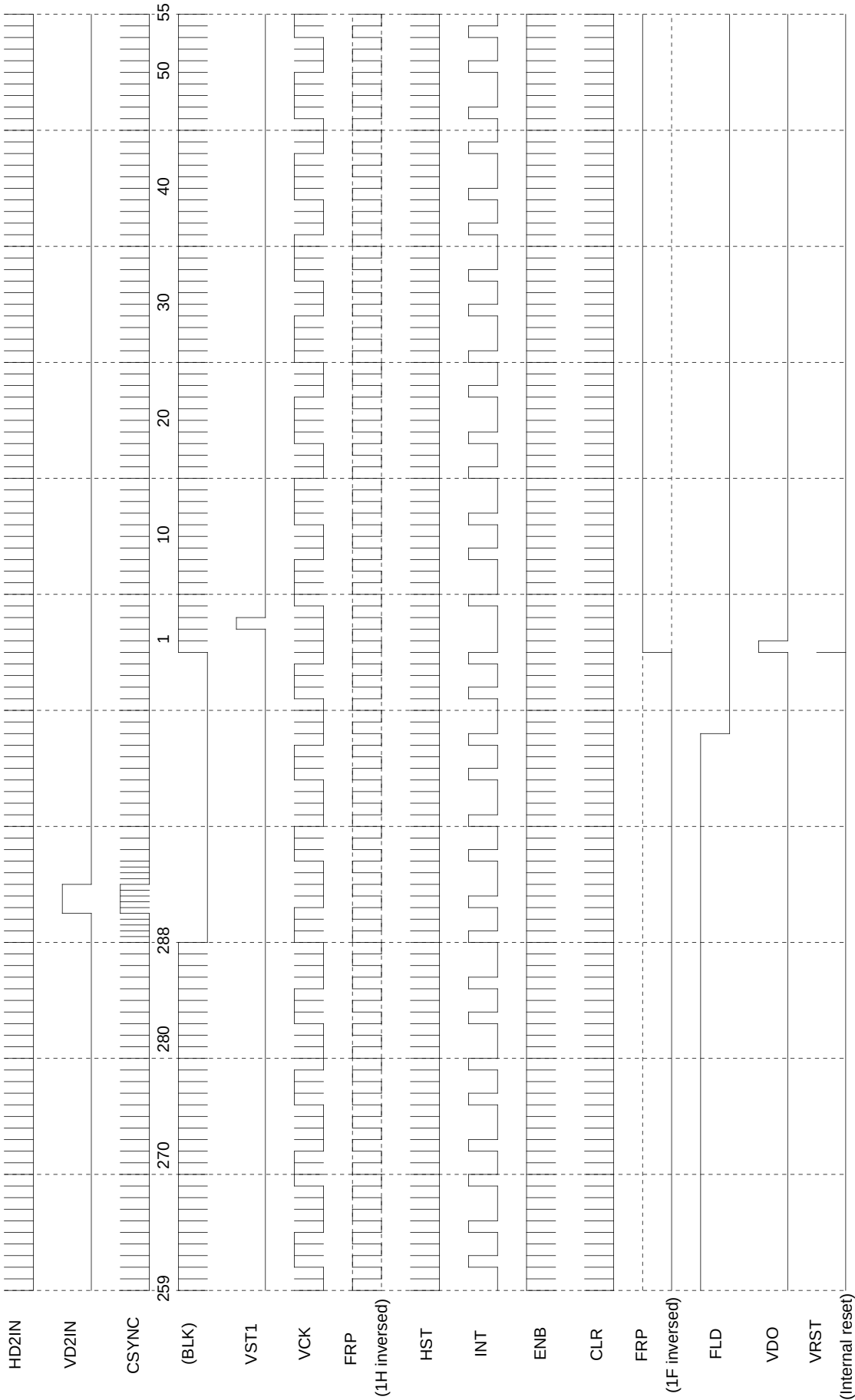
Vertical Direction Timing Chart (PAL, odd field)

SLDWN: H (Down scan)  
VP: 1110010 LSB



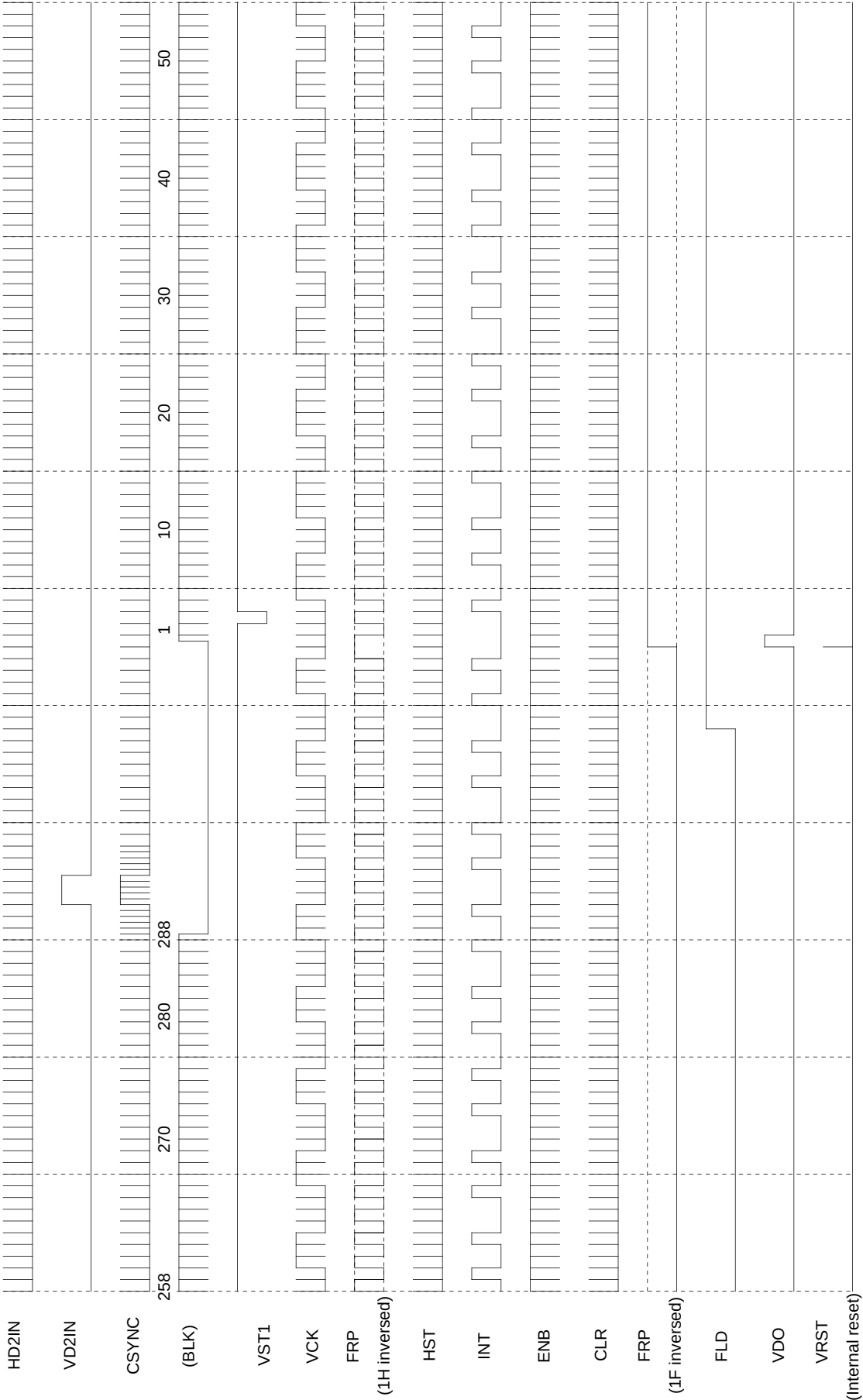
Vertical Direction Timing Chart (PAL, even field)

SLDWN: H (Down scan)  
VP: 1110010 LSB

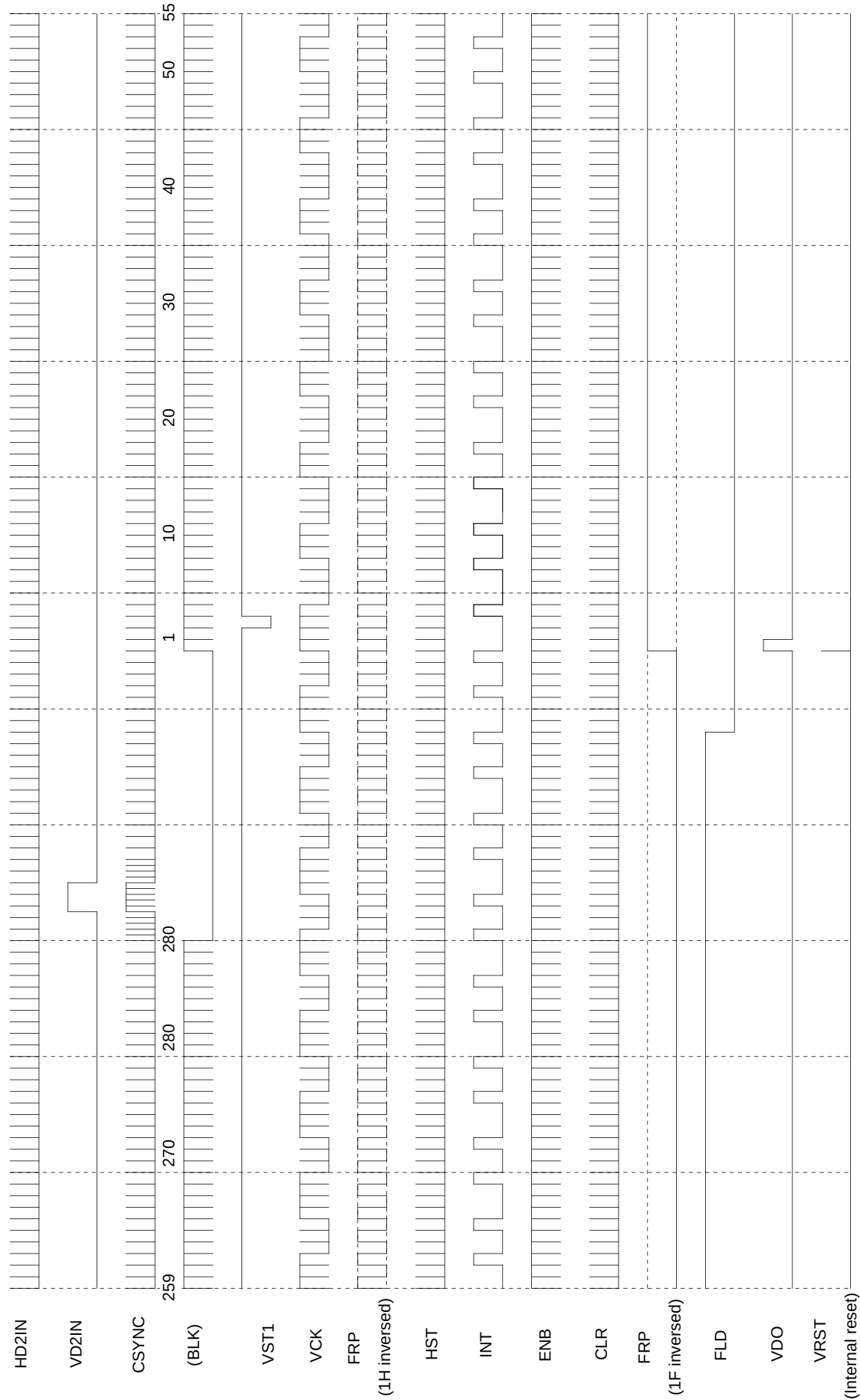


Vertical Direction Timing Chart (PAL, odd field)

SLDWN: L (Up scan)  
VP: 1110010 LSB



Vertical Direction Timing Chart (PAL, even field)  
SLDWN: L (Up scan)  
VP: 1110010 LSB



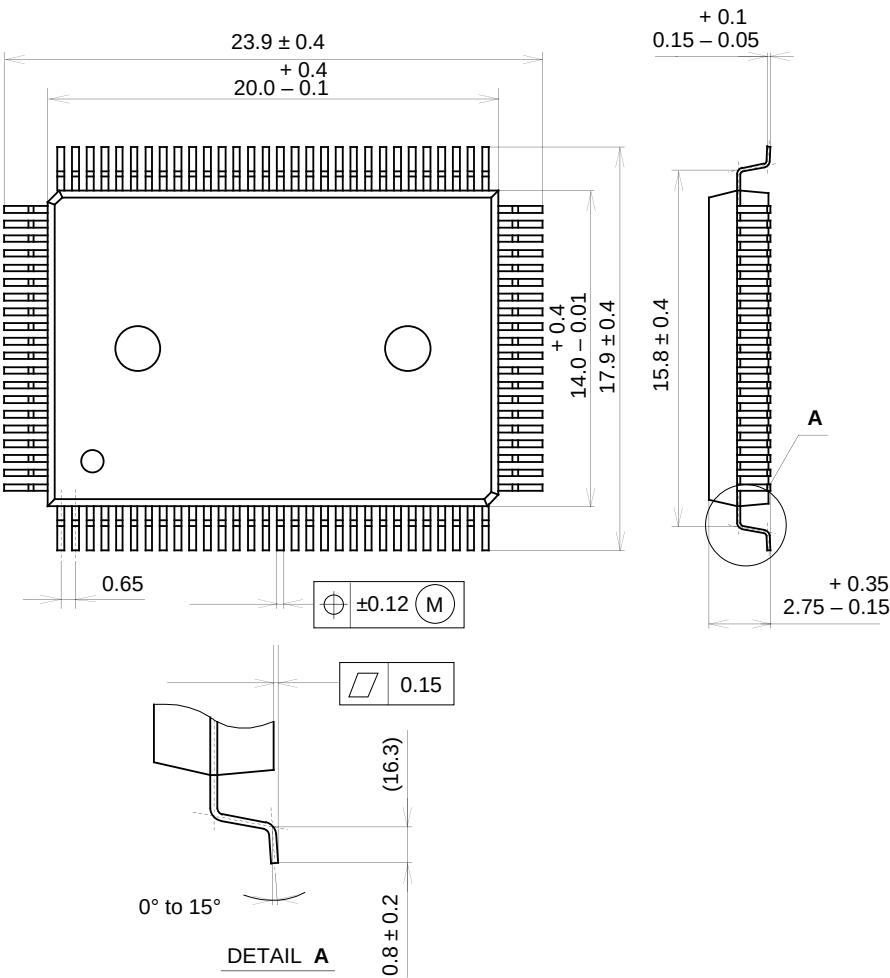


[illegible]

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Package Outline    Unit : mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

|            |                  |                  |                   |
|------------|------------------|------------------|-------------------|
| SONY CODE  | QFP-100P-L01     | PACKAGE MATERIAL | EPOXY RESIN       |
| EIAJ CODE  | *QFP100-P-1420-A | LEAD TREATMENT   | SOLDER PLATING    |
| JEDEC CODE | _____            | LEAD MATERIAL    | COPPER / 42 ALLOY |
|            |                  | PACKAGE WEIGHT   | 1.4g              |