National Semiconductor

# COP620C/COP622C/COP640C/COP642C/ COP820C/COP822C/COP840C/COP842C/ COP920C/COP922C/COP940C/COP942C Single-Chip microCMOS Microcontrollers

## General Description

The COP820C and COP840C are members of the COPS™ microcontroller family. They are fully static parts, fabricated using double-metal silicon gate microCMOS technology. This low cost microcontroller is a complete microcomputer containing all system timing, interrupt logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS™ serial I/O, a 16-bit timer/counter with capture register and a multi-sourced interrupt. Each I/O pin has software selectable options to adapt the device to the specific application. The part operates over a voltage range of 2.5 to 6.0V. High throughput is achieved with an efficient, regular instruction set operating at a 1 microsecond per instruction rate.

## Features

- Low Cost 8-bit microcontroller
- Fully static CMOS
- 1 μs instruction time (10 MHz clock)
- Low current drain (2.2 mA at 3 μs instruction rate)
  Low current static HALT mode (Typically < 1 μA)
- Single supply operation: 2.5 to 6.0V
- 1024 bytes ROM/64 Bytes RAM—COP820C family
- 2048 bytes ROM/128 Bytes RAM—COP840C family
- 16-bit read/write timer operates in a variety of modes
  — Timer with 16-bit auto reload register
  — 16-bit external event counter
  — Timer with 16-bit capture register (selectable edge)
- Multi-source interrupt
  — Reset master clear
  — External interrupt with selectable edge
  — Timer interrupt or capture interrupt
  — Software interrupt
- 8-bit stack pointer (stack in RAM)
- Powerful instruction set, most instructions single byte
- BCD arithmetic instructions
- MICROWIRE/PLUS serial I/O
- 28 pin package (optionally 20 pin package)
- 24 input/output pins (28-pin package)
- Software selectable I/O options (TRI-STATE®, push-pull, weak pull-up)
- Schmitt trigger inputs on Port G
- Temperature ranges: 0°C to +70°C, −40°C to +85°C, −55°C to +125°C
- Form Factor emulation devices
- Fully supported by MetaLink's development systems

## Block Diagram

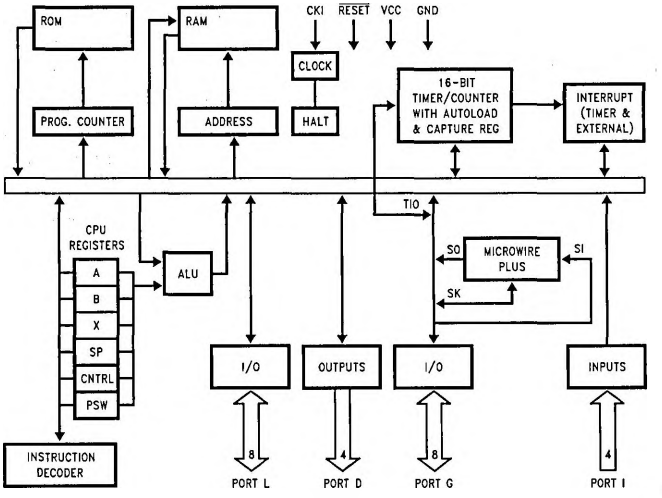



**FIGURE 1**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 7V |
| Voltage at any Pin | −0.3V to $V_{CC}$ + 0.3V |
| Total Current into $V_{CC}$ Pin (Source) | 50 mA |
| Total Current out of GND Pin (Sink) | 60 mA |
| Storage Temperature Range | −65°C to +140°C |

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

## DC Electrical Characteristics COP92XC, COP94XC; 0°C ≤ $T_A$ ≤ +70°C unless otherwise specified

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operating Voltage | | | | | |
| COP9XXC | | 2.3 | | 4.0 | V |
| COP9XXCH | | 4.0 | | 6.0 | V |
| Power Supply Ripple (Note 1) | Peak to Peak | | | 0.1 $V_{CC}$ | V |
| Supply Current (Note 2) | | | | | |
| CKI = 10 MHz | $V_{CC}$ = 6V, tc = 1 μs | | | 6.0 | mA |
| CKI = 4 MHz | $V_{CC}$ = 6V, tc = 2.5 μs | | | 4.0 | mA |
| CKI = 4 MHz | $V_{CC}$ = 4V, tc = 2.5 μs | | | 2.0 | mA |
| CKI = 1 MHz | $V_{CC}$ = 4V, tc = 10 μs | | | 1.2 | mA |
| HALT Current | $V_{CC}$ = 6V, CKI = 0 MHz | | <0.7 | 8.0 | μA |
| (Note 3) | $V_{CC}$ = 4V, CKI = 0 MHz | | <0.4 | 5.0 | μA |
| Input Levels | | | | | |
| RESET, CKI | | | | | |
| Logic High | | 0.9 $V_{CC}$ | | | V |
| Logic Low | | | | 0.1 $V_{CC}$ | V |
| All Other Inputs | | | | | |
| Logic High | | 0.7 $V_{CC}$ | | | V |
| Logic Low | | | | 0.2 $V_{CC}$ | V |
| Hi-Z Input Leakage | $V_{CC}$ = 6.0V | −1 | | +1 | μA |
| Input Pullup Current | $V_{CC}$ = 6.0V, $V_{IN}$ = 0V | −40 | | −250 | μA |
| G Port Input Hysteresis | | | | 0.35 $V_{CC}$ | V |
| Output Current Levels | | | | | |
| D Outputs | | | | | |
| Source | $V_{CC}$ = 4.5V, $V_{OH}$ = 3.8V | −0.4 | | | mA |
| | $V_{CC}$ = 2.3V, $V_{OH}$ = 1.6V | −0.2 | | | mA |
| Sink | $V_{CC}$ = 4.5V, $V_{OL}$ = 1.0V | 10 | | | mA |
| | $V_{CC}$ = 2.3V, $V_{OL}$ = 0.4V | 2 | | | mA |
| All Others | | | | | |
| Source (Weak Pull-Up) | $V_{CC}$ = 4.5V, $V_{OH}$ = 3.2V | −10 | | −110 | μA |
| | $V_{CC}$ = 2.3V, $V_{OH}$ = 1.6V | −2.5 | | −33 | μA |
| Source (Push-Pull Mode) | $V_{CC}$ = 4.5V, $V_{OH}$ = 3.8V | −0.4 | | | mA |
| | $V_{CC}$ = 2.3V, $V_{OH}$ = 1.6V | −0.2 | | | |
| Sink (Push-Pull Mode) | $V_{CC}$ = 4.5V, $V_{OL}$ = 0.4V | 1.6 | | | mA |
| | $V_{CC}$ = 2.3V, $V_{OL}$ = 0.4V | 0.7 | | | |
| TRI-STATE Leakage | $V_{CC}$ = 6.0V | −1.0 | | +1.0 | μA |
| Allowable Sink/Source Current Per Pin | | | | | |
| D Outputs (Sink) | | | | 15 | mA |
| All Others | | | | 3 | mA |
| Maximum Input Current (Note 4) Without Latchup (Room Temp) | Room Temp | | | ±100 | mA |
| RAM Retention Voltage, Vr | 500 ns Rise and Fall Time (Min) | 2.0 | | | V |
| Input Capacitance | | | | 7 | pF |
| Load Capacitance on D2 | | | | 1000 | pF |

## DC Electrical Characteristics (Continued)

**Note 1:** Rate of voltage change must be less than 0.5V/ms.

**Note 2:** Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

**Note 3:** The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to $V_{CC}$, L and G0—G5 configured as outputs and set high. The D port set to zero.

**Note 4:** Except pin G7: +100 mA, −25 mA (COP920C only). Sampled and not 100% tested. Pins G6 and $\overline{\text{RESET}}$ are designed with a high voltage input network for factory testing. These pins allow input voltages greater than $V_{CC}$ and the pins will have sink current to $V_{CC}$ when biased at voltages greater than $V_{CC}$ (the pins do not have source current when biased at a voltage below $V_{CC}$). The effective resistance to $V_{CC}$ is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

## AC Electrical Characteristics $0°C \le T_A \le +70°C$ unless otherwise specified

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Instruction Cycle Time (tc) | | | | | |
| Ext., Crystal/Resonator | $V_{CC} \ge 4.0V$ | 1 | | DC | μs |
| (Div-by 10) | $2.3V \le V_{CC} \le 4.0V$ | 2.5 | | DC | μs |
| R/C Oscillator Mode | $V_{CC} \ge 4.0V$ | 3 | | DC | μs |
| (Div-by 10) | $2.3V \le V_{CC} \le 4.0V$ | 7.5 | | DC | μs |
| CKI Clock Duty Cycle (Note 5) | fr = Max | 40 | | 60 | % |
| Rise Time (Note 5) | fr = 10 MHz Ext Clock | | | 12 | ns |
| Fall Time (Note 5) | fr = 10 MHz Ext Clock | | | 8 | ns |
| Inputs | | | | | |
| $t_{SETUP}$ | $V_{CC} \ge 4.0V$ | 200 | | | ns |
| | $2.3V \le V_{CC} \le 4.0V$ | 500 | | | ns |
| $t_{HOLD}$ | $V_{CC} \ge 4.0V$ | 60 | | | ns |
| | $2.3V \le V_{CC} \le 4.0V$ | 150 | | | ns |
| Output Propagation Delay | $C_L = 100$ pF, $R_L = 2.2$ kΩ | | | | |
| $t_{PD1}$, $t_{PD0}$ | | | | | |
| SO, SK | $V_{CC} \ge 4.0V$ | | | 0.7 | μs |
| | $2.5V \le V_{CC} \le 4.0V$ | | | 1.75 | μs |
| All Others | $V_{CC} \ge 4.0V$ | | | 1 | μs |
| | $2.5V \le V_{CC} \le 4.0V$ | | | 2.5 | μs |
| MICROWIRE™ Setup Time ($t_{UWS}$) | | 20 | | | ns |
| MICROWIRE Hold Time ($t_{UWH}$) | | 56 | | | ns |
| MICROWIRE Output Propagation Delay ($t_{UPD}$) | | | | 220 | ns |
| Input Pulse Width | | | | | |
| Interrupt Input High Time | | $t_C$ | | | |
| Interrupt Input Low Time | | $t_C$ | | | |
| Timer Input High Time | | $t_C$ | | | |
| Timer Input Low Time | | $t_C$ | | | |
| Reset Pulse Width | | 1.0 | | | μs |

**Note 5:** Parameter sampled (not 100% tested).

# COP820C/COP822C/COP840C/COP842C

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 7V |
| Voltage at any Pin | −0.3V to $V_{CC}$ + 0.3V |
| Total Current into $V_{CC}$ Pin (Source) | 50 mA |
| Total Current out of GND Pin (Sink) | 60 mA |
| Storage Temperature Range | −65°C to +140°C |

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

## DC Electrical Characteristics

COP82XC, COP84XC: $-40°C \le T_A \le +85°C$ unless otherwise specified

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operating Voltage | | 2.5 | | 6.0 | V |
| Power Supply Ripple (Note 1) | Peak to Peak | | | 0.1 $V_{CC}$ | V |
| Supply Current (Note 2) | | | | | |
| CKI = 10 MHz | $V_{CC}$ = 6V, tc = 1 μs | | | 6.0 | mA |
| CKI = 4 MHz | $V_{CC}$ = 6V, tc = 2.5 μs | | | 4.0 | mA |
| CKI = 4 MHz | $V_{CC}$ = 4.0V, tc = 2.5 μs | | | 2.0 | mA |
| CKI = 1 MHz | $V_{CC}$ = 4.0V, tc = 10 μs | | | 1.2 | mA |
| HALT Current (Note 3) | $V_{CC}$ = 6V, CKI = 0 MHz | | <1 | 10 | μA |
| Input Levels | | | | | |
| RESET, CKI | | | | | |
| Logic High | | 0.9 $V_{CC}$ | | | V |
| Logic Low | | | | 0.1 $V_{CC}$ | V |
| All Other Inputs | | | | | |
| Logic High | | 0.7 $V_{CC}$ | | | V |
| Logic Low | | | | 0.2 $V_{CC}$ | V |
| Hi-Z Input Leakage | $V_{CC}$ = 6.0V | −2 | | +2 | μA |
| Input Pullup Current | $V_{CC}$ = 6.0V, $V_{IN}$ = 0V | −40 | | −250 | μA |
| G Port Input Hysteresis | | | | 0.35 $V_{CC}$ | V |
| Output Current Levels | | | | | |
| D Outputs | | | | | |
| Source | $V_{CC}$ = 4.5V, $V_{OH}$ = 3.8V | −0.4 | | | mA |
| | $V_{CC}$ = 2.5V, $V_{OH}$ = 1.8V | −0.2 | | | mA |
| Sink | $V_{CC}$ = 4.5V, $V_{OL}$ = 1.0V | 10 | | | mA |
| | $V_{CC}$ = 2.5V, $V_{OL}$ = 0.4V | 2 | | | mA |
| All Others | | | | | |
| Source (Weak Pull-Up) | $V_{CC}$ = 4.5V, $V_{OH}$ = 3.2V | −10 | | −110 | μA |
| | $V_{CC}$ = 2.5V, $V_{OH}$ = 1.8V | −2.5 | | −33 | μA |
| Source (Push-Pull Mode) | $V_{CC}$ = 4.5V, $V_{OH}$ = 3.8V | −0.4 | | | mA |
| | $V_{CC}$ = 2.5V, $V_{OH}$ = 1.8V | −0.2 | | | |
| Sink (Push-Pull Mode) | $V_{CC}$ = 4.5V, $V_{OL}$ = 0.4V | 1.6 | | | mA |
| | $V_{CC}$ = 2.5V, $V_{OL}$ = 0.4V | 0.7 | | | |
| TRI-STATE Leakage | | −2.0 | | +2.0 | μA |
| Allowable Sink/Source Current Per Pin | | | | | |
| D Outputs (Sink) | | | | 15 | mA |
| All Others | | | | 3 | mA |
| Maximum Input Current (Note 4) Without Latchup (Room Temp) | Room Temp | | | ±100 | mA |
| RAM Retention Voltage, Vr | 500 ns Rise and Fall Time (Min) | 2.0 | | | V |
| Input Capacitance | | | | 7 | pF |
| Load Capacitance on D2 | | | | 1000 | pF |

**Note 1:** Rate of voltage change must be less than 0.5V/ms.

**Note 2:** Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

**Note 3:** The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to $V_{CC}$, L and G0—G5 configured as outputs and set high. The D port set to zero.

**Note 4:** Except pin G7: +100 mA, −25 mA (COP820C only). Sampled and not 100% tested. Pins G6 and RESET are designed with a high voltage input network for factory testing. These pins allow input voltages greater than $V_{CC}$ and the pins will have sink current to $V_{CC}$ when biased at voltages greater than $V_{CC}$ (the pins do not have source current when biased at a voltage below $V_{CC}$). The effective resistance to $V_{CC}$ is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

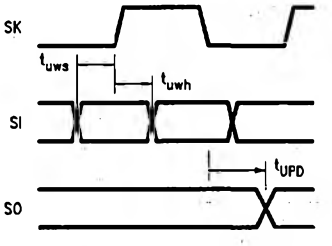
# COP820C/COP822C/COP840C/COP842C

## AC Electrical Characteristics $-40°C \le T_A \le +85°C$ unless otherwise specified

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Instruction Cycle Time (tc) | | | | | |
| Ext. or Crystal/Resonator | $V_{CC} \ge 4.5V$ | 1 | | DC | μs |
| (Div-by 10) | $2.5V \le V_{CC} < 4.5V$ | 2.5 | | DC | μs |
| R/C Oscillator Mode | $V_{CC} \ge 4.5V$ | 3 | | DC | μs |
| (Div-by 10) | $2.5V \le V_{CC} < 4.5V$ | 7.5 | | DC | μs |
| CKI Clock Duty Cycle (Note 5) | fr = Max | 40 | | 60 | % |
| Rise Time (Note 5) | fr = 10 MHz Ext Clock | | | 12 | ns |
| Fall Time (Note 5) | fr = 10 MHz Ext Clock | | | 8 | ns |
| Inputs | | | | | |
| $t_{SETUP}$ | $V_{CC} \ge 4.5V$ | 200 | | | ns |
| | $2.5V \le V_{CC} < 4.5V$ | 500 | | | ns |
| $t_{HOLD}$ | $V_{CC} \ge 4.5V$ | 60 | | | ns |
| | $2.5V \le V_{CC} < 4.5V$ | 150 | | | ns |
| Output Propagation Delay | $C_L$ = 100 pF, $R_L$ = 2.2 kΩ | | | | |
| $t_{PD1}$, $t_{PD0}$ | | | | | |
| SO, SK | $V_{CC} \ge 4.5V$ | | | 0.7 | μs |
| | $2.5V \le V_{CC} < 4.5V$ | | | 1.75 | μs |
| All Others | $V_{CC} \ge 4.5V$ | | | 1 | μs |
| | $2.5V \le V_{CC} < 4.5V$ | | | 2.5 | μs |
| MICROWIRE Setup Time ($t_{UWS}$) | | 20 | | | ns |
| MICROWIRE Hold Time ($t_{UWH}$) | | 56 | | | ns |
| MICROWIRE Output Propagation Delay ($t_{UPD}$) | | | | 220 | ns |
| Input Pulse Width | | | | | |
| Interrupt Input High Time | | $t_C$ | | | |
| Interrupt Input Low Time | | $t_C$ | | | |
| Timer Input High Time | | $t_C$ | | | |
| Timer Input Low Time | | $t_C$ | | | |
| Reset Pulse Width | | 1.0 | | | μs |

**Note 5:** Parameter sampled (not 100% tested).

## Timing Diagram




TL/DD/9103-19

**FIGURE 2. MICROWIRE/PLUS Timing**

# COP620C/COP622C/COP640C/COP642C

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 6V |
| Voltage at any Pin | −0.3V to $V_{CC}$ + 0.3V |
| Total Current into $V_{CC}$ Pin (Source) | 40 mA |
| Total Current out of GND Pin (Sink) | 48 mA |
| Storage Temperature Range | −65°C to +140°C |

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

## DC Electrical Characteristics COP62XC, COP64XC: −55°C ≤ $T_A$ ≤ +125°C unless otherwise specified

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operating Voltage | | 4.5 | | 5.5 | V |
| Power Supply Ripple (Note 1) | Peak to Peak | | | 0.1 $V_{CC}$ | V |
| Supply Current (Note 2) | | | | | |
| CKI = 10 MHz | $V_{CC}$ = 5.5V, tc = 1 μs | | | 6.0 | mA |
| CKI = 4 MHz | $V_{CC}$ = 5.5V, tc = 2.5 μs | | | 4 | mA |
| HALT Current (Note 3) | $V_{CC}$ = 5.5V, CKI = 0 MHz | | <10 | 30 | μA |
| Input Levels | | | | | |
| RESET, CKI | | | | | |
| Logic High | | 0.9 $V_{CC}$ | | | V |
| Logic Low | | | | 0.1 $V_{CC}$ | V |
| All Other Inputs | | | | | |
| Logic High | | 0.7 $V_{CC}$ | | | V |
| Logic Low | | | | 0.2 $V_{CC}$ | V |
| Hi-Z Input Leakage | $V_{CC}$ = 5.5V | −5 | | +5 | μA |
| Input Pullup Current | $V_{CC}$ = 4.5V, $V_{IN}$ = 0V | −35 | | −300 | μA |
| G Port Input Hysteresis | | | | 0.35 $V_{CC}$ | V |
| Output Current Levels | | | | | |
| D Outputs | | | | | |
| Source | $V_{CC}$ = 4.5V, $V_{OH}$ = 3.8V | −0.35 | | | mA |
| Sink | $V_{CC}$ = 4.5V, $V_{OL}$ = 1.0V | 9 | | | mA |
| All Others | | | | | |
| Source (Weak Pull-Up) | $V_{CC}$ = 4.5V, $V_{OH}$ = 3.2V | −9 | | −120 | μA |
| Source (Push-Pull Mode) | $V_{CC}$ = 4.5V, $V_{OH}$ = 3.8V | −0.35 | | | mA |
| Sink (Push-Pull Mode) | $V_{CC}$ = 4.5V, $V_{OL}$ = 0.4V | 1.4 | | | mA |
| TRI-STATE Leakage | | −5.0 | | +5.0 | μA |
| Allowable Sink/Source Current Per Pin | | | | | |
| D Outputs (Sink) | | | | 12 | mA |
| All Others | | | | 2.5 | mA |
| Maximum Input Current (Room Temp) Without Latchup (Note 5) | Room Temp | | | ±100 | mA |
| RAM Retention Voltage, Vr | 500 ns Rise and Fall Time (Min) | 2.5 | | | V |
| Input Capacitance | | | | 7 | pF |
| Load Capacitance on D2 | | | | 1000 | pF |

**Note 1:** Rate of voltage change must be less than 0.5V/ms.

**Note 2:** Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

**Note 3:** The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to $V_{CC}$, L and G0—G5 configured as outputs and set high. The D port set to zero.

**Note 4:** Except pin G7: +100 mA, −25 mA (COP620C only). Sampled and not 100% tested. Pins G6 and RESET are designed with a high voltage input network for factory testing. These pins allow input voltages greater than $V_{CC}$ and the pins will have sink current to $V_{CC}$ when biased at voltages greater than $V_{CC}$ (the pins do not have source current when biased at a voltage below $V_{CC}$). The effective resistance to $V_{CC}$ is 750Ω (typical). These two pins will not latch up. The voltage at the pins must be limited to less than 14V.

# COP620C/COP622C/COP640C/COP642C

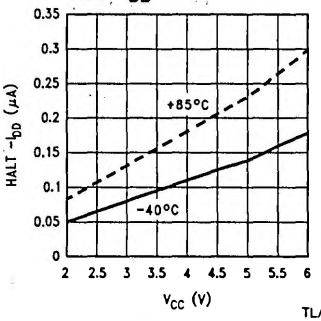
## AC Electrical Characteristics $-55°C \le T_A \le +125°C$ unless otherwise specified

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Instruction Cycle Time (tc) | | | | | |
| Ext. or Crystal/Resonant (Div-by 10) | $V_{CC} \ge 4.5V$ | 1 | | DC | μs |
| CKI Clock Duty Cycle (Note 5) | fr = Max | 40 | | 60 | % |
| Rise Time (Note 5) | fr = 10 MHz Ext Clock | | | 12 | ns |
| Fall Time (Note 5) | fr = 10 MHz Ext Clock | | | 8 | ns |
| Inputs | | | | | |
| $t_{SETUP}$ | $V_{CC} \ge 4.5V$ | 220 | | | ns |
| $t_{HOLD}$ | $V_{CC} \ge 4.5V$ | 66 | | | ns |
| Output Propagation Delay $t_{PD1}$, $t_{PD0}$ | $R_L$ = 2.2k, $C_L$ = 100 pF | | | | |
| SO, SK | $V_{CC} \ge 4.5V$ | | | 0.8 | μs |
| All Others | $V_{CC} \ge 4.5V$ | | | 1.1 | μs |
| MICROWIRE Setup Time ($t_{UWS}$) | | 20 | | | ns |
| MICROWIRE Hold Time ($t_{UWH}$) | | 56 | | | ns |
| MICROWIRE Output Valid Time ($t_{UPD}$) | | | | 220 | ns |
| Input Pulse Width | | | | | |
| Interrupt Input High Time | | $t_C$ | | | |
| Interrupt Input Low Time | | $t_C$ | | | |
| Timer Input High Time | | $t_C$ | | | |
| Timer Input Low Time | | $t_C$ | | | |
| Reset Pulse Width | | 1 | | | μs |

**Note 5:** Parameter sampled (not 100% tested).

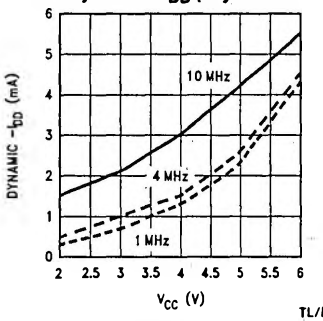
## Typical Performance Characteristics ($-40°C \le T_A \le +85°C$)

**Halt—$I_{DD}$**



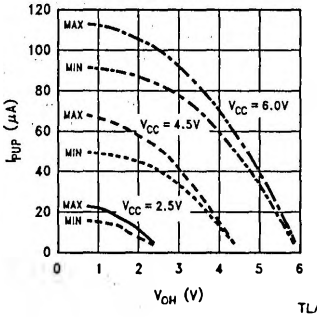

TL/DD/9103-20

**Dynamic—$I_{DD}$ (Crystal Clock Option)**



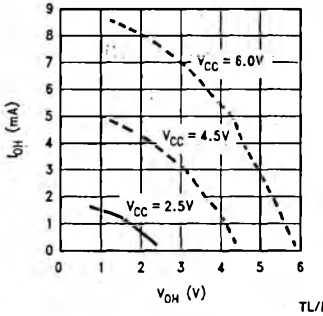

TL/DD/9103-21

**Port L/G Weak Pull-Up Source Current**



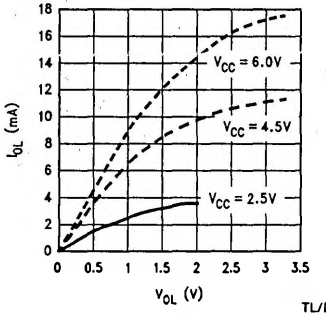

TL/DD/9103-22

**Port L/G Push-Pull Source Current**



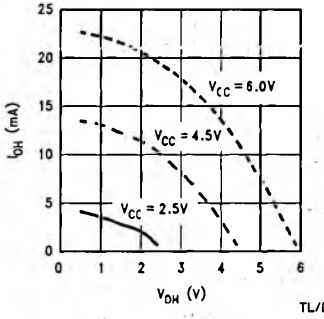

TL/DD/9103-23

**Port L/G Push-Pull Sink Current**



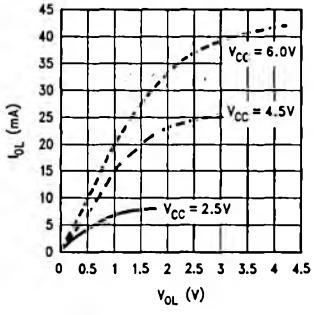

TL/DD/9103-24

**Port D Source Current**




TL/DD/9103-25

**Port D Sink Current**

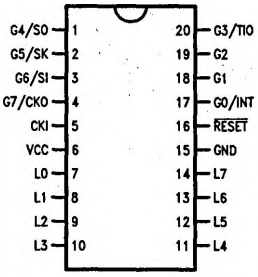



TL/DD/9103-26

## Connection Diagrams

**DUAL-IN-LINE PACKAGE**

**20 DIP**

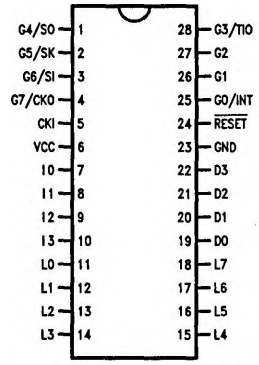



TL/DD/9103-3

Top View

**Order Number COP622C-XXX/N, COP642C-XXX/N, COP822C-XXX/N, COP842C-XXX/N, COP922C-XXX/N or COP942C-XXX/N**
**See NS Package Number N20A**

**28 DIP**

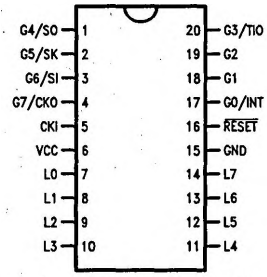



TL/DD/9103-5

**Order Number COP620C-XXX/N, COP640C-XXX/N, COP820C-XXX/N, COP840C-XXX/D, COP920C-XXX/N or COP940C-XXX/N**
**See NS Package Number N28B**

**SURFACE MOUNT**

**20 SO Wide**

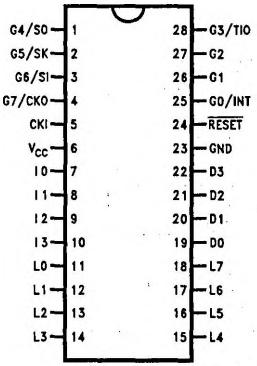



TL/DD/9103-3

Top View

**Order Number COP822C-XXX/WM, COP842C-XXX/WM, COP922C-XXX/WM or COP942C-XXX/WM**
**See NS Package Number M20B**

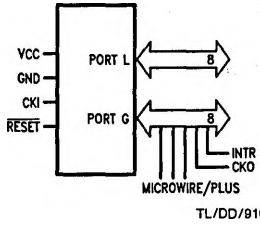
**28-Lead SO**




TL/DD/9103-18

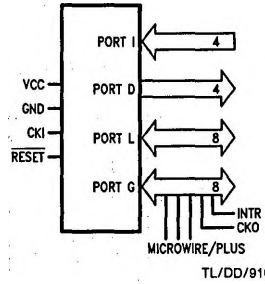
**Order Number COP820C-XXX/WM, COP840C-XXX/WM, COP920C-XXX/WM or COP940C-XXX/WM**
**See NS Package Number M28A**

**20 DIP/SO**




TL/DD/9103-6

**28 DIP/SO**




TL/DD/9103-8

**FIGURE 3. Connection Diagrams**

## Pin Descriptions

$V_{CC}$ and GND are the power supply pins.

CKI is the clock input. This can come from an external source, a R/C generated oscillator or a crystal (in conjunction with CKO). See Oscillator description.

$\overline{\text{RESET}}$ is the master reset input. See Reset description.

PORT I is a four bit Hi-Z input port.

PORT L is an 8-bit I/O port.

There are two registers associated with each L I/O port: a data register and a configuration register. Therefore, each L I/O bit can be individually configured under software control as shown below:

| Port L Config. | Port L Data | Port L Setup |
|---|---|---|
| 0 | 0 | Hi-Z Input (TRI-STATE) |
| 0 | 1 | Input With Weak Pull-Up |
| 1 | 0 | Push-Pull "0" Output |
| 1 | 1 | Push-Pull "1" Output |

Three data memory address locations are allocated for these ports, one for data register, one for configuration register and one for the input pins.

PORT G is an 8-bit port with 6 I/O pins (G0–G5) and 2 input pins (G6, G7). All eight G-pins have Schmitt Triggers on the inputs. The G7 pin functions as an input pin under normal operation and as the continue pin to exit the HALT mode. There are two registers with each I/O port: a data register and a configuration register. Therefore, each I/O bit can be individually configured under software control as shown below.

| Port G Config. | Port G Data | Port G Setup |
|---|---|---|
| 0 | 0 | Hi-Z Input (TRI-STATE) |
| 0 | 1 | Input With Weak Pull-Up |
| 1 | 0 | Push-Pull "0" Output |
| 1 | 1 | Push-Pull "1" Output |

Three data memory address locations are allocated for these ports, one for data register, one for configuration register and one for the input pins. Since G6 and G7 are input only pins, any attempt by the user to set them up as outputs by writing a one to the configuration register will be disregarded. Reading the G6 and G7 configuration bits will return zeros. Note that the chip will be placed in the HALT mode by setting the G7 data bit.

Six bits of Port G have alternate features:

G0 INTR (an external interrupt)

G3 TIO (timer/counter input/output)

G4 SO (MICROWIRE serial data output)

G5 SK (MICROWIRE clock I/O)

G6 SI (MICROWIRE serial data input)

G7 CKO crystal oscillator output (selected by mask option) or HALT restart input (general purpose input)

Pins G1 and G2 currently do not have any alternate functions.

PORT D is a four bit output port that is set high when $\overline{\text{RESET}}$ goes low. Care must be exercised with the D2 pin operation. At RESET, the external load on this pin must ensure that the output voltage stays above 0.9 $V_{CC}$ to prevent the device from entering special modes. Also, keep the external loading on the D2 pin to less than 1000 pf.

## Functional Description

*Figure 1* shows the block diagram of the internal architecture. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device.

### ALU AND CPU REGISTERS

The ALU can do an 8-bit addition, subtraction, logical or shift operation in one cycle time.

There are five CPU registers:

A is the 8-bit Accumulator register

PU is the upper 7 bits of the program counter (PC)

PL is the lower 8 bits of the program counter (PC)

B is the 8-bit address register, can be auto incremented or decremented.

X is the 8-bit alternate address register, can be incremented or decremented.

SP is the 8-bit stack pointer, points to subroutine stack (in RAM).

B, X and SP registers are mapped into the on chip RAM. The B and X registers are used to address the on chip RAM. The SP register is used to address the stack in RAM during subroutine calls and returns.

### PROGRAM MEMORY

Program memory for the COP820C family consists of 1024 bytes of ROM (2048 bytes of ROM for the COP840C family). These bytes may hold program instructions or constant data. The program memory is addressed by the 15-bit program counter (PC). ROM can be indirectly read by the LAID instruction for table lookup.

### DATA MEMORY

The data memory address space includes on chip RAM, I/O and registers. Data memory is addressed directly by the instruction or indirectly by the B, X and SP registers.

The COP820C family has 64 bytes of RAM and the COP840C family has 128 bytes of RAM. Sixteen bytes of RAM are mapped as "registers" that can be loaded immediately, decremented or tested. Three specific registers: B, X and SP are mapped into this space, the other bytes are available for general usage.

The instruction set permits any bit in memory to be set, reset or tested. All I/O and registers (except the A & PC) are memory mapped; therefore, I/O bits and register bits can be directly and individually set, reset and tested.

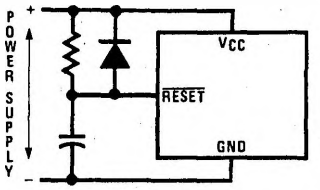
**Note:** RAM contents are undefined upon power-up.

### RESET

The $\overline{\text{RESET}}$ input when pulled low initializes the microcontroller. Initialization will occur whenever the $\overline{\text{RESET}}$ input is pulled low. Upon initialization, the ports L and G are placed in the TRI-STATE mode and the Port D is set high. The PC, PSW and CNTRL registers are cleared. The data and configuration registers for Ports L & G are cleared.

The external RC network shown in Figure 4 should be used to ensure that the $\overline{\text{RESET}}$ pin is held low until the power supply to the chip stabilizes.

## Functional Description (Continued)




TL/DD/9103-9

RC ≥ 5X Power Supply Rise Time

**FIGURE 4. Recommended Reset Circuit**

### OSCILLATOR CIRCUITS

*Figure 5* shows the three clock oscillator configurations.

### A. CRYSTAL OSCILLATOR

The device can be driven by a crystal clock. The crystal network is connected between the pins CKI and CKO.

Table I shows the component values required for various standard crystal values.

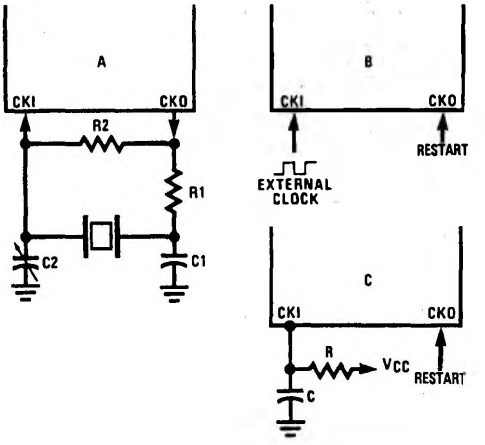
### B. EXTERNAL OSCILLATOR

CKI can be driven by an external clock signal. CKO is available as a general purpose input and/or HALT restart control.

### C. R/C OSCILLATOR

CKI is configured as a single pin RC controlled Schmitt trigger oscillator. CKO is available as a general purpose input and/or HALT restart control.

Table II shows the variation in the oscillator frequencies as functions of the component (R and C) values.




TL/DD/9103-10

**FIGURE 5. Crystal and R-C Connection Diagrams**

### OSCILLATOR MASK OPTIONS

The device can be driven by clock inputs between DC and 10 MHz.

**TABLE I. Crystal Oscillator Configuration, $T_A = 25°C$**

| R1 (kΩ) | R2 (MΩ) | C1 (pF) | C2 (pF) | CKI Freq (MHz) | Conditions |
|---|---|---|---|---|---|
| 0 | 1 | 30 | 30–36 | 10 | $V_{CC} = 5V$ |
| 0 | 1 | 30 | 30–36 | 4 | $V_{CC} = 5V$ |
| 0 | 1 | 200 | 100–150 | 0.455 | $V_{CC} = 5V$ |

**TABLE II. RC Oscillator Configuration, $T_A = 25°C$**

| R (kΩ) | C (pF) | CKI Freq. (MHz) | Instr. Cycle (μs) | Conditions |
|---|---|---|---|---|
| 3.3 | 82 | 2.2 to 2.7 | 3.7 to 4.6 | $V_{CC} = 5V$ |
| 5.6 | 100 | 1.1 to 1.3 | 7.4 to 9.0 | $V_{CC} = 5V$ |
| 6.8 | 100 | 0.9 to 1.1 | 8.8 to 10.8 | $V_{CC} = 5V$ |

**Note:** 3k ≤ R ≤ 200k, 50 pF ≤ C ≤ 200 pF

## Functional Description (Continued)

The device has three mask options for configuring the clock input. The CKI and CKO pins are automatically configured upon selecting a particular option.

— Crystal (CKI/10) CKO for crystal configuration

— External (CKI/10) CKO available as G7 input

— R/C (CKI/10) CKO available as G7 input

G7 can be used either as a general purpose input or as a control input to continue from the HALT mode.

### CURRENT DRAIN

The total current drain of the chip depends on:

1) Oscillator operating mode—I1

2) Internal switching current—I2

3) Internal leakage current—I3

4) Output source current—I4

5) DC current caused by external input not at $V_{CC}$ or GND—I5

Thus the total current drain, It is given as

$$It = I1 + I2 + I3 + I4 + I5$$

To reduce the total current drain, each of the above components must be minimum.

Operating with a crystal network will draw more current than an external square-wave. The R/C mode will draw the most. Switching current, governed by the equation below, can be reduced by lowering voltage and frequency. Leakage current can be reduced by lowering voltage and temperature. The other two items can be reduced by carefully designing the end-user's system.

$$I2 = C \times V \times f$$

Where

C = equivalent capacitance of the chip.

V = operating voltage

f = CKI frequency

### HALT MODE

The device supports a power saving mode of operation: HALT. The controller is placed in the HALT mode by setting the G7 data bit, alternatively the user can stop the clock input. In the HALT mode all internal processor activities including the clock oscillator are stopped. The fully static architecture freezes the state of the controller and retains all information until continuing. In the HALT mode, power requirements are minimal as it draws only leakage currents and output current. The applied voltage ($V_{CC}$) may be decreased down to Vr (minimum RAM retention voltage) without altering the state of the machine.

There are two ways to exit the HALT mode: via the $\overline{\text{RESET}}$ or by the CKO pin. A low on the $\overline{\text{RESET}}$ line reinitializes the microcontroller and starts executing from the address 0000H. A low to high transition on the CKO pin (only if the external or the R/C clock option is selected) causes the microcontroller to continue with no reinitialization from the address following the HALT instruction. This also resets the G7 data bit.

### INTERRUPTS

There are three interrupt sources, as shown below.

A maskable interrupt on external G0 input (positive or negative edge sensitive under software control)

A maskable interrupt on timer underflow or timer capture

A non-maskable software/error interrupt on opcode zero

### INTERRUPT CONTROL

The GIE (global interrupt enable) bit enables the interrupt function. This is used in conjunction with ENI and ENTI to select one or both of the interrupt sources. This bit is reset when interrupt is acknowledged.

ENI and ENTI bits select external and timer interrupt respectively. Thus the user can select either or both sources to interrupt the microcontroller when GIE is enabled.

IEDG selects the external interrupt edge (0 = rising edge, 1 = falling edge). The user can get an interrupt on both rising and falling edges by toggling the state of IEDG bit after each interrupt.

IPND and TPND bits signal which interrupt is pending. After interrupt is acknowledged, the user can check these two bits to determine which interrupt is pending. This permits the interrupts to be prioritized under software. The pending flags have to be cleared by the user. Setting the GIE bit high inside the interrupt subroutine allows nested interrupts.

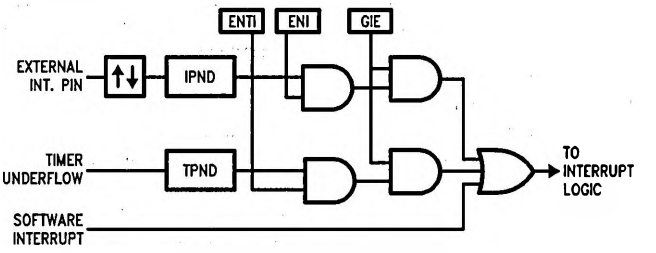
The software interrupt does not reset the GIE bit. This means that the controller can be interrupted by other interrupt sources while servicing the software interrupt.

### INTERRUPT PROCESSING

The interrupt, once acknowledged, pushes the program counter (PC) onto the stack and the stack pointer (SP) is decremented twice. The Global Interrupt Enable (GIE) bit is reset to disable further interrupts. The microcontroller then vectors to the address 00FFH and resumes execution from that address. This process takes 7 cycles to complete. At the end of the interrupt subroutine, any of the following three instructions return the processor back to the main program: RET, RETSK or RETI. Either one of the three instructions will pop the stack into the program counter (PC). The stack pointer is then incremented twice. The RETI instruction additionally sets the GIE bit to re-enable further interrupts.

Any of the three instructions can be used to return from a hardware interrupt subroutine. The RETSK instruction should be used when returning from a software interrupt subroutine to avoid entering an infinite loop.

## Functional Description (Continued)




TL/DD/9103–11

**FIGURE 6. Interrupt Block Diagram**

### DETECTION OF ILLEGAL CONDITIONS

The device contains a hardware mechanism that allows it to detect illegal conditions which may occur from coding errors, noise and 'brown out' voltage drop situations. Specifically it detects cases of executing out of undefined ROM area and unbalanced stack situations.

Reading an undefined ROM location returns 00 (hexadecimal) as its contents. The opcode for a software interrupt is also '00'. Thus a program accessing undefined ROM will cause a software interrupt.

Reading an undefined RAM location returns an FF (hexadecimal). The subroutine stack grows down for each subroutine call. By initializing the stack pointer to the top of RAM, the first unbalanced return instruction will cause the stack pointer to address undefined RAM. As a result the program will attempt to execute from FFFF (hexadecimal), which is an undefined ROM location and will trigger a software interrupt.

### MICROWIRE/PLUS™

MICROWIRE/PLUS is a serial synchronous bidirectional communications interface. The MICROWIRE/PLUS capability enables the device to interface with any of National Semiconductor's MICROWIRE peripherals (i.e. A/D converters, display drivers, EEPROMS, etc.) and with other microcontrollers which support the MICROWIRE/PLUS interface. It consists of an 8-bit serial shift register (SIO) with serial data input (SI), serial data output (SO) and serial shift clock (SK). *Figure 7* shows the block diagram of the MICROWIRE/PLUS interface.

The shift clock can be selected from either an internal source or an external source. Operating the MICROWIRE/PLUS interface with the internal clock source is called the Master mode of operation. Similarly, operating the MICROWIRE/PLUS interface with an external shift clock is called the Slave mode of operation.

The CNTRL register is used to configure and control the MICROWIRE/PLUS mode. To use the MICROWIRE/PLUS, the MSEL bit in the CNTRL register is set to one. The SK clock rate is selected by the two bits, SL0 and SL1, in the CNTRL register. Table III details the different clock rates that may be selected.

**TABLE III**

| SL1 | SL0 | SK Cycle Time |
|---|---|---|
| 0 | 0 | $2t_C$ |
| 0 | 1 | $4t_C$ |
| 1 | x | $8t_C$ |

where,

$t_C$ is the instruction cycle clock.

### MICROWIRE/PLUS OPERATION

Setting the BUSY bit in the PSW register causes the MICROWIRE/PLUS arrangement to start shifting the data. It gets reset when eight data bits have been shifted. The user may reset the BUSY bit by software to allow less than 8 bits to shift. The device may enter the MICROWIRE/PLUS mode either as a Master or as a Slave. *Figure 8* shows how two microcontrollers and several peripherals may be interconnected using the MICROWIRE/PLUS arrangement.

#### Master MICROWIRE/PLUS Operation

In the MICROWIRE/PLUS Master mode of operation the shift clock (SK) is generated internally. The MICROWIRE/PLUS Master always initiates all data exchanges. (See *Figure 8*). The MSEL bit in the CNTRL register must be set to enable the SO and SK functions onto the G Port. The SO and SK pins must also be selected as outputs by setting appropriate bits in the Port G configuration register. Table IV summarizes the bit settings required for Master mode of operation.

### SLAVE MICROWIRE/PLUS OPERATION

In the MICROWIRE/PLUS Slave mode of operation the SK clock is generated by an external source. Setting the MSEL bit in the CNTRL register enables the SO and SK functions onto the G Port. The SK pin must be selected as an input and the SO pin is selected as an output pin by appropriately setting up the Port G configuration register. Table IV summarizes the settings required to enter the Slave mode of operation.

The user must set the BUSY flag immediately upon entering the Slave mode. This will ensure that all data bits sent by the Master will be shifted properly. After eight clock pulses the BUSY flag will be cleared and the sequence may be repeated. (See *Figure 8*.)

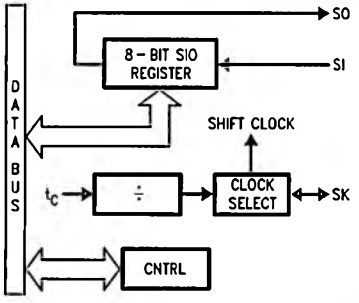
## Functional Description (Continued)

**TABLE IV**

| G4 Config. Bit | G5 Config. Bit | G4 Fun. | G5 Fun. | G6 Fun. | Operation |
|---|---|---|---|---|---|
| 1 | 1 | SO | Int. SK | SI | MICROWIRE Master |
| 0 | 1 | TRI-STATE | Int. SK | SI | MICROWIRE Master |
| 1 | 0 | SO | Ext. SK | SI | MICROWIRE Slave |
| 0 | 0 | TRI-STATE | Ext. SK | SI | MICROWIRE Slave |

### TIMER/COUNTER

The device has a powerful 16-bit timer with an associated 16-bit register enabling them to perform extensive timer functions. The timer T1 and its register R1 are each organized as two 8-bit read/write registers. Control bits in the register CNTRL allow the timer to be started and stopped under software control. The timer-register pair can be operated in one of three possible modes. Table V details various timer operating modes and their requisite control settings.




TL/DD/9103–12

**FIGURE 7. MICROWIRE/PLUS Block Diagram**

### MODE 1. TIMER WITH AUTO-LOAD REGISTER

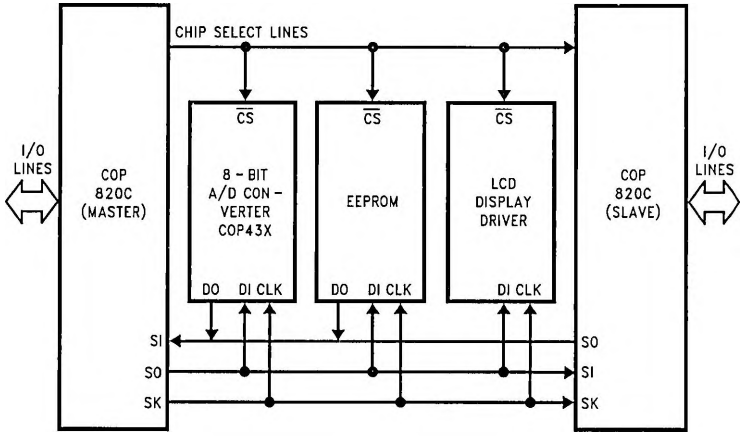
In this mode of operation, the timer T1 counts down at the instruction cycle rate. Upon underflow the value in the register R1 gets automatically reloaded into the timer which continues to count down. The timer underflow can be programmed to interrupt the microcontroller. A bit in the control register CNTRL enables the TIO (G3) pin to toggle upon timer underflows. This allow the generation of square-wave outputs or pulse width modulated outputs under software control. (See *Figure 9*)

### MODE 2. EXTERNAL COUNTER

In this mode, the timer T1 becomes a 16-bit external event counter. The counter counts down upon an edge on the TIO pin. Control bits in the register CNTRL program the counter to decrement either on a positive edge or on a negative edge. Upon underflow the contents of the register R1 are automatically copied into the counter. The underflow can also be programmed to generate an interrupt. (See *Figure 9*)

### MODE 3. TIMER WITH CAPTURE REGISTER

Timer T1 can be used to precisely measure external frequencies or events in this mode of operation. The timer T1 counts down at the instruction cycle rate. Upon the occurrence of a specified edge on the TIO pin the contents of the timer T1 are copied into the register R1. Bits in the control register CNTRL allow the trigger edge to be specified either as a positive edge or as a negative edge. In this mode the user can elect to be interrupted on the specified trigger edge. (See *Figure 10.*)




TL/DD/9103–13

**FIGURE 8. MICROWIRE/PLUS Application**

## Functional Description (Continued)

**TABLE V. Timer Operating Modes**

| CNTRL Bits 7 6 5 | Operation Mode | T Interrupt | Timer Counts On |
|---|---|---|---|
| 0 0 0 | External Counter W/Auto-Load Reg. | Timer Underflow | TIO Pos. Edge |
| 0 0 1 | External Counter W/Auto-Load Reg. | Timer Underflow | TIO Neg. Edge |
| 0 1 0 | Not Allowed | Not Allowed | Not Allowed |
| 0 1 1 | Not Allowed | Not Allowed | Not Allowed |
| 1 0 0 | Timer W/Auto-Load Reg. | Timer Underflow | $t_C$ |
| 1 0 1 | Timer W/Auto-Load Reg./Toggle TIO Out | Timer Underflow | $t_C$ |
| 1 1 0 | Timer W/Capture Register | TIO Pos. Edge | $t_C$ |
| 1 1 1 | Timer W/Capture Register | TIO Neg. Edge | $t_C$ |

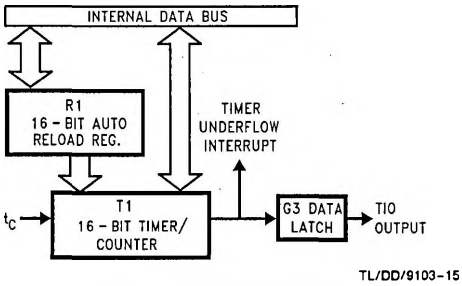



**FIGURE 9. Timer/Counter Auto Reload Mode Block Diagram**

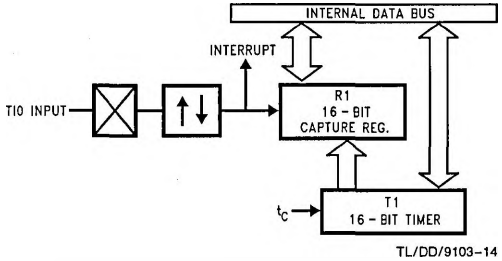



**FIGURE 10. Timer Capture Mode Block Diagram**

### TIMER PWM APPLICATION

*Figure 11* shows how a minimal component D/A converter can be built out of the Timer-Register pair in the Auto-Reload mode. The timer is placed in the "Timer with auto reload" mode and the TIO pin is selected as the timer output. At the outset the TIO pin is set high, the timer T1 holds the on time and the register R1 holds the signal off time. Setting TRUN bit starts the timer which counts down at the instruction cycle rate. The underflow toggles the TIO output and copies the off time into the timer, which continues to run. By alternately loading in the on time and the off time at each successive interrupt a PWM frequency can be easily generated.

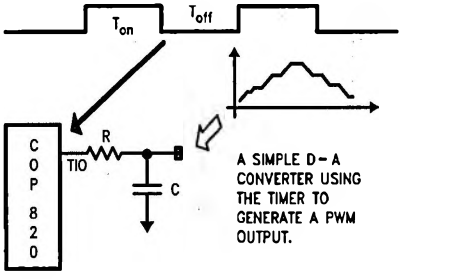



**FIGURE 11. Timer Application**

## Control Registers

**CNTRL REGISTER (ADDRESS X'00EE)**

The Timer and MICROWIRE/PLUS control register contains the following bits:

| | |
|---|---|
| SL1 & SL0 | Select the MICROWIRE/PLUS clock divide-by |
| IEDG | External interrupt edge polarity select (0 = rising edge, 1 = falling edge) |
| MSEL | Enable MICROWIRE/PLUS functions SO and SK |
| TRUN | Start/Stop the Timer/Counter (1 = run, 0 = stop) |
| TC3 | Timer input edge polarity select (0 = rising edge, 1 = falling edge) |
| TC2 | Selects the capture mode |
| TC1 | Selects the timer mode |

| TC1 | TC2 | TC3 | TRUN | MSEL | IEDG | SL1 | SL0 |
|---|---|---|---|---|---|---|---|

BIT 7 BIT 0

**PSW REGISTER (ADDRESS X'00EF)**

The PSW register contains the following select bits:

| | |
|---|---|
| GIE | Global interrupt enable |
| ENI | External interrupt enable |
| BUSY | MICROWIRE/PLUS busy shifting |
| IPND | External interrupt pending |
| ENTI | Timer interrupt enable |
| TPND | Timer interrupt pending |
| C | Carry Flag |
| HC | Half carry Flag |

| HC | C | TPND | ENTI | IPND | BUSY | ENI | GIE |
|---|---|---|---|---|---|---|---|

Bit 7 Bit 0

## Addressing Modes

**REGISTER INDIRECT**

This is the "normal" mode of addressing. The operand is the memory addressed by the B register or X register.

**DIRECT**

The instruction contains an 8-bit address field that directly points to the data memory for the operand.

**IMMEDIATE**

The instruction contains an 8-bit immediate field as the operand.

**REGISTER INDIRECT (AUTO INCREMENT AND DECREMENT)**

This is a register indirect mode that automatically increments or decrements the B or X register after executing the instruction.

**RELATIVE**

This mode is used for the JP instruction, the instruction field is added to the program counter to get the new program location. JP has a range of from −31 to +32 to allow a one byte relative jump (JP + 1 is implemented by a NOP instruction). There are no 'pages' when using JP, all 15 bits of PC are used.

## Memory Map

All RAM, ports and registers (except A and PC) are mapped into data memory address space.

| Address | Contents |
|---|---|
| **COP820C Family** | |
| 00 to 2F | On Chip RAM Bytes |
| 30 to 7F | Unused RAM Address Space (Reads as all Ones) |
| **COP840C Family** | |
| 00 to 6F | On Chip RAM Bytes |
| 70 to 7F | Unused RAM Address Space (Reads as all Ones) |
| **COP820C and COP840C Families** | |
| 80 to BF | Expansion Space for on Chip EERAM |
| C0 to CF | Expansion Space for I/O and Registers |
| D0 to DF | On Chip I/O and Registers |
| D0 | Port L Data Register |
| D1 | Port L Configuration Register |
| D2 | Port L Input Pins (Read Only) |
| D3 | Reserved for Port L |
| D4 | Port G Data Register |
| D5 | Port G Configuration Register |
| D6 | Port G Input Pins (Read Only) |
| D7 | Port I Input Pins (Read Only) |
| D8–DB | Reserved for Port C |
| DC | Port D Data Register |
| DD–DF | Reserved for Port D |
| E0 to EF | On Chip Functions and Registers |
| E0–E7 | Reserved for Future Parts |
| E8 | Reserved |
| E9 | MICROWIRE/PLUS Shift Register |
| EA | Timer Lower Byte |
| EB | Timer Upper Byte |
| EC | Timer Autoload Register Lower Byte |
| ED | Timer Autoload Register Upper Byte |
| EE | CNTRL Control Register |
| EF | PSW Register |
| F0 to FF | On Chip RAM Mapped as Registers |
| FC | X Register |
| FD | SP Register |
| FE | B Register |

Reading unused memory locations below 7FH will return all ones. Reading other unused memory locations will return undefined data.

# Instruction Set

## REGISTER AND SYMBOL DEFINITIONS

### Registers

| | |
|---|---|
| A | 8-bit Accumulator register |
| B | 8-bit Address register |
| X | 8-bit Address register |
| SP | 8-bit Stack pointer register |
| PC | 15-bit Program counter register |
| PU | upper 7 bits of PC |
| PL | lower 8 bits of PC |
| C | 1-bit of PSW register for carry |
| HC | Half Carry |
| GIE | 1-bit of PSW register for global interrupt enable |

### Symbols

| | |
|---|---|
| [B] | Memory indirectly addressed by B register |
| [X] | Memory indirectly addressed by X register |
| Mem | Direct address memory or [B] |
| Meml | Direct address memory or [B] or Immediate data |
| Imm | 8-bit Immediate data |
| Reg | Register memory: addresses F0 to FF (Includes B, X and SP) |
| Bit | Bit number (0 to 7) |
| ← | Loaded with |
| ↔ | Exchanged with |

## Instruction Set

| | | |
|---|---|---|
| ADD | add | A ← A + Meml |
| ADC | add with carry | A ← A + Meml + C, C ← Carry<br>HC ← Half Carry |
| SUBC | subtract with carry | A ← A + $\overline{\text{Meml}}$ + C, C ← Carry<br>HC ← Half Carry |
| AND | Logical AND | A ← A and Meml |
| OR | Logical OR | A ← A or Meml |
| XOR | Logical Exclusive-OR | A ← A xor Meml |
| IFEQ | IF equal | Compare A and Meml, Do next if A = Meml |
| IFGT | IF greater than | Compare A and Meml, Do next if A > Meml |
| IFBNE | IF B not equal | Do next if lower 4 bits of B ≠ Imm |
| DRSZ | Decrement Reg. ,skip if zero | Reg ← Reg − 1, skip if Reg goes to 0 |
| SBIT | Set bit | 1 to bit,<br>Mem (bit = 0 to 7 immediate) |
| RBIT | Reset bit | 0 to bit,<br>Mem |
| IFBIT | If bit | If bit,<br>Mem is true, do next instr. |
| X | Exchange A with memory | A ↔ Mem |
| LD A | Load A with memory | A ← Meml |
| LD mem | Load Direct memory Immed. | Mem ← Imm |
| LD Reg | Load Register memory Immed. | Reg ← Imm |
| X | Exchange A with memory [B] | A ↔ [B] (B ← B ± 1) |
| X | Exchange A with memory [X] | A ↔ [X] (X ← X ± 1) |
| LD A | Load A with memory [B] | A ← [B] (B ← B ± 1) |
| LD A | Load A with memory [X] | A ← [X] (X ← X ± 1) |
| LD M | Load Memory Immediate | [B] ← Imm (B ← B ± 1) |
| CLRA | Clear A | A ← 0 |
| INCA | Increment A | A ← A + 1 |
| DECA | Decrement A | A ← A − 1 |
| LAID | Load A indirect from ROM | A ← ROM(PU,A) |
| DCORA | DECIMAL CORRECT A | A ← BCD correction (follows ADC, SUBC) |
| RRCA | ROTATE A RIGHT THRU C | C → A7 → ... → A0 → C |
| SWAPA | Swap nibbles of A | A7 ... A4 ↔ A3 ... A0 |
| SC | Set C | C ← 1, HC ← 1 |
| RC | Reset C | C ← 0, HC ← 0 |
| IFC | If C | If C is true, do next instruction |
| IFNC | If not C | If C is not true, do next instruction |
| JMPL | Jump absolute long | PC ← ii (ii = 15 bits, 0 to 32k) |
| JMP | Jump absolute | PC11..0 ← i (i = 12 bits) |
| JP | Jump relative short | PC ← PC + r (r is −31 to +32, not 1) |
| JSRL | Jump subroutine long | [SP] ← PL,[SP-1] ← PU,SP-2,PC ← ii |
| JSR | Jump subroutine | [SP] ← PL,[SP-1] ← PU,SP-2,PC11..0 ← i |
| JID | Jump indirect | PL ← ROM(PU,A) |
| RET | Return from subroutine | SP+2,PL ← [SP],PU ← [SP-1] |
| RETSK | Return and Skip | SP+2,PL ← [SP],PU ← [SP-1],Skip next instruction |
| RETI | Return from Interrupt | SP+2,PL ← [SP],PU ← [SP-1],GIE ← 1 |
| INTR | Generate an interrupt | [SP] ← PL,[SP−1] ← PU,SP-2,PC ← 0FF |
| NOP | No operation | PC ← PC + 1 |

Bits 7–4

| F | E | D | C | B | A | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| JP -15 | JP -31 | LD 0F0,#i | DRSZ 0F0 | RRCA | RC | ADC A, #i | ADC A, [B] | IFBIT 0,[B] | * | LD B, 0F | IFBNE 0 | JSR 0000-00FF | JMP 0000-00FF | JP + 17 | INTR | 0 |
| JP -14 | JP -30 | LD 0F1,#i | DRSZ 0F1 | * | SC | SUBC A, #i | SUBC A,[B] | IFBIT 1,[B] | * | LD B, 0E | IFBNE 1 | JSR 0100-01FF | JMP 0100-01FF | JP + 18 | JP + 2 | 1 |
| JP -13 | JP -29 | LD 0F2,#i | DRSZ 0F2 | X A, [X+] | X A, [B+] | IFEQ A, #i | IFEQ A,[B] | IFBIT 2,[B] | * | LD B, 0D | IFBNE 2 | JSR 0200-02FF | JMP 0200-02FF | JP + 19 | JP + 3 | 2 |
| JP -12 | JP -28 | LD 0F3,#i | DRSZ 0F3 | X A, [X−] | X A, [B−] | IFGT A, #i | IFGT A,[B] | IFBIT 3,[B] | * | LD B, 0C | IFBNE 3 | JSR 0300-03FF | JMP 0300-03FF | JP + 20 | JP + 4 | 3 |
| JP -11 | JP -27 | LD 0F4,#i | DRSZ 0F4 | * | LAID | ADD A, #i | ADD A,[B] | IFBIT 4,[B] | CLRA | LD B, 0B | IFBNE 4 | JSR 0400-04FF | JMP 0400-04FF | JP + 21 | JP + 5 | 4 |
| JP -10 | JP -26 | LD 0F5,#i | DRSZ 0F5 | * | JID | AND A, #i | AND A,[B] | IFBIT 5,[B] | SWAPA | LD B, 0A | IFBNE 5 | JSR 0500-05FF | JMP 0500-05FF | JP + 22 | JP + 6 | 5 |
| JP -9 | JP -25 | LD 0F6,#i | DRSZ 0F6 | X A, [X] | X A, [B] | XOR A, #i | XOR A,[B] | IFBIT 6,[B] | DCORA | LD B, 9 | IFBNE 6 | JSR 0600-06FF | JMP 0600-06FF | JP + 23 | JP + 7 | 6 |
| JP -8 | JP -24 | LD 0F7,#i | DRSZ 0F7 | * | * | OR A, #i | OR A,[B] | IFBIT 7,[B] | * | LD B, 8 | IFBNE 7 | JSR 0700-07FF | JMP 0700-07FF | JP + 24 | JP + 8 | 7 |
| JP -7 | JP -23 | LD 0F8,#i | DRSZ 0F8 | NOP | * | LD A, #i | IFC | SBIT 0,[B] | RBIT 0,[B] | LD B, 7 | IFBNE 8 | JSR 0800-08FF | JMP 0800-08FF | JP + 25 | JP + 9 | 8 |
| JP -6 | JP -22 | LD 0F9,#i | DRSZ 0F9 | * | * | * | IFNC | SBIT 1,[B] | RBIT 1,[B] | LD B, 6 | IFBNE 9 | JSR 0900-09FF | JMP 0900-09FF | JP + 26 | JP + 10 | 9 |
| JP -5 | JP -21 | LD 0FA,#i | DRSZ 0FA | LD A, [X+] | LD A, [B+] | LD [B+],#i | INCA | SBIT 2,[B] | RBIT 2,[B] | LD B, 5 | IFBNE 0A | JSR 0A00-0AFF | JMP 0A00-0AFF | JP + 27 | JP + 11 | A |
| JP -4 | JP -20 | LD 0FB,#i | DRSZ 0FB | LD A, [X−] | LD A, [B−] | LD [B−],#i | DECA | SBIT 3,[B] | RBIT 3,[B] | LD B, 4 | IFBNE 0B | JSR 0B00-0BFF | JMP 0B00-0BFF | JP + 28 | JP + 12 | B |
| JP -3 | JP -19 | LD 0FC,#i | DRSZ 0FC | LD Md, #i | JMPL | X A,Md | * | SBIT 4,[B] | RBIT 4,[B] | LD B, 3 | IFBNE 0C | JSR 0C00-0CFF | JMP 0C00-0CFF | JP + 29 | JP +13 | C |
| JP -2 | JP -18 | LD 0FD,#i | DRSZ 0FD | DIR | JSRL | LD A, Md | RETSK | SBIT 5,[B] | RBIT 5,[B] | LD B, 2 | IFBNE 0D | JSR 0D00-0DFF | JMP 0D00-0DFF | JP + 30 | JP +14 | D |
| JP -1 | JP -17 | LD 0FE,#i | DRSZ 0FE | LD A, [X] | LD A, [B] | LD [B], #i | RET | SBIT 6, [B] | RBIT 6, [B] | LD B, 1 | IFBNE 0E | JSR 0E00−0EFF | JMP 0E00−0EFF | JP + 31 | JP +15 | E |
| JP -0 | JP -16 | LD 0FF,#1 | DRSZ 0FF | * | * | * | RETI | SBIT 7,[B] | RBIT 7,[B] | LD B, 0 | IFBNE 0F | JSR 0F00-0FFF | JMP 0F00-0FFF | JP + 32 | JP + 16 | F |

Bits 3–0

where, i is the immediate data Md is a directly addressed memory location * is an unused opcode (see following table)

## Instruction Execution Time

Most instructions are single byte (with immediate addressing mode instruction taking two bytes).

Most single instructions take one cycle time to execute.

See the BYTES and CYCLES per INSTRUCTION table for details.

## BYTES and CYCLES per INSTRUCTION

The following table shows the number of bytes and cycles for each instruction in the format of byte/cycle.

**Arithmetic and Logic Instructions**

| | [B] | Direct | Immed. |
|---|---|---|---|
| ADD | 1/1 | 3/4 | 2/2 |
| ADC | 1/1 | 3/4 | 2/2 |
| SUBC | 1/1 | 3/4 | 2/2 |
| AND | 1/1 | 3/4 | 2/2 |
| OR | 1/1 | 3/4 | 2/2 |
| XOR | 1/1 | 3/4 | 2/2 |
| IFEQ | 1/1 | 3/4 | 2/2 |
| IFGT | 1/1 | 3/4 | 2/2 |
| IFBNE | 1/1 | | |
| DRSZ | | 1/3 | |
| SBIT | 1/1 | 3/4 | |
| RBIT | 1/1 | 3/4 | |
| IFBIT | 1/1 | 3/4 | |

**Memory Transfer Instructions**

| | Register Indirect [B] | Register Indirect [X] | Direct | Immed. | Register Indirect Auto Incr & Decr [B+, B−] | Register Indirect Auto Incr & Decr [X+, X−] | |
|---|---|---|---|---|---|---|---|
| X A,* | 1/1 | 1/3 | 2/3 | | 1/2 | 1/3 | |
| LD A,* | 1/1 | 1/3 | 2/3 | 2/2 | 1/2 | 1/3 | |
| LD B,Imm | | | | 1/1 | | | (If B < 16) |
| LD B,Imm | | | | 2/3 | | | (If B > 15) |
| LD Mem,Imm | 2/2 | | 3/3 | | 2/2 | | |
| LD Reg,Imm | | | | 2/3 | | | |

* => Memory location addressed by B or X or directly.

**Instructions Using A & C**

| | |
|---|---|
| CLRA | 1/1 |
| INCA | 1/1 |
| DECA | 1/1 |
| LAID | 1/3 |
| DCORA | 1/1 |
| RRCA | 1/1 |
| SWAPA | 1/1 |
| SC | 1/1 |
| RC | 1/1 |
| IFC | 1/1 |
| IFNC | 1/1 |

**Transfer of Control Instructions**

| | |
|---|---|
| JMPL | 3/4 |
| JMP | 2/3 |
| JP | 1/3 |
| JSRL | 3/5 |
| JSR | 2/5 |
| JID | 1/3 |
| RET | 1/5 |
| RETSK | 1/5 |
| RETI | 1/5 |
| INTR | 1/7 |
| NOP | 1/1 |

The following table shows the instructions assigned to unused opcodes. This table is for information only. The operations performed are subject to change without notice. Do not use these opcodes.

| Unused Opcode | Instruction | Unused Opcode | Instruction |
|---|---|---|---|
| 60 | NOP | A9 | NOP |
| 61 | NOP | AF | LD A, [B] |
| 62 | NOP | B1 | C → HC |
| 63 | NOP | B4 | NOP |
| 67 | NOP | B5 | NOP |
| 8C | RET | B7 | X A, [X] |
| 99 | NOP | B9 | NOP |
| 9F | LD [B], #i | BF | LD A, [X] |
| A7 | X A, [B] | | |
| A8 | NOP | | |

## Option List

The mask programmable options are listed out below. The options are programmed at the same time as the ROM pattern to provide the user with hardware flexibility to use a variety of oscillator configuration.

**OPTION 1: CKI INPUT**

= 1 Crystal (CKI/10) CKO for crystal configuration
= 2 External (CKI/10) CKO available as G7 input
= 3 R/C (CKI/10) CKO available as G7 input

**OPTION 2: BONDING**

= 1 28 pin package
= 2 N.A.
= 3 20 pin package
= 4 20 SO package
= 5 28 SO package

The following option information is to be sent to National along with the EPROM.

**Option Data**

Option 1 Value_is: CKI Input

Option 2 Value_is: COP Bonding

**How to Order**

To order a complete development package, select the section for the microcontroller to be developed and order the parts listed. Contact the sales office for more detail.

## Development Support

**IN-CIRCUIT EMULATOR**

The MetaLink iceMASTER™—COP8 Model 400 In-Circuit Emulator for the COP8 family of microcontrollers features high-performance operation, ease of use, and an extremely flexible user-interface for maximum productivity. Interchangeable probe cards, which connect to the standard common base, support the various configurations and packages of the COP8 family.

The iceMASTER provides real time, full speed emulation up to 10 MHz, 32 kBytes of emulation memory and 4k frames of trace buffer memory. The user may define as many as 32k trace and break triggers which can be enabled, disabled, set or cleared. They can be simple triggers based on code or address ranges or complex triggers based on code address, direct address, opcode value, opcode class or immediate operand. Complex breakpoints can be ANDed and ORed together. Trace information consists of address bus values, opcodes and user selectable probe clips status (external event lines). The trace buffer can be viewed as raw hex or as disassembled instructions. The probe clip bit values can be displayed in binary, hex or digital waveform formats.

During single-step operation the dynamically annotated code feature displays the contents of all accessed (read and write) memory locations and registers, as well as flow-of-control direction change markers next to each instruction executed.

The iceMASTER's performance analyzer offers a resolution of better than 6 μs. The user can easily monitor the time spent executing specific portions of code and find "hot spots" or "dead code". Up to 15 independent memory areas based on code address or label ranges can be defined. Analysis results can be viewed in bargraph format or as actual frequency count.

Emulator memory operations for program memory include single line assembler, disassembler, view, change and write to file. Data memory operations include fill, move, compare, dump to file, examine and modify. The contents of any memory space can be directly viewed and modified from the corresponding window.

The iceMASTER comes with an easy to use windowed interface. Each window can be sized, highlighted, color-controlled, added, or removed completely. Commands can be accessed via pull-down-menus and/or redefineable hot keys. A context sensitive hypertext/hyperlinked on-line help system explains clearly the options the user has from within any window.

The iceMASTER connects easily to a PC via the standard COMM port and its 115.2 kBaud serial link keeps typical program download time to under 3 seconds.

The following tables list the emulator and probe cards ordering information:

**Emulator Ordering Information**

| Part Number | Description | Current Version |
|---|---|---|
| IM-COP8/400/1‡ | MetaLink base unit in-circuit emulator for all COP8 devices, symbolic debugger software and RS-232 serial interface cable, with 110V @ 60 Hz Power Supply. | HOST SOFTWARE: VER. 3.3 REV.5, Model File Rev 3.050. |
| IM-COP8/400/2‡ | MetaLink base unit in-circuit emulator for all COP8 devices, symbolic debugger software and RS-232 serial interface cable, with 220V @ 50 Hz Power Supply. | |
| DM-COP8/880/‡ | MetaLink iceMASTER Debug Module. This is the low cost version of the MetaLink iceMASTER. Firmware: Ver.6.07. | |

‡These parts include National's COP8 Assembler/Linker/Librarian Package (COP8-DEV-IBMA)

## Development Support (Continued)

**Probe Card Ordering Information**

| Part Number | Package | Voltage Range | Emulates |
|---|---|---|---|
| MHW-880C20D5PC | 20 DIP | 4.5V–5.5V | COP822C, 842C, 8782C |
| MHW-880C20DWPC | 20 DIP | 2.5V–6.0V | COP822C, 842C, 8782C |
| MHW-880C28D5PC | 28 DIP | 4.5V–5.5V | COP820C, 840C, 881C, 8781C |
| MHW-880C28DWPC | 28 DIP | 2.5V–6.0V | COP820C, 840C, 881C, 8781C |

### MACRO CROSS ASSEMBLER

National Semiconductor offers a COP8 macro cross assembler. It runs on industry standard compatible PCs and supports all of the full-symbolic debugging features of the MetaLink iceMASTER emulators.

**Assembler Ordering Information**

| Part Number | Description | Manual |
|---|---|---|
| COP8-DEV-IBMA | COP8 Assembler/ Linker/Librarian for IBM®, PC-XT®, AT® or compatible | 424410632-001 |

### SINGLE CHIP EMULATOR DEVICE

The COP8 family is fully supported by single chip form, fit, and function emulators. For more detailed information refer to the emulation device specific data sheets and the emulator selection table below.

**Single Chip Emulator Selection Table**

| Device Number | Clock Option | Package | Description | Emulates |
|---|---|---|---|---|
| COP8781CN | Programmable | 28 DIP | One Time Programmable (OTP) | COP840C, COP820C |
| COP8781CJ | Programmable | 28 DIP | UV Erasable | COP840C, COP820C |
| COP8781CWM | Programmable | 28 SO | OTP | COP840C, COP820C |
| COP8782CN | Programmable | 20 DIP | OTP | COP842C, COP822C |
| COP8782CJ | Programmable | 20 DIP | UV Erasable | COP842C, COP822C |
| COP8782CWM | Programmable | 20 SO | OTP | COP842C, COP822C |

## Development Support (Continued)

### PROGRAMMING SUPPORT

Programming of the single chip emulator devices is supported by different sources. The following programmers are certified for programming the One Time Programmable (OTP) devices:

**EPROM Programmer Information**

| Manufacturer and Product | U.S. Phone Number | Europe Phone Number | Asia Phone Number |
|---|---|---|---|
| MetaLink-Debug Module | (602) 926-0797 | Germany: +49-81-41-1030 | Hong Kong: +852-737-1800 |
| Xeltek-Superpro | (408) 745-7974 | Germany: +49-20-41 684758 | Singapore: +65 276 6433 |
| BP Microsystems-EP-1140 | (800) 225-2102 | Germany: +49-89-857 66 67 | Hong Kong: +852 388 0629 |
| Data I/O- Unisite; -System 29, -System 39 | (800) 322-8246 | Europe: +31-20-622866<br>Germany: +49-89-85-8020 | Japan: +33-432-6991 |
| Abcom- COP8 Programmer | | Europe: +89 80 8707 | |
| System General Turpro-1-FX; -APRO | (408) 263-6667 | Switzerland: +31-921-7844 | Taiwan Taipei: +2-9173005 |

### INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities could be found. The minimum requirement for accessing the Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down-loaded to disk for later use.

**ORDER P/N: MOLE-DIAL-A-HLP**

Information System Package contains:

Dial-A-Helper Users Manual

Public Domain Communications Software

### FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factory applications support. If a user has questions, he can leave messages on our electronic bulletin board, which we will respond to.

Voice: (800) 272-9959

Modem: CANADA/U.S.: (800) NSC-MICRO
(800) 672-6427

Baud: 14.4k

Setup: Length: 8-Bit
Parity: None
Stop Bit: 1

Operation: 24 Hrs. 7 Days