

## COP420/COP421/COP422 and COP320/COP321/COP322 Single-Chip N-Channel Microcontrollers

### General Description

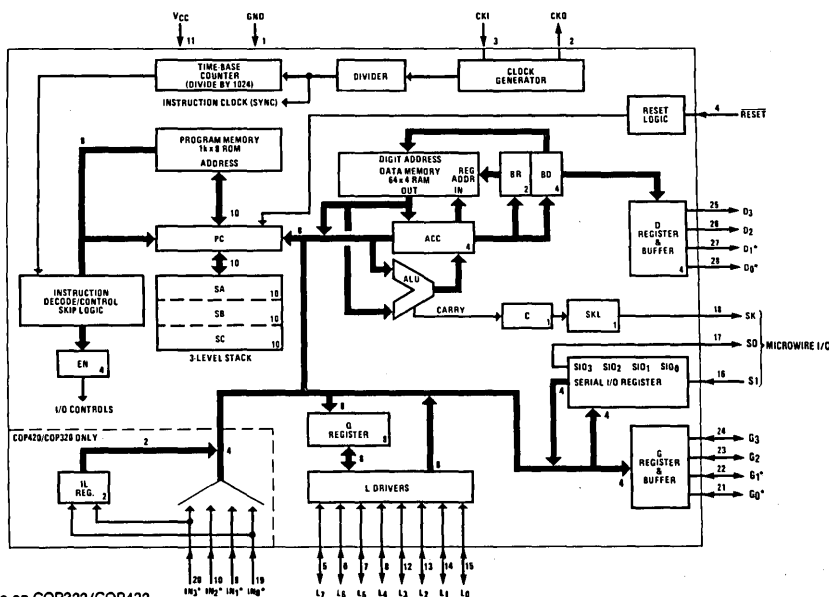
The COP420, COP421, COP422, COP320, COP321 and COP322 Single-Chip N-Channel Microcontrollers are members of the COP<sup>SM</sup> family, fabricated using N-channel, silicon gate MOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The COP421 is identical to the COP420, except with 19 I/O lines instead of 23; the COP422 has 15 I/O lines. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

The COP320 is the extended temperature range version of the COP420 (likewise the COP321 and COP322 are the extended temperature range versions of the COP421/COP422). The COP320/321/322 are exact functional equivalents of the COP420/421/422.

### Features

- Low cost
- Powerful instruction set
- 1k x 8 ROM, 64 x 4 RAM
- 23 I/O lines (COP420, COP320)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 4.0  $\mu$ s instruction time
- Single supply operation
- Internal time-base counter for real-time processing
- Internal binary counter register with MICROWIRE<sup>TM</sup> compatible serial I/O capacity
- General purpose and TRI-STATE<sup>®</sup> outputs
- TTL/CMOS compatible in and out
- LED direct drive outputs
- Software/hardware compatible with other members of COP400 family
- Extended temperature range device COP320/COP321/COP322 ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

### Block Diagram



\*Not available on COP322/COP422.

FIGURE 1

TL/DD/6921-1

**COP420/COP421/COP422 and COP320/COP321/COP322****Absolute Maximum Ratings**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin -0.3V to +7V

Operating Temperature Range

COP420/COP421/COP422 0°C to 70°C

COP320/COP321/COP322 -40°C to +85°C

Storage Temperature Range -65°C to +150°C

Total Sink Current 75 mA

Total Source Current 95 mA

Package Power Dissipation  
24 and 28 pin

750 mW at 25°C

400 mW at 70°C

250 mW at 85°C

Package Power Dissipation  
20 pin

650 mW at 25°C

300 mW at 70°C

200 mW at 85°C

Lead Temperature (soldering, 10 sec.) 300°C

*Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

**COP420/COP421/COP422****DC Electrical Characteristics** 0°C ≤ T<sub>A</sub> ≤ +70°C, 4.5V ≤ V<sub>CC</sub> ≤ 6.3V unless otherwise noted

| Parameter                     | Conditions                                                   | Min                 | Max  | Units |
|-------------------------------|--------------------------------------------------------------|---------------------|------|-------|
| Operation Voltage             |                                                              | 4.5                 | 6.3  | V     |
| Power Supply Ripple           | Peak to Peak (Note 3)                                        |                     | 0.4  | V     |
| Supply Current                | Outputs Open                                                 |                     | 38   | mA    |
| Supply Current                | Outputs Open,<br>V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C |                     | 30   | mA    |
| Input Voltage Levels          |                                                              |                     |      |       |
| CKI Input Levels              |                                                              |                     |      |       |
| Crystal Input                 |                                                              |                     |      |       |
| Logic High                    | V <sub>CC</sub> = Max.                                       | 3.0                 |      |       |
| Logic High                    | V <sub>CC</sub> = 5V ± 5%                                    | 2.0                 |      | V     |
| Logic Low                     |                                                              | -0.3                | 0.4  | V     |
| TTL Input                     | V <sub>CC</sub> = 5V ± 5%                                    |                     |      |       |
| Logic High                    |                                                              | 2.0                 |      | V     |
| Logic Low                     |                                                              | -0.3                | 0.8  | V     |
| Schmitt Trigger Inputs        |                                                              |                     |      |       |
| RESET, CKI (÷ 4)              |                                                              |                     |      |       |
| Logic High                    |                                                              | 0.7 V <sub>CC</sub> |      | V     |
| Logic Low                     |                                                              | -0.3                | 0.6  | V     |
| SO Input Level (Test Mode)    | (Note 2)                                                     | 2.0                 | 3.0  | V     |
| All Other Inputs              |                                                              |                     |      |       |
| Logic High                    | V <sub>CC</sub> = Max.                                       | 3.0                 |      | V     |
| Logic High                    | V <sub>CC</sub> = 5V ± 5%                                    | 2.0                 |      | V     |
| Logic Low                     |                                                              | -0.3                | 0.8  | V     |
| Input Levels High Trip Option |                                                              |                     |      |       |
| Logic High                    |                                                              | 3.6                 |      | V     |
| Logic Low                     |                                                              | -0.3                | 1.2  | V     |
| Input Load Source Current     | V <sub>CC</sub> = 5V                                         |                     |      |       |
| CKO                           |                                                              | -4                  | -800 | μA    |
| All Others                    |                                                              | -100                | -800 | μA    |
| Input Capacitance             |                                                              |                     | 7    | pF    |
| Hi-Z Input Leakage            |                                                              | -1                  | +1   | μA    |
| Output Voltage Levels         |                                                              |                     |      |       |
| Standard Outputs              |                                                              |                     |      |       |
| TTL Operation                 | V <sub>CC</sub> = 5V ± 10%                                   |                     |      |       |
| Logic High                    | I <sub>OH</sub> = -100 μA                                    | 2.4                 |      | V     |
| Logic Low                     | I <sub>OL</sub> = 1.6 mA                                     | -0.3                | 0.4  | V     |
| CMOS Operation (Note 1)       |                                                              |                     |      |       |
| Logic High                    | I <sub>OH</sub> = -10 μA                                     | V <sub>CC</sub> - 1 |      | V     |
| Logic Low                     | I <sub>OL</sub> = +10 μA                                     |                     | 0.2  | V     |

Note 1: TRI-STATE and LED configurations are excluded.

Note 2: SO output "0" level must be less than 0.8V for normal operation.

**COP420/COP421/COP422****DC Electrical Characteristics**  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$  unless otherwise noted (Continued)

| Parameter                               | Conditions                                      | Min  | Max  | Units         |
|-----------------------------------------|-------------------------------------------------|------|------|---------------|
| Output Current Levels                   |                                                 |      |      |               |
| LED Direct Drive Output                 | $V_{CC} = 6\text{V}$                            |      |      |               |
| Logic High                              | $V_{OH} = 2.0\text{V}$                          | 2.5  | 14   | mA            |
| CKI Sink Current (R/C Option)           | $V_{IN} = 3.5\text{V}$                          | 2    |      | mA            |
| CKO (RAM Supply Current)                | $V_R = 3.3\text{V}$                             |      | 3    | mA            |
| TRI-STATE or Open Drain Leakage Current | $V_{CC} = 5\text{V}$                            | -2.5 | +2.5 | $\mu\text{A}$ |
| Output Current Levels                   |                                                 |      |      |               |
| Output Sink Current ( $I_{OL}$ )        | $V_{CC} = 4.5\text{V}$ , $V_{OL} = 0.4\text{V}$ | +1.6 |      | mA            |
| Output Source Current ( $I_{OH}$ )      |                                                 |      |      |               |
| Standard Configuration                  |                                                 |      |      |               |
| All Outputs                             | $V_{CC} = 6.3\text{V}$ , $V_{OH} = 3.0\text{V}$ | -200 | -900 | $\mu\text{A}$ |
|                                         | $V_{CC} = 4.5\text{V}$ , $V_{OH} = 2.0\text{V}$ | -100 | -500 | $\mu\text{A}$ |
| Push-Pull Configuration                 |                                                 |      |      |               |
| SO, SK Outputs                          | $V_{CC} = 6.3\text{V}$ , $V_{OH} = 3.0\text{V}$ | -1.0 |      | mA            |
|                                         | $V_{CC} = 4.5\text{V}$ , $V_{OH} = 2.0\text{V}$ | -0.4 |      | mA            |
| TRI-STATE Configuration                 |                                                 |      |      |               |
| $L_0$ - $L_7$ Outputs                   | $V_{CC} = 6.3\text{V}$ , $V_{OH} = 3.2\text{V}$ | -0.8 |      | mA            |
|                                         | $V_{CC} = 4.5\text{V}$ , $V_{OH} = 1.5\text{V}$ | -0.9 |      | mA            |
| LED Configuration                       |                                                 |      |      |               |
| $L_0$ - $L_7$ Outputs                   | $V_{CC} = 6.3\text{V}$ , $V_{OH} = 3.0\text{V}$ | -1.0 |      | mA            |
|                                         | $V_{CC} = 4.5\text{V}$ , $V_{OH} = 2.0\text{V}$ | -0.5 |      | mA            |
| Allowable Sink Current                  |                                                 |      |      |               |
| Per Pin (L, D, G)                       |                                                 |      | 10   | mA            |
| Per Pin (All Others)                    |                                                 |      | 2    | mA            |
| Per Port (L)                            |                                                 |      | 16   | mA            |
| Per Port (D, G)                         |                                                 |      | 10   | mA            |
| Allowable Source Current                |                                                 |      |      |               |
| Per Pin (L)                             |                                                 |      | -15  | mA            |
| Per Pin (All Others)                    |                                                 |      | -1.5 | mA            |

**COP320/COP321/COP322****DC Electrical Characteristics**  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$  unless otherwise noted

| Parameter                               | Conditions                                 | Min          | Max  | Units         |
|-----------------------------------------|--------------------------------------------|--------------|------|---------------|
| Operation Voltage                       |                                            | 4.5          | 5.5  | V             |
| Power Supply Ripple                     | Peak to Peak (Note 3)                      |              | 0.4  | V             |
| Supply Current                          | $T_A = -40^{\circ}\text{C}$ , Outputs Open |              | 40   | mA            |
| Input Voltage Levels                    |                                            |              |      |               |
| CKI Input Levels                        |                                            |              |      |               |
| Crystal Input                           |                                            |              |      |               |
| Logic High                              |                                            | 2.2          |      | V             |
| Logic Low                               |                                            | -0.3         | 0.3  | V             |
| TTL Input                               | $V_{CC} = 5\text{V} \pm 5\%$               |              |      |               |
| Logic High                              |                                            | 2.2          |      | V             |
| Logic Low                               |                                            | -0.3         | 0.6  | V             |
| Schmitt Trigger Inputs                  |                                            |              |      |               |
| RESET, CKI (+4)                         |                                            |              |      |               |
| Logic High                              |                                            | $0.7 V_{CC}$ |      | V             |
| Logic Low                               |                                            | -0.3         | 0.4  | V             |
| SO Input Level (Test Mode)              | (Note 2)                                   | 2.0          | 3.0  | V             |
| All Other Inputs                        |                                            |              |      |               |
| Logic High                              | $V_{CC} = \text{Max.}$                     | 3.0          |      | V             |
| Logic High                              | $V_{CC} = 5\text{V} \pm 5\%$               | 2.2          |      | V             |
| Logic Low                               |                                            | -0.3         | 0.6  | V             |
| Input Levels High Trip Option           |                                            |              |      |               |
| Logic High                              |                                            | 3.6          |      | V             |
| Logic Low                               |                                            | -0.3         | 1.2  | V             |
| Input Load Source Current               | $V_{CC} = 5\text{V}$                       |              |      |               |
| CKO                                     |                                            | -4           | -800 | $\mu\text{A}$ |
| All Others                              |                                            | -100         | -800 | $\mu\text{A}$ |
| Input Capacitance                       |                                            |              | 7    | pF            |
| Hi-Z Input Leakage                      |                                            | -2           | +2   | $\mu\text{A}$ |
| Output Voltage Levels                   |                                            |              |      |               |
| Standard Outputs                        |                                            |              |      |               |
| TTL Operation                           | $V_{CC} = 5\text{V} \pm 10\%$              |              |      |               |
| Logic High                              | $I_{OH} = -75 \mu\text{A}$                 | 2.4          |      | V             |
| Logic Low                               | $I_{OL} = 1.6 \text{ mA}$                  | -0.3         | 0.4  | V             |
| CMOS Operation (Note 1)                 |                                            |              |      |               |
| Logic High                              | $I_{OH} = -10 \mu\text{A}$                 | $V_{CC} - 1$ |      | V             |
| Logic Low                               | $I_{OL} = +10 \mu\text{A}$                 | -0.3         | 0.2  | V             |
| Output Current Levels                   |                                            |              |      |               |
| LED Direct Drive Output                 | $V_{CC} = 5\text{V}$ (Note 4)              |              |      |               |
| Logic High                              | $V_{OH} = 2.0\text{V}$                     | 1.0          | 12   | mA            |
| CKI Sink Current (R/C Option)           | $V_{IN} = 3.5\text{V}$                     | 2            |      | mA            |
| CKO (RAM Supply Current)                | $V_R = 3.3\text{V}$                        |              | 4    | mA            |
| TRI-STATE or Open Drain Leakage Current |                                            | -5           | +5   | $\mu\text{A}$ |
| Allowable Sink Current                  |                                            |              |      |               |
| Per Pin (L, D, G)                       |                                            |              | 10   | mA            |
| Per Pin (All Others)                    |                                            |              | 2    | mA            |
| Per Port (L)                            |                                            |              | 16   | mA            |
| Per Port (D, G)                         |                                            |              | 10   | mA            |
| Allowable Source Current                |                                            |              |      |               |
| Per Pin (L)                             |                                            |              | -15  | mA            |
| Per Pin (All Others)                    |                                            |              | -1.5 | mA            |

Note 1: TRI-STATE and LED configurations are excluded.

Note 2: SO output "0" level must be less than 0.6V for normal operation.

## AC Electrical Characteristics

COP420/COP421/COP422  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 6.3\text{V}$  unless otherwise noted

COP320/COP321/COP322  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$  unless otherwise noted

| Parameter                       | Conditions                                                                                           | Min | Max  | Units         |
|---------------------------------|------------------------------------------------------------------------------------------------------|-----|------|---------------|
| Instruction Cycle Time          |                                                                                                      | 4   | 10   | $\mu\text{s}$ |
| Operating CKI Frequency         | $\div 16$ mode                                                                                       | 1.6 | 4.0  | MHz           |
|                                 | $\div 8$ mode                                                                                        | 0.8 | 2.0  | MHz           |
| CKI Duty Cycle (Note 1)         |                                                                                                      | 40  | 60   | %             |
| Rise Time                       | Freq. = 4 MHz                                                                                        |     | 60   | ns            |
| Fall Time                       | Freq. = 4 MHz                                                                                        |     | 40   | ns            |
| CKI Using RC (Figure 8c)        | $\div 4$ mode                                                                                        |     |      |               |
| Frequency                       | $R = 15\text{ k}\Omega \pm 5\%$ , $C = 100\text{ pF}$                                                | 0.5 | 1.0  | MHz           |
| Instruction Cycle Time (Note 5) |                                                                                                      | 4   | 8    | $\mu\text{s}$ |
| CKO as SYNC Input (Figure 8d)   |                                                                                                      |     |      |               |
| $t_{\text{SYNC}}$               | Figure 3a                                                                                            | 50  |      | ns            |
| Inputs:                         |                                                                                                      |     |      |               |
| SI                              |                                                                                                      |     |      |               |
| $t_{\text{SETUP}}$              |                                                                                                      | 0.3 |      | $\mu\text{s}$ |
| $t_{\text{HOLD}}$               |                                                                                                      | 250 |      | ns            |
| All Other Inputs                |                                                                                                      |     |      |               |
| $t_{\text{SETUP}}$              |                                                                                                      | 1.7 |      | $\mu\text{s}$ |
| $t_{\text{HOLD}}$               |                                                                                                      | 300 |      | ns            |
| Output Propagation Delay        | Test Conditions:<br>$R_L = 5\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , $V_{\text{OUT}} = 1.5\text{V}$ | 300 |      | ns            |
| SO and SK                       |                                                                                                      |     |      |               |
| $t_{\text{pd1}}$                |                                                                                                      |     | 1.0  | $\mu\text{s}$ |
| $t_{\text{pd0}}$                |                                                                                                      |     | 1.0  | $\mu\text{s}$ |
| CKO                             |                                                                                                      |     |      |               |
| $t_{\text{pd1}}$                |                                                                                                      |     | 0.25 | $\mu\text{s}$ |
| $t_{\text{pd0}}$                |                                                                                                      |     | 0.25 | $\mu\text{s}$ |
| All Other Outputs               |                                                                                                      |     |      |               |
| $t_{\text{pd1}}$                |                                                                                                      |     | 1.4  | $\mu\text{s}$ |
| $t_{\text{pd0}}$                |                                                                                                      |     | 1.4  | $\mu\text{s}$ |

Note 1: Duty cycle =  $t_{W1}/(t_{W1} + t_{W0})$ .

Note 2: See Figure 9 for additional I/O characteristics.

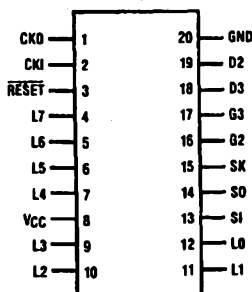
Note 3: Voltage change must be less than 0.5V in a 1 ms period.

Note 4: LED direct drive must not be used. Exercise great care not to exceed maximum device power dissipation limits when sourcing similar loads at high temperature.

Note 5: Variation due to the device included.

## Connection Diagrams

**COP422, COP322  
DIP**



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**Top View**

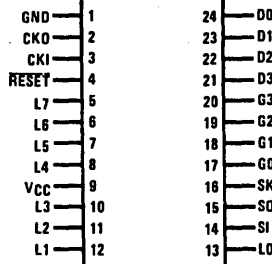
Order Number COP322-XXX/N  
or COP422-XXX/N

See NS Molded Package N20A

Order Number COP322-XXX/D  
or COP422-XXX/D

See NS Hermetic Package D20A

**COP421, COP321  
DIP and SO Wide**



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**Top View**

Order Number COP321-XXX/N  
or COP421-XXX/N

See NS Molded Package N24A

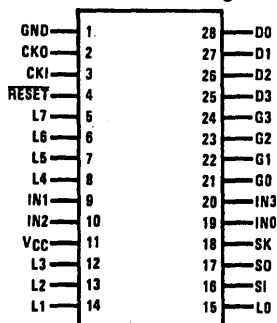
Order Number COP321-XXX/D  
or COP421-XXX/D

See NS Hermetic Package D24C

Order Number COP321-XXX/WM  
or COP421-XXX/WM

See NS Surface Mount Package M24B

**COP420, COP320  
Dual-In-Line Package**



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**Top View**

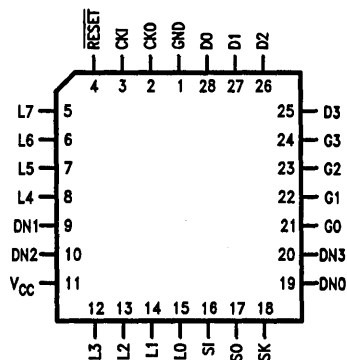
Order Number COP320-XXX/N  
or COP420-XXX/N

See NS Molded Package N28B

Order Number COP320-XXX/D  
or COP320-XXX/D

See NS Hermetic Package D28C

**28 PLCC**



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Order Number COP320-XXX/V  
or COP420-XXX/V

See NS PLCC Package V28A

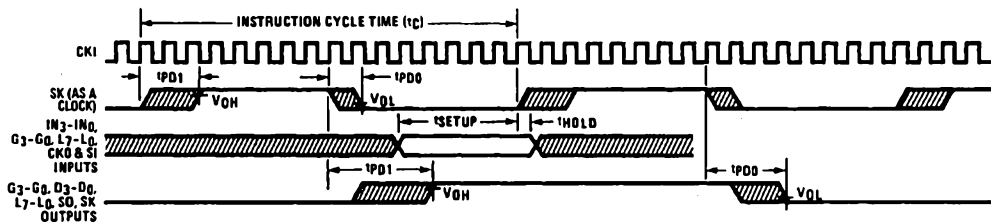
**FIGURE 2**

## Pin Descriptions

| Pin     | Description                                |
|---------|--------------------------------------------|
| L7-L0   | 8 bidirectional I/O ports with TRI-STATE   |
| G3-G0   | 4 bidirectional I/O ports                  |
| D3-D0   | 4 general purpose outputs                  |
| IN3-IN0 | 4 general purpose inputs (COP420/320 only) |
| SI      | Serial input (or counter input)            |
| SO      | Serial output (or general purpose output)  |

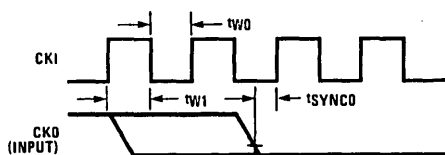
| Pin             | Description                                                             |
|-----------------|-------------------------------------------------------------------------|
| SK              | Logic-controlled clock (or general purpose output)                      |
| CKI             | System oscillator input                                                 |
| CKO             | System oscillator output (or general purpose input or RAM power supply) |
| RESET           | System reset input                                                      |
| V <sub>CC</sub> | Power supply                                                            |
| GND             | Ground                                                                  |

## Timing Diagrams



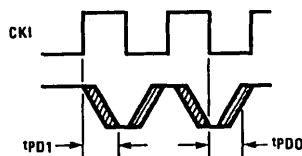
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FIGURE 3. Input/Output Timing Diagrams (Crystal Divide by 16 Mode)



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FIGURE 3A. Synchronization Timing



TL/DD/6921-7

FIGURE 3B. CKO Output Timing

## Functional Description COP420/COP421/COP422, COP320/COP321/COP322

For ease of reading this description, only COP420 and/or COP421 are referenced; however, all such references apply equally to the COP422, COP322, COP320 and/or COP321, respectively.

A block diagram of the COP420 is given in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2V). When a bit is reset, it is a logic "0" (less than 0.8V).

### PROGRAM MEMORY

Program Memory consists of a 1,024 byte ROM. As can be seen by an examination of the COP420/421 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 16 pages of 64 words each.

ROM addressing is accomplished by a 10-bit PC register. Its binary value selects one of the 1,024 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 10-bit binary count value. Three levels of subroutine nesting are implemented by the 10-bit subroutine save registers, SA, SB and SC, providing a last-in, first-out (LIFO) hardware subroutine stack.

ROM instruction words are fetched, decoded and executed by the Instruction Decode, Control and Skip Logic circuitry.

### DATA MEMORY

Data memory consists of 256-bit RAM, organized as 4 data registers of 16 4-bit digits. RAM addressing is implemented by a 6-bit **B register** whose upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the 6-bit contents of the operand field of these instructions. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

### INTERNAL LOGIC

The 4-bit **A register** (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load the input 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

## Functional Description COP420/COP421/COP422, COP320/COP321/COP322 (Continued)

A 4-bit **adder** performs the arithmetic and logic functions of the COP420/421, storing its results in A. It also outputs a carry bit to the 1-bit **C register**, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (See XAS instruction and EN register description, below.)

Four **general-purpose inputs**,  $IN_3$ – $IN_0$ , are provided;  $IN_1$ ,  $IN_2$  and  $IN_3$  may be selected, by a mask-programmable option, as Read Strobe, Chip Select and Write Strobe inputs, respectively, for use in MICROBUS applications.

The **D register** provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The **G register** contents are outputs to 4 general-purpose bidirectional I/O ports.  $G_0$  may be mask-programmed as an output for MICROBUS applications.

The **Q register** is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control. (See LEI instruction.)

The **8 L drivers**, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa–Sg and decimal point segments of the display.

The **SIO register** functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (See EN register description, below.) Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers. For example of additional parallel output capacity see **Application #2**.

The XAS instruction copies C into the **SKL latch**. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

The **EN register** is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register ( $EN_3$ – $EN_0$ ).

1. The least significant bit of the enable register,  $EN_0$  selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With  $EN_0$  set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0" occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of  $EN_3$ . With  $EN_0$  reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at DI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (See 4 below.) The SK output becomes a logic-controlled clock.

2. With the  $EN_1$  set the  $IN_1$  input is enabled as an interrupt input. Immediately following an interrupt,  $EN_1$  is reset to disable further interrupts.

3. With  $EN_2$  set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting  $EN_2$  disables the L drivers, placing the L I/O ports in a high impedance input state.

4.  $EN_3$ , in conjunction with  $EN_0$ , affects the SO output. With  $EN_0$  set (binary counter option selected) SO will output the value loaded into  $EN_3$ . With  $EN_0$  reset (serial shift register option selected), setting EN enables SO as the output of the SIO shift register outputting serial shifted data each instruction time. Resetting  $EN_3$  with the serial shift register option selected disables SO as the shift register output data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". The table below provides summary of the modes associated with  $EN_3$  and  $EN_1$ .

### OSCILLATOR

There are three basic clock oscillator configurations available as shown by *Figure 8*.

- Crystal Controlled Oscillator.** CKI and CKO are connected to an external crystal. The instruction cycle time equals the crystal frequency divided by 16 (optional by 8).
- External Oscillator.** CKI is an external clock input signal. The external frequency is divided by 16 (optional by 8) to give the instruction cycle time. CKO is now available to be used as the RAM power supply ( $V_R$ ) or as a general purpose input.
- RC Controlled Oscillator.** CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available for non-timing functions.

Enable Register Modes—Bits  $EN_3$  and  $EN_0$

| $EN_3$ | $EN_0$ | SIO            | SI                      | SO         | SK                                           |
|--------|--------|----------------|-------------------------|------------|----------------------------------------------|
| 0      | 0      | Shift Register | Input to Shift Register | 0          | If SKL = 1, SK = CLOCK<br>If SKL = 0, SK = 0 |
| 1      | 0      | Shift Register | Input to Shift Register | Serial Out | If SKL = 1, SK = CLOCK<br>If SKL = 0, SK = 0 |
| 0      | 1      | Binary Counter | Input to Binary Counter | 0          | If SKL = 1, SK = 1<br>If SKL = 0, SK = 0     |
| 1      | 1      | Binary Counter | Input to Binary Counter | 1          | If SKL = 1, SK = 1<br>If SKL = 0, SK = 0     |

# Functional Description COP420/COP421/COP422, COP320/COP321/COP322 (Continued)

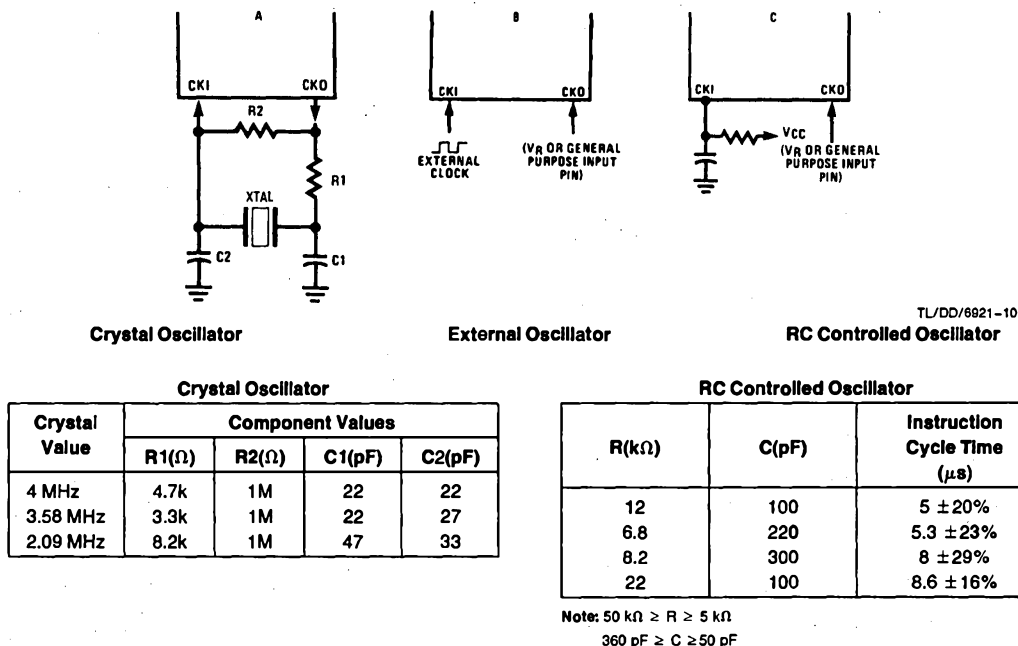


FIGURE 8. COP420/421/COP320/321 Oscillator

## CKO PIN OPTIONS

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. As an option CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction. As another option, CKO can be a RAM power supply pin ( $V_R$ ), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using either option is appropriate in applications where the COP420/421 system timing configuration does not require use of the CKO pin.

## RAM KEEP-ALIVE OPTION (NOT AVAILABLE ON COP422)

Selecting CKO as the RAM power supply ( $V_R$ ) allows the user to shut off the chip power supply ( $V_{CC}$ ) and maintain data in the RAM. To insure that RAM data integrity is maintained, the following conditions must be met:

1. RESET must go low before  $V_{CC}$  goes below spec during power off;  $V_{CC}$  must be within spec before RESET goes high on power up.
2.  $V_R$  must be within the operating range of the chip, and equal to  $V_{CC} \pm 1V$  during normal operation.
3.  $V_R$  must be ≥ 3.3V with  $V_{CC}$  off.

## INTERRUPT

The following features are associated with the  $IN_1$  interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

- a. The interrupt, once acknowledged as explained below, pushes the next sequential program counter address (PC

- + 1) onto the stack, pushing in turn the contents of the other subroutine-save registers to the next lower level (PC + 1 → SA → SB → SC). Any previous contents of SC are lost. The program counter is set to hex address 0FF (the last word of page 3) and  $EN_1$  is reset.
- b. An interrupt will be acknowledged only after the following conditions are met:
  1.  $EN_1$  has been set.
  2. A low-going pulse ("1" to "0") at least two instruction cycles wide occurs on the  $IN_1$  input.
  3. A currently executing instruction has been completed.
  4. All successive transfer of control instructions and successive LBIs have been completed (e.g., if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed.
- c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the end of the interrupt routine, a RET instruction is executed to "pop" the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines and LQID instructions should not be nested within the interrupt service routine, since their

## Functional Description COP420/COP421/COP422, COP320/COP321/COP322 (Continued)

popping the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.

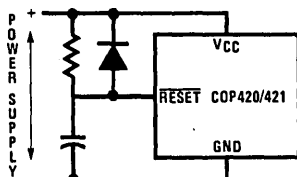
- d. The first instruction of the interrupt routine at hex address 0FF must be a NOP.
- e. A LEI instruction can be put immediately before the RET to re-enable interrupts.

### INITIALIZATION

The Reset Logic, internal to the COP420/421, will initialize (clear) the device upon power-up if the power supply rise time is less than 1 ms and greater than 1  $\mu$ s. If the power supply rise time is greater than 1 ms, the user must provide an external RC network and diode to the RESET pin as shown below. The RESET pin is configured as a Schmitt trigger input. If not used it should be connected to V<sub>CC</sub>.

Initialization will occur whenever a logic "0" is applied to the RESET input, provided it stays low for at least three instruction cycle times.

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization.* The first instruction at address 0 must be a CLRA.



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FIGURE 7. Power-Up Clear Circuit

### I/O OPTIONS

COP420/421 outputs have the following optional configurations, illustrated in Figure 9a:

- a. **Standard**—an enhancement mode device to ground in conjunction with a depletion-mode device to V<sub>CC</sub>, compatible with TTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.
- b. **Open-Drain**—an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.
- c. **Push-Pull**—An enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V<sub>CC</sub>. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.
- d. **Standard L**—same as a., but may be disabled. Available on L outputs only.
- e. **Open Drain L**—same as b., but may be disabled. Available on L outputs only.

## Functional Description COP420/COP421/COP422, COP320/COP321/COP322 (Continued)

**f. LED Direct Drive**—an enhancement-mode device to ground and to  $V_{CC}$ , meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (See Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display.

**g. TRI-STATE Push-Pull**—an enhancement-mode device to ground and  $V_{CC}$ . These outputs are TRI-STATE outputs, allowing for connection of these outputs to a data bus shared by other bus drivers.

COP420/COP421 inputs have the following optional configurations:

**h.** An on-chip depletion load device to  $V_{CC}$ .

**i.** A Hi-Z input which must be driven to a "1" or "0" by external components.

The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1–6, respectively). Minimum and maximum current ( $I_{OUT}$  and  $V_{OUT}$ ) curves are given in *Figure 9b* for each

of these devices to allow the designer to effectively use these I/O configurations in designing a COP420/421 system.

The SO, SK outputs can be configured as shown in *a.*, *b.*, or *c.* The D and G outputs can be configured as shown in *a.* or *b.* Note that when inputting data to the G ports, the G outputs should be set to "1." The L outputs can be configured as in *d.*, *e.*, *f.* or *g.*

An important point to remember if using configuration *d.* or *f.* with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current (see *Figure 9b*, device 2); however, when the L lines are used as input, the disabled depletion device can *not* be relied on to source sufficient current to pull an input to logic "1".

### COP421

If the COP420 is bonded as a 24-pin device, it becomes the COP421, illustrated in *Figure 2*, COP420/421 Connection Diagrams. Note that the COP421 does not contain the four general purpose IN inputs ( $IN_3$ – $IN_0$ ). Use of this option precludes, of course, use of the IN options and interrupt feature. All other options are available for the COP421.

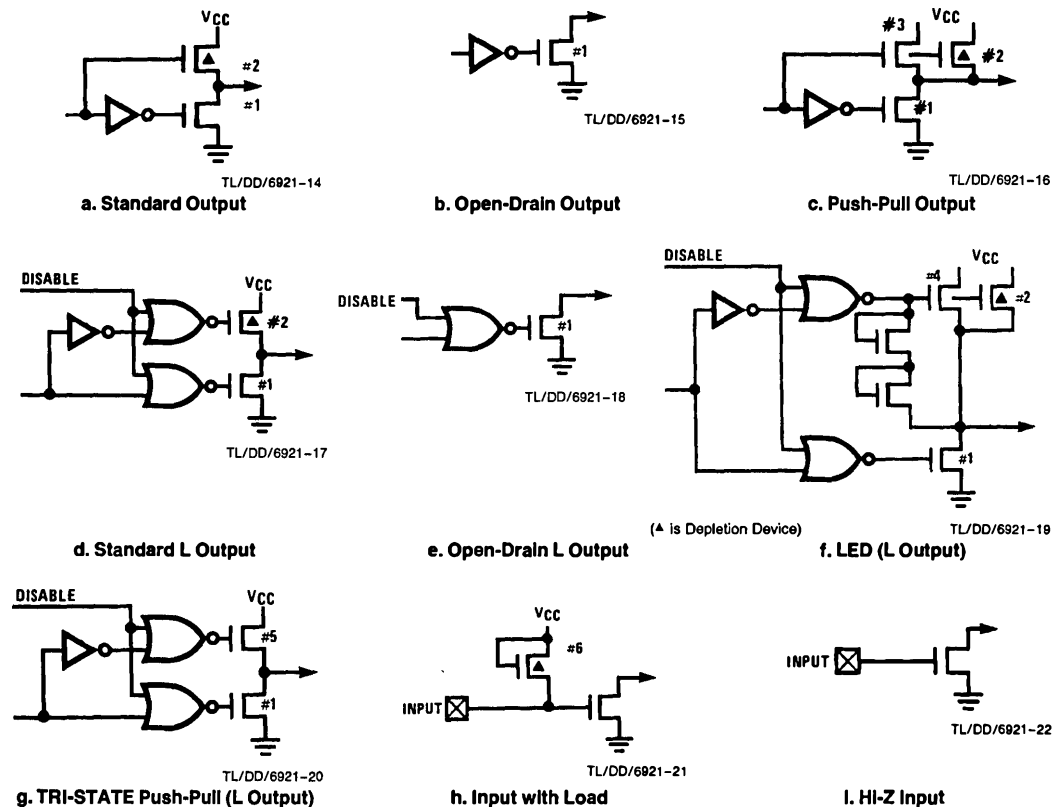


FIGURE 9a. Input/Output Configurations

## L-Bus Considerations

False states may be generated on L<sub>0</sub>–L<sub>7</sub> during the execution of the CAMQ instruction. The L-ports should not be used as clocks for edge sensitive devices such as flip-flops, counters, shift registers, etc. The following short program illustrates this situation.

START:

```
CLRA      ;ENABLE THE Q
LEI  4    ;REGISTER TO L LINES
LBI  TEST
STII  3
AISC  12
```

LOOP:

```
LBI  TEST ;LOAD Q WITH X'C3
CAMQ
JP   LOOP
```

In this program the internal Q register is enabled onto the L lines and a steady bit pattern of logic highs is output on L<sub>0</sub>, L<sub>1</sub>, L<sub>6</sub>, L<sub>7</sub>, and logic lows on L<sub>2</sub>–L<sub>5</sub> via the two-byte CAMQ instruction. Timing constraints on the device are such that the Q register may be temporarily loaded with the second byte of the CAMQ opcode (X'3C) prior to receiving the valid data pattern. If this occurs, the opcode will ripple onto the L lines and cause negative-going glitches on L<sub>0</sub>, L<sub>1</sub>, L<sub>6</sub>, L<sub>7</sub>, and positive glitches on L<sub>2</sub>–L<sub>5</sub>. Glitch durations are under 2 microseconds, although the exact value may vary due to data patterns, processing parameters, and L line loading. These false states are peculiar only to the CAMQ instruction and the L lines.

# Typical Performance Characteristics

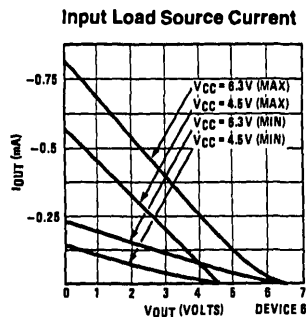
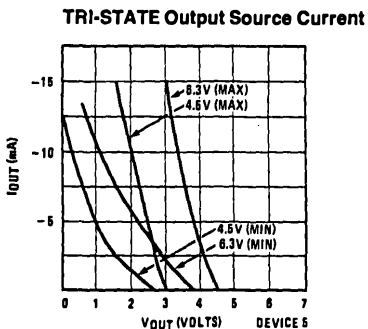
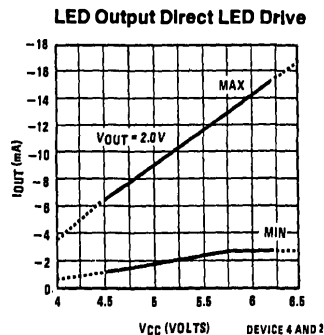
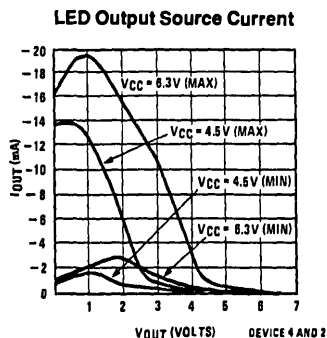
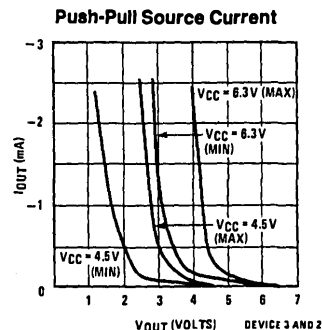
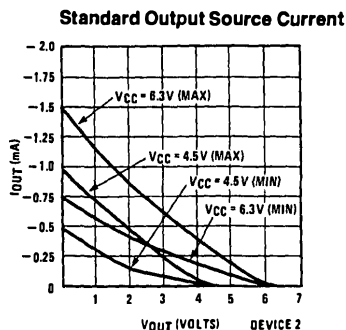
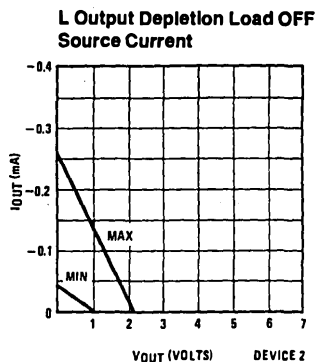
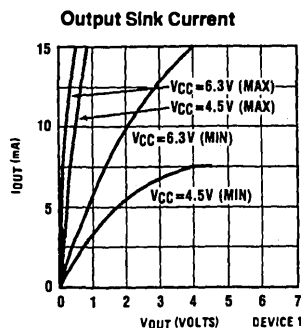


FIGURE 9b. COP420/COP421 Input/Output Characteristics

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## Typical Performance Characteristics (Continued)

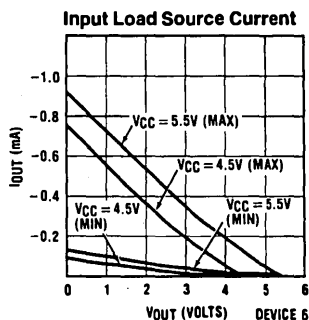
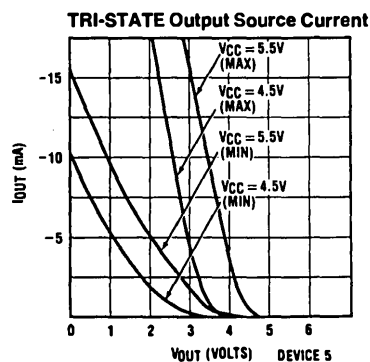
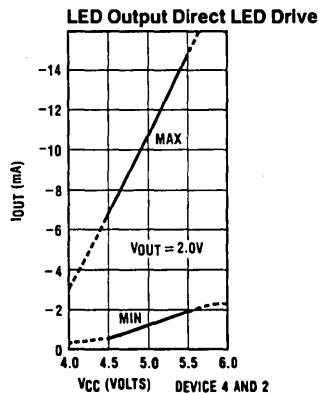
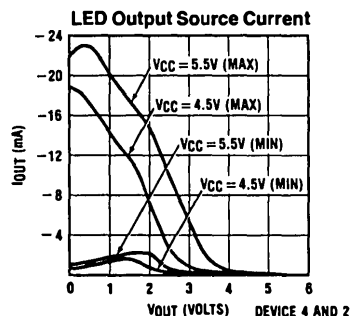
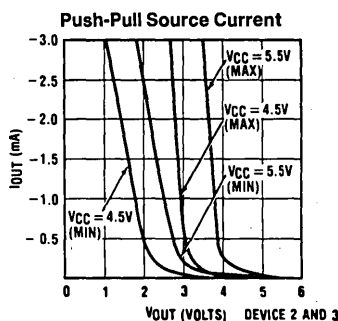
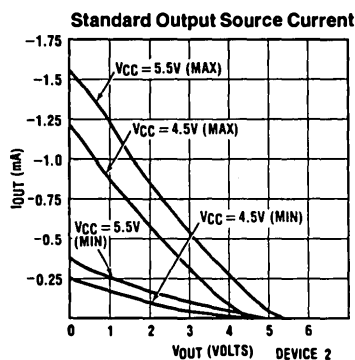
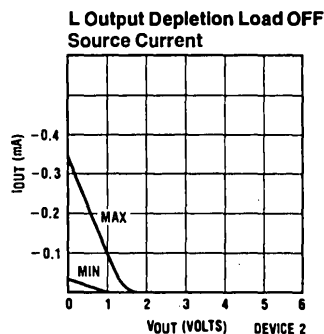
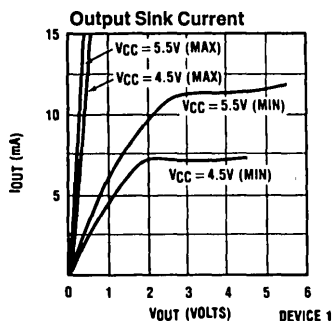


FIGURE 9c. COP320/COP321 Input/Output Characteristics

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## Instruction Set

Table I is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table II provides the mnemonic, operand, machine code, data flow, skip conditions and description associated with each instruction in the COP420/COP421/COP422 instruction set.

**TABLE I. COP420/421/422/320/321/322 Instruction Set Table Symbols**

| Symbol                               | Definition                                                                      | Symbol                                         | Definition                                            |
|--------------------------------------|---------------------------------------------------------------------------------|------------------------------------------------|-------------------------------------------------------|
| <b>INTERNAL ARCHITECTURE SYMBOLS</b> |                                                                                 | <b>INSTRUCTION OPERAND SYMBOLS</b>             |                                                       |
| A                                    | 4-bit Accumulator                                                               | d                                              | 4-bit Operand Field, 0-15 binary (RAM Digit Select)   |
| B                                    | 6-bit RAM Address Register                                                      | r                                              | 2-bit Operand Field, 0-3 binary (RAM Register Select) |
| Br                                   | Upper 2 bits of B (register address)                                            | a                                              | 10-bit Operand Field, 0-1023 binary (ROM Address)     |
| Bd                                   | Lower 4 bits of B (digit address)                                               | y                                              | 4-bit Operand Field, 0-15 binary (Immediate Data)     |
| C                                    | 1-bit Carry Register                                                            | RAM(s) Contents of RAM location addressed by s |                                                       |
| D                                    | 4-bit Data Output Port                                                          | ROM(t) Contents of ROM location addressed by t |                                                       |
| EN                                   | 4-bit Enable Register                                                           | <b>OPERATIONAL SYMBOLS</b>                     |                                                       |
| G                                    | 4-bit Register to latch data for G I/O Port                                     | +                                              | Plus                                                  |
| IL                                   | Two 1-bit latches associated with the IN <sub>3</sub> or IN <sub>0</sub> inputs | -                                              | Minus                                                 |
| IN                                   | 4-bit Input Port                                                                | →                                              | Replaces                                              |
| L                                    | 8-bit TRI-STATE I/O Port                                                        | ↔                                              | Is exchanged with                                     |
| M                                    | 4-bit contents of RAM Memory pointed to by B Register                           | =                                              | Is equal to                                           |
| PC                                   | 9-bit ROM Address Register (program counter)                                    | $\bar{A}$                                      | The one's complement of A                             |
| Q                                    | 8-bit Register to latch data for L I/O Port                                     | ⊕                                              | Exclusive-OR                                          |
| SA                                   | 10-bit Subroutine Save Register A                                               | :                                              | Range of values                                       |
| SB                                   | 10-bit Subroutine Save Register B                                               |                                                |                                                       |
| SC                                   | 10 Subroutine Save Register A                                                   |                                                |                                                       |
| SIO                                  | 4-bit Shift Register and Counter                                                |                                                |                                                       |
| SK                                   | Logic-Controlled Clock Output                                                   |                                                |                                                       |

**TABLE II. COP420/421/422/320/321/322 Instruction Set**

| Mnemonic                       | Operand | Hex Code | Machine Language Code (Binary) | Data Flow                                                                   | Skip Conditions | Description                                  |
|--------------------------------|---------|----------|--------------------------------|-----------------------------------------------------------------------------|-----------------|----------------------------------------------|
| <b>ARITHMETIC INSTRUCTIONS</b> |         |          |                                |                                                                             |                 |                                              |
| ASC                            |         | 30       | <u>0011</u> <u>0000</u>        | $A + C + \text{RAM}(B) \rightarrow A$<br>$\text{Carry} \rightarrow C$       | Carry           | Add with Carry, Skip on Carry                |
| ADD                            |         | 31       | <u>0011</u> <u>0001</u>        | $A + \text{RAM}(B) \rightarrow A$                                           | None            | Add RAM to A                                 |
| ADT                            |         | 4A       | <u>0100</u> <u>1010</u>        | $A + 10_{10} \rightarrow A$                                                 | None            | Add Ten to A                                 |
| AISC                           | y       | 5-       | <u>0101</u> <u>y</u>           | $A + y \rightarrow A$                                                       | Carry           | Add immediate, Skip on Carry ( $y \neq 0$ )  |
| CASC                           |         | 10       | <u>0001</u> <u>0000</u>        | $\bar{A} + \text{RAM}(B) + C \rightarrow A$<br>$\text{Carry} \rightarrow C$ | Carry           | Complement and Add with Carry, Skip on Carry |
| CLRA                           |         | 00       | <u>0000</u> <u>0000</u>        | $0 \rightarrow A$                                                           | None            | Clear A                                      |
| COMP                           |         | 40       | <u>0100</u> <u>0000</u>        | $\bar{A} \rightarrow A$                                                     | None            | One's complement of A to A                   |
| NOP                            |         | 44       | <u>0100</u> <u>0100</u>        | None                                                                        | None            | No Operation                                 |
| RC                             |         | 32       | <u>0011</u> <u>0010</u>        | "0" $\rightarrow C$                                                         | None            | Reset C                                      |
| SC                             |         | 22       | <u>0010</u> <u>0010</u>        | "1" $\rightarrow C$                                                         | None            | Set C                                        |
| XOR                            |         | 02       | <u>0000</u> <u>0010</u>        | $A \oplus \text{RAM}(B) \rightarrow A$                                      | None            | Exclusive-OR RAM with A                      |

## Instruction Set (Continued)

TABLE II. COP420/421/422/320/321/322 Instruction Set (Continued)

| Mnemonic                                | Operand | Hex Code | Machine Language Code (Binary)               | Data Flow                                                                 | Skip Conditions       | Description                                    |
|-----------------------------------------|---------|----------|----------------------------------------------|---------------------------------------------------------------------------|-----------------------|------------------------------------------------|
| <b>TRANSFER OF CONTROL INSTRUCTIONS</b> |         |          |                                              |                                                                           |                       |                                                |
| JID                                     |         | FF       | 1111 1111                                    | ROM (PC <sub>8</sub> , A, M) → PC <sub>7:0</sub>                          | None                  | Jump Indirect (Note 3)                         |
| JMP                                     | a       | 6 --     | 0110 00 a <sub>9</sub><br>a <sub>7:0</sub>   | a → PC                                                                    | None                  | Jump                                           |
| JP                                      | a       | --       | 1 a <sub>6:0</sub><br>(pages 2,3 only)       | a → PC <sub>6:0</sub>                                                     | None                  | Jump within Page (Note 4)                      |
|                                         |         | --       | 11 a <sub>5:0</sub><br>(all other pages)     | a → PC <sub>5:0</sub>                                                     |                       |                                                |
| JSRP                                    | a       | --       | 10 a <sub>5:0</sub>                          | PC + 1 → SA → SB → SC<br>010 → PC <sub>8:6</sub><br>a → PC <sub>5:0</sub> | None                  | Jump to Subroutine Page (Note 5)               |
| JSR                                     | a       | 6 --     | 0110 10 a <sub>9:8</sub><br>a <sub>7:0</sub> | PC + 1 → SA → SB → SC<br>a → PC                                           | None                  | Jump to Subroutine                             |
| RET                                     |         | 48       | 0100 1000                                    | SC → SB → SA → PC                                                         | None                  | Return from Subroutine                         |
| RETSK                                   |         | 49       | 0100 1001                                    | SC → SB → SA → PC                                                         | Always Skip on Return | Return from Subroutine then Skip               |
| <b>MEMORY REFERENCE INSTRUCTIONS</b>    |         |          |                                              |                                                                           |                       |                                                |
| CAMQ                                    |         | 33       | 0011 0011                                    | A → Q <sub>7:4</sub>                                                      | None                  | Copy A, RAM to Q                               |
|                                         |         | 3C       | 0011 1100                                    | RAM(B) → Q <sub>3:0</sub>                                                 |                       |                                                |
| CQMA                                    |         | 33       | 0011 0011                                    | Q <sub>7:4</sub> → RAM(B)                                                 | None                  | Copy Q to RAM, A                               |
|                                         |         | 2C       | 0010 1100                                    | Q <sub>3:0</sub> → A                                                      |                       |                                                |
| LD                                      | r       | -5       | 00 r 0101                                    | RAM(B) → A<br>Br ⊕ r → Br                                                 | None                  | Load RAM into A<br>Exclusive-OR Br with r      |
| LDD                                     | r,d     | 23       | 0010 0011                                    | RAM(r,d) → A                                                              | None                  | Load A with RAM pointed to directly by r,d     |
|                                         |         | --       | 00 r d                                       |                                                                           |                       |                                                |
| LQID                                    |         | BF       | 1011 1111                                    | ROM(PC <sub>9:8</sub> , A, M) → Q<br>SB → SC                              | None                  | Load Q Indirect (Note 3)                       |
| RMB                                     | 0       | 4C       | 0100 1100                                    | 0 → RAM(B) <sub>0</sub>                                                   | None                  | Reset RAM Bit                                  |
|                                         | 1       | 45       | 0100 0101                                    | 0 → RAM(B) <sub>1</sub>                                                   |                       |                                                |
|                                         | 2       | 42       | 0100 0010                                    | 0 → RAM(B) <sub>2</sub>                                                   |                       |                                                |
|                                         | 3       | 43       | 0100 0011                                    | 0 → RAM(B) <sub>3</sub>                                                   |                       |                                                |
| SMB                                     | 0       | 4D       | 0100 1101                                    | 1 → RAM(B) <sub>0</sub>                                                   | None                  | Set RAM Bit                                    |
|                                         | 1       | 47       | 0100 1101                                    | 1 → RAM(B) <sub>1</sub>                                                   |                       |                                                |
|                                         | 2       | 46       | 0100 0110                                    | 1 → RAM(B) <sub>2</sub>                                                   |                       |                                                |
|                                         | 3       | 4B       | 0100 1011                                    | 1 → RAM(B) <sub>3</sub>                                                   |                       |                                                |
| STII                                    | y       | 7 --     | 0111 y                                       | y → RAM(B)<br>Bd + 1 → Bd                                                 | None                  | Store Memory Immediate and Increment Bd        |
| X                                       | r       | -6       | 00 r 0110                                    | RAM(B) ↔ A<br>Br ⊕ r → Br                                                 | None                  | Exchange RAM with A,<br>Exclusive-OR Br with r |
| XAD                                     | r,d     | 23       | 0010 0011                                    | RAM(r,d) ↔ A                                                              | None                  | Exchange A with RAM pointed to directly by r,d |
|                                         |         | --       | 10 r d                                       |                                                                           |                       |                                                |

**Instruction Set** (Continued)**TABLE II. COP420/421/422/320/321/322 Instruction Set** (Continued)

| Mnemonic                                         | Operand | Hex Code | Machine Language Code (Binary)                                           | Data Flow                                                                               | Skip Conditions                                        | Description                                                  |
|--------------------------------------------------|---------|----------|--------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|--------------------------------------------------------|--------------------------------------------------------------|
| <b>MEMORY REFERENCE INSTRUCTIONS</b> (Continued) |         |          |                                                                          |                                                                                         |                                                        |                                                              |
| XDS                                              | r       | -7       | 00 r 0111                                                                | RAM(B) $\leftrightarrow$ A<br>Bd - 1 $\rightarrow$ Bd<br>Br $\oplus$ r $\rightarrow$ Br | Bd decrements past 0                                   | Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r |
| XIS                                              | r       | -4       | 00 r 0100                                                                | RAM(B) $\leftrightarrow$ A<br>Bd + 1 $\rightarrow$ Bd<br>Br $\oplus$ r $\rightarrow$ Br | Bd increments past 15                                  | Exchange RAM with A and Increment Bd, Exclusive-OR Br with r |
| <b>REGISTER REFERENCE INSTRUCTIONS</b>           |         |          |                                                                          |                                                                                         |                                                        |                                                              |
| CAB                                              |         | 50       | 0101 0000                                                                | A $\rightarrow$ Bd                                                                      | None                                                   | Copy A to Bd                                                 |
| CBA                                              |         | 4E       | 0100 1110                                                                | Bd $\rightarrow$ A                                                                      | None                                                   | Copy Bd to A                                                 |
| LBI                                              | r,d     | --       | 00 r (d-1)<br>(d = 0,9:15)<br>or<br>33 0011 0011<br>-- 10 r d<br>(any d) | r,d $\rightarrow$ B                                                                     | Skip until not a LBI                                   | Load B Immediate with r,d (Note 6)                           |
| LEI                                              | y       | 33<br>6- | 0011 0011<br>0010 y                                                      | y $\rightarrow$ EN                                                                      | None                                                   | Load EN Immediate (Note 7)                                   |
| XABR                                             |         | 12       | 0001 0010                                                                | A $\leftrightarrow$ Br (0,0 $\rightarrow$ A <sub>3</sub> ,A <sub>2</sub> )              | None                                                   | Exchange A with Br                                           |
| <b>TEST INSTRUCTIONS</b>                         |         |          |                                                                          |                                                                                         |                                                        |                                                              |
| SKC                                              |         | 20       | 0010 0000                                                                |                                                                                         | C = "1"                                                | Skip if C is True                                            |
| SKE                                              |         | 21       | 0010 0001                                                                |                                                                                         | A = RAM(B)                                             | Skip if A Equals RAM                                         |
| SKGZ                                             |         | 33<br>21 | 0011 0011<br>0010 0001                                                   |                                                                                         | G <sub>3:0</sub> = 0                                   | Skip if G is Zero (all 4 bits)                               |
| SKGBZ                                            |         | 33       | 0011 0011                                                                | 1st byte<br>2nd byte                                                                    |                                                        | Skip if G Bit is Zero                                        |
|                                                  | 0       | 01       | 0000 0001                                                                |                                                                                         | G <sub>0</sub> = 0                                     |                                                              |
|                                                  | 1       | 11       | 0001 0001                                                                |                                                                                         | G <sub>1</sub> = 0                                     |                                                              |
|                                                  | 2       | 03       | 0000 0011                                                                |                                                                                         | G <sub>2</sub> = 0                                     |                                                              |
|                                                  | 3       | 13       | 0010 0011                                                                |                                                                                         | G <sub>3</sub> = 0                                     |                                                              |
| SKMBZ                                            | 0       | 01       | 0000 0001                                                                |                                                                                         | RAM(B) <sub>0</sub> = 0                                | Skip if RAM Bit is Zero                                      |
|                                                  | 1       | 11       | 0001 0001                                                                |                                                                                         | RAM(B) <sub>1</sub> = 0                                |                                                              |
|                                                  | 2       | 03       | 0000 0011                                                                |                                                                                         | RAM(B) <sub>2</sub> = 0                                |                                                              |
|                                                  | 3       | 13       | 0001 0011                                                                |                                                                                         | RAM(B) <sub>3</sub> = 0                                |                                                              |
| SKT                                              |         | 41       | 0100 0001                                                                |                                                                                         | A time-base counter carry has occurred since last test | Skip on Timer (Note 3)                                       |

**Instruction Set** (Continued)

TABLE II. COP420/421/422/320/321/322 Instruction Set (Continued)

| Mnemonic                         | Operand | Hex Code  | Machine Language Code (Binary) | Data Flow                                               | Skip Conditions | Description                    |
|----------------------------------|---------|-----------|--------------------------------|---------------------------------------------------------|-----------------|--------------------------------|
| <b>INPUT/OUTPUT INSTRUCTIONS</b> |         |           |                                |                                                         |                 |                                |
| ING                              |         | 33<br>2A  | 0011 0011<br>0010 1010         | $G \rightarrow A$                                       | None            | Input G Ports to A             |
| ININ                             |         | 33<br>28  | 0011 0011<br>0010 1000         | $IN \rightarrow A$                                      | None            | Input IN Inputs to A (Note 2)  |
| INIL                             |         | 33<br>29  | 0011 0011<br>0010 1001         | $IL_3, CKO, "0", IL_0 \rightarrow A$                    | None            | Input IL Latches to A (Note 3) |
| INL                              |         | 33<br>2E  | 0011 0011<br>0010 1110         | $L_{7:4} \rightarrow RAM(B)$<br>$L_{3:0} \rightarrow A$ | None            | Input L Ports to RAM, A        |
| OBD                              |         | 33<br>3E  | 0011 0011<br>0011 1110         | $Bd \rightarrow D$                                      | None            | Output Bd to D Outputs         |
| OGI                              | y       | 33<br>5-- | 0011 0011<br>0101  y           | $y \rightarrow G$                                       | None            | Output to G Ports Immediate    |
| OMG                              |         | 33<br>3A  | 0011 0011<br>0011 1010         | $RAM(B) \rightarrow G$                                  | None            | Output RAM to G Ports          |
| XAS                              |         | 4F        | 0100 1111                      | $A \leftrightarrow SIO, C \rightarrow SKL$              | None            | Exchange A with SIO (Note 3)   |

**Note 1:** All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example,  $A_3$  indicates the most significant (left-most) bit of the 4-bit register.

**Note 2:** The ININ instruction is not available on the COP421/COP321 and COP422/COP322 since these devices do not contain the IN inputs.

**Note 3:** For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

**Note 4:** The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

**Note 5:** A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

**Note 6:** LBI is a single-byte instruction if  $d = 0, 8, 10, 11, 12, 13, 14$ , or 15. The machine code for the lower 4 bits equals the binary value of the "d" data minus 1, e.g., to load the lower four bits of B (Bd) with the value 9 (1001<sub>2</sub>), the lower 4 bits of the LBI instruction equal 8 (1000<sub>2</sub>). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111<sub>2</sub>).

**Note 7:** Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register.)

## Description of Selected Instructions

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing COP420/421 programs.

### XAS INSTRUCTION

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (See Functional Description, EN Register, above.) If

SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

### JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 10-bit word,  $PC_{9:8}, A, M, PC_9$  and  $PC_8$  are not affected by this instruction.

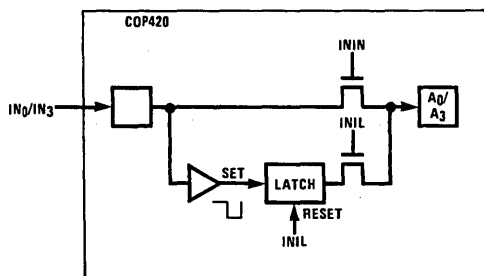
Note that JID requires 2 instruction cycles to execute.

## Description of Selected Instructions (Continued)

### INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches,  $IL_3$  and  $IL_0$  (see Figure 10) and CKO into A. The  $IL_3$  and  $IL_0$  latches are set if a low-going pulse ("1" to "0") has occurred on the  $IN_3$  and  $IN_0$  inputs since the last INIL instruction, provided the input pulse stays low for at least two instruction times. Execution of an INIL inputs  $IL_3$  and  $IL_0$  into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the  $IN_3$  and  $IN_0$  lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A "0" is always placed in A1 upon the execution of an INIL. The general purpose inputs  $IN_3$ – $IN_0$  are input to A upon execution of an ININ instruction. (See Table II, ININ instruction.) INIL is useful in recognizing pulses of short duration or pulses which occur too often to be read conveniently by an ININ instruction.

Note: IL latches are not cleared on reset.



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FIGURE 10

### LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 10-bit word  $PC_9$ ,  $PC_8$ , A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack ( $PC + 1 \rightarrow SA \rightarrow SB \rightarrow SC$ ) and replaces the least significant 8 bits of PC as follows:  $A \rightarrow PC_{7:4}$ ,  $RAM(B) \rightarrow PC_{3:0}$ , leaving  $PC_9$  and  $PC_8$  unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" ( $SC \rightarrow SB \rightarrow SA \rightarrow PC$ ), restoring the saved value of PC to continue sequential program execu-

tion. Since LQID pushes  $SB \rightarrow SC$ , the previous contents of SC are lost. Also, when LQID pops the stack, the previously pushed contents of SB are left in SC. The net result is that the content of SB are placed in SC ( $SB \rightarrow SC$ ). Note that LQID takes two instruction cycle times to execute.

### SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of an internal 10-bit time-base counter. This counter divides the instruction cycle clock frequency by 1024 and provides a latched indication of counter overflow. The SKT instruction tests this latch, executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction, therefore, allow the COP420/421 to generate its own time-base for real-time processing rather than relying on an external input signal.

For example, using a 2.097 MHz crystal as the time-base to the clock generator, the instruction cycle clock frequency will be 131 kHz (crystal frequency  $\div$  16) and the binary counter output pulse frequency will be 128 Hz. For time-of-day or similar real-time processing, the SKT instruction can call a routine which increments a "seconds" counter every 128 ticks.

### INSTRUCTION SET NOTES

- The first word of a COP420/421 program (ROM address 0) must be a CLRA (Clear A) instruction.
- Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths take the same number of cycle times whether instructions are skipped or executed except JID and LQID. LQID and JID take two cycle times if executed and one if skipped.
- The ROM is organized into 16 pages of 64 words each. The Program Counter is a 10-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3, 7, 11 or 15 will access data in the next group of four pages.

## Option List

The COP420/421/422 mask-programmable options are assigned numbers which correspond with the COP420 pins.

The following is a list of COP420 options. When specifying a COP421 or COP422 chip, Options 9, 10, 19, 20 and 29 must all be set to zero. When specifying a COP422 chip, Options 21, 22, 27 and 28 must also be zero, and Option 2 must not be a 1. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0: Ground—no options available

Option 2: CKO Pin

= 0: clock generator output to crystal

0 not available if option 3 = 4 or 5)

= 1: Pin is RAM power supply ( $V_R$ ) input  
(Not available on COP422/COP322)

= 2: general purpose input with load device

= 4: general purpose Hi Z input

Option 3: CKI Input

= 0: crystal input divided by 16

= 1: crystal input divided by 8

= 2: TTL external clock input divided by 16

= 3: TTL external clock input divided by 8

= 4: single-pin RC controlled oscillator ( $\div 4$ )

= 5: Schmitt trigger clock input ( $\div 4$ )

Option 4: RESET Pin

= 0: load devices to  $V_{CC}$

= 1: Hi-Z input

Option 5: L<sub>7</sub> Driver

= 0: Standard output (*Figure 9D*)

= 1: Open-Drain output (E)

= 2: LED direct drive output (F)

= 3: TRI-STATE push-pull output (G)

Option 6: L<sub>6</sub> Driver

same as Option 5

Option 7: L<sub>5</sub> Driver

same as Option 5

Option 8: L<sub>4</sub> Driver

same as Option 5

Option 9: IN<sub>1</sub> Input

= 0: load devices to  $V_{CC}$  (H)

= 1: Hi-Z input (I)

Option 10: IN<sub>2</sub> Input

same as Option 9

Option 11 = 0:  $V_{CC}$  Pin—no options available

Option 12: L<sub>3</sub> Driver

same as Option 5

Option 13: L<sub>2</sub> Driver

same as Option 5

Option 14: L<sub>1</sub> Driver

same as Option 5

Option 15: L<sub>0</sub> Driver

same as Option 5

Option 16: SI Input

same as Option 9

Option 17: SO Driver

= 0: standard output (A)

= 1: open-drain output (B)

= 2: push-pull output (C)

Option 18: SK Driver

same as Option 17

Option 19: IN<sub>0</sub> Input

same as Option 9

Option 20: IN<sub>3</sub> Input

same as Option 9

Option 21: G<sub>0</sub> I/O Port

= 0: Standard output (A)

= 1: Open-Drain output (B)

Option 22: G<sub>1</sub> I/O Port

same as Option 21

Option 23: G<sub>2</sub> I/O Port

same as Option 21

Option 24: G<sub>3</sub> I/O Port

same as Option 21

Option 25: D<sub>3</sub> Output

= 0: Standard output (A)

= 1: Open-Drain output (B)

Option 26: D<sub>2</sub> Output

same as Option 25

Option 27: D<sub>1</sub> Output

same as Option 25

Option 28: D<sub>0</sub> Output

same as Option 25

Option 29: COP Function

= 0: normal operation

Option 30: COP Bonding

= 0: COP420 (28-pin device)

= 1: COP421 (24-pin device)

= 2: 28- and 24-pin device

= 3: COP422 (20-pin device)

= 4: 28- and 20-pin device

= 5: 24- and 20-pin device

= 6: 28-, 24- and 20-pin device

Option 31: In Input Levels

= 0: normal input levels

= 1: Higher voltage input levels  
("0" = 1.2V, "1" = 3.6V)

Option 32: G Input Levels

same as Option 31

Option 33: L Input Levels

same as Option 31

Option 34: CKO Input Levels

same as Option 31

Option 35: SI Input Levels

same as Option 31

## Option List (Continued)

### COP OPTION LIST

The following option information is to be sent to National along with the EPROM.

#### OPTION DATA

OPTION 1 VALUE = 0 IS: GROUND PIN  
 OPTION 2 VALUE = \_\_\_\_\_ IS: CKO PIN  
 OPTION 3 VALUE = \_\_\_\_\_ IS: CKI INPUT  
 OPTION 4 VALUE = \_\_\_\_\_ IS: RESET INPUT  
 OPTION 5 VALUE = \_\_\_\_\_ IS: L<sub>7</sub> DRIVER  
 OPTION 6 VALUE = \_\_\_\_\_ IS: L<sub>6</sub> DRIVER  
 OPTION 7 VALUE = \_\_\_\_\_ IS: L<sub>5</sub> DRIVER  
 OPTION 8 VALUE = \_\_\_\_\_ IS: L<sub>4</sub> DRIVER  
 OPTION 9 VALUE = \_\_\_\_\_ IS: IN<sub>1</sub> INPUT  
 OPTION 10 VALUE = \_\_\_\_\_ IS: IN<sub>2</sub> INPUT  
 OPTION 11 VALUE = \_\_\_\_\_ IS: VCC PIN  
 OPTION 12 VALUE = \_\_\_\_\_ IS: L<sub>3</sub> DRIVER  
 OPTION 13 VALUE = \_\_\_\_\_ IS: L<sub>2</sub> DRIVER  
 OPTION 14 VALUE = \_\_\_\_\_ IS: L<sub>1</sub> DRIVER  
 OPTION 15 VALUE = \_\_\_\_\_ IS: L<sub>0</sub> DRIVER  
 OPTION 16 VALUE = \_\_\_\_\_ IS: SI INPUT  
 OPTION 17 VALUE = \_\_\_\_\_ IS: SO DRIVER  
 OPTION 18 VALUE = \_\_\_\_\_ IS: SK DRIVER  
 OPTION 19 VALUE = \_\_\_\_\_ IS: IN<sub>0</sub> INPUT  
 OPTION 20 VALUE = \_\_\_\_\_ IS: IN<sub>3</sub> INPUT  
 OPTION 21 VALUE = \_\_\_\_\_ IS: G<sub>0</sub> I/O PORT  
 OPTION 22 VALUE = \_\_\_\_\_ IS: G<sub>1</sub> I/O PORT  
 OPTION 23 VALUE = \_\_\_\_\_ IS: G<sub>2</sub> I/O PORT  
 OPTION 24 VALUE = \_\_\_\_\_ IS: G<sub>3</sub> I/O PORT  
 OPTION 25 VALUE = \_\_\_\_\_ IS: D<sub>3</sub> OUTPUT  
 OPTION 26 VALUE = \_\_\_\_\_ IS: D<sub>2</sub> OUTPUT  
 OPTION 27 VALUE = \_\_\_\_\_ IS: D<sub>1</sub> OUTPUT  
 OPTION 28 VALUE = \_\_\_\_\_ IS: D<sub>0</sub> OUTPUT  
 OPTION 29 VALUE = 0 IS: COP FUNCTION  
 OPTION 30 VALUE = \_\_\_\_\_ IS: COP BONDING  
 OPTION 31 VALUE = \_\_\_\_\_ IS: IN INPUT LEVELS  
 OPTION 32 VALUE = \_\_\_\_\_ IS: G INPUT LEVELS  
 OPTION 33 VALUE = \_\_\_\_\_ IS: L INPUT LEVELS  
 OPTION 34 VALUE = \_\_\_\_\_ IS: CKO INPUT LEVELS  
 OPTION 35 VALUE = \_\_\_\_\_ IS: SI INPUT LEVELS

#### TEST MODE (Non-Standard Operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed COP420. With SO forced to logic "1", two test modes are provided, depending upon the value of SI:

- RAM and Internal Logic Test Mode (SI = 1)
- ROM Test Mode (SI = 0)

These special test modes should not be employed by the user; they are intended for manufacturing test only.

#### APPLICATION # 1: COP420 General Controller

Figure 8 shows an interconnect diagram for a COP420 used as a general controller. Operation of the system is as follows:

- The L<sub>7</sub>–L<sub>0</sub> outputs are configured as LED Direct Drive outputs, allowing direct connection to the segments of the display.

- The D<sub>3</sub>–D<sub>0</sub> outputs drive the digits of the multiplexed display directly and scan the columns of the 4 x 4 keyboard matrix.
- The IN<sub>3</sub>–IN<sub>0</sub> inputs are used to input the 4 rows of the keyboard matrix. Reading the IN lines in conjunction with the current value of the D outputs allows detection, debouncing, and decoding of any one of the 16 keyswitches.
- CKI is configured as a single-pin oscillator input allowing system timing to be controlled by a single-pin RC network. CKO is therefore available for use as a V<sub>R</sub> RAM power supply pin. RAM data integrity is thereby assured when the main power supply is shut down (see RAM Keep-Alive option description).
- SI is selected as the input to a binary counter input. With SIO used as a binary counter, SO and SK can be used as general purpose outputs.
- The 4 bidirectional G I/O ports (G<sub>3</sub>–G<sub>0</sub>) are available for use as required by the user's application.

#### APPLICATION # 2: MUSICAL ORGAN AND MUSIC BOX

**Play Mode:** Twenty-five musical keys and 25 LEDs are provided to denote F to F with half notes in between. All the keys and LEDs are directly detected and driven by the microprocessor. Depression of the key will give the corresponding musical note and light up the corresponding LED.

**Clear:** Memory is provided to store a played tune. Depression of the CLEAR key erases the memory and the microprocessor is ready to store new musical notes. A maximum of 28 notes can be stored where each note can be of one to eight musical beats. (Two bytes of memory are required to store one musical note. Any note longer than eight musical beats will require additional memory space for storage.)

**Playback:** Depression of this button will playback the tune stored in the memory since last "clear."

**Preprogrammed Tunes:** There are ten preprogrammed tunes (each has an average of 55 notes) masked in the chip. Any tune can be recalled by depressing the "Tune Button" followed by the corresponding "Sharp Key."

**Learn Mode:** This mode is for the player to learn the ten preprogrammed tunes. By pressing the "Learn Button" followed by the corresponding "Sharp Key," the LEDs will be lighted up one by one to indicate the notes of the selected tune. The LED will remain "on" until the player presses the correct musical key; the LED for the next note will then be lighted up.

**Pause:** In addition to the 25 musical keys, there is a special pause key. The depression of this key generates a blank note to the memory.

**Note:** In the Learn Mode when playing "Oh Susanna," the pause key must be used.

**Tempo:** This is a control input to the musical beat time oscillator for varying the speed of the musical tunes.

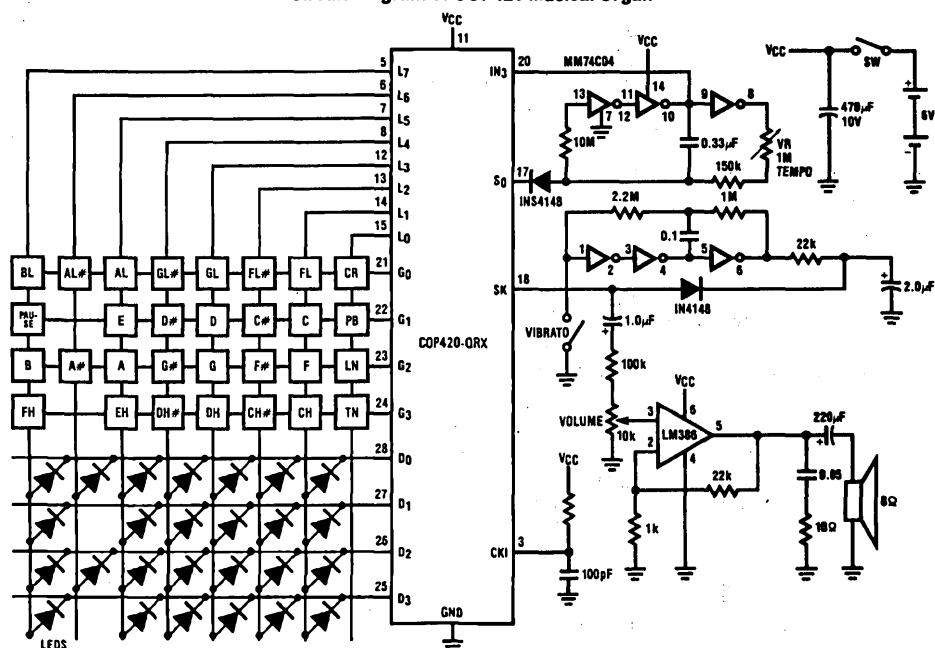
**Vibrato:** This is a switch control to vary the frequency vibration of the note.

**Tunes Listing:** The following is a listing of the ten preprogrammed tunes: 1) Jingle Bells, 2) Twinkle, Twinkle Little Star, 3) Happy Birthday, 4) Yankee Doodle, 5) Silent Night, 6) This Old Man, 7) London Bridge Is Falling Down, 8) Auld Lang Syne, 9) Oh Susanna, 10) Clementine.



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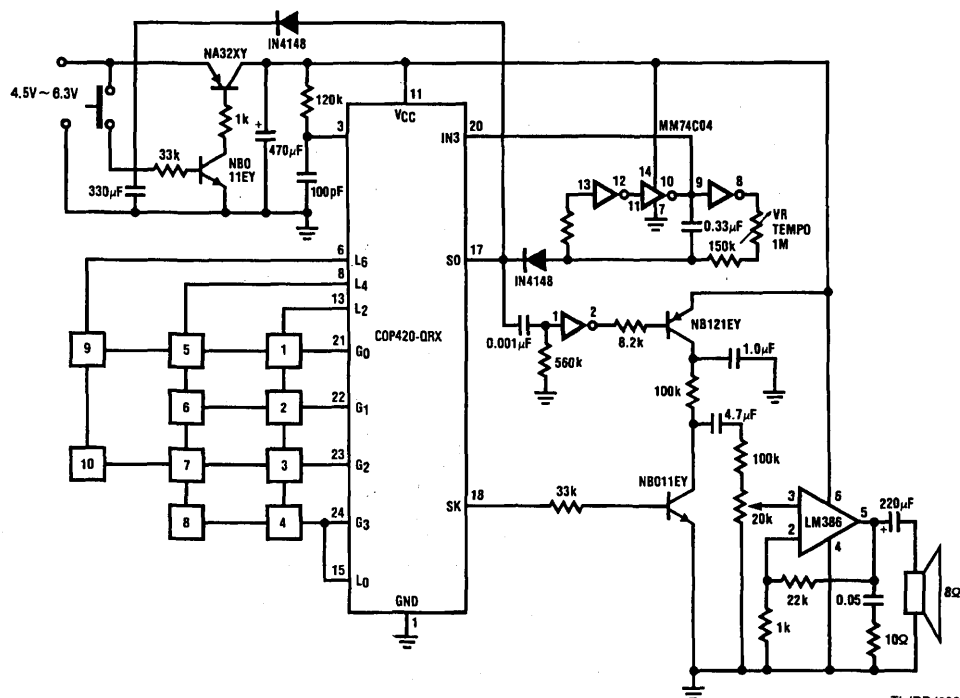
### Circuit Diagram of COP420 Musical Organ



TL/DD/8921-27

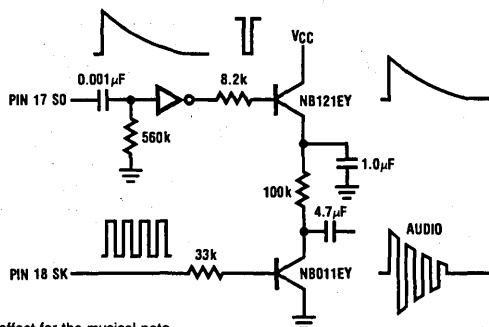
## Typical Applications (Continued)

### Music Box Application with Direct Key Access



TL/DD/6921-28

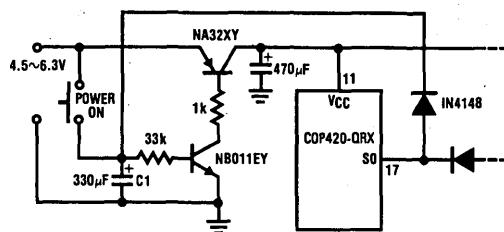
### Bell Sound Circuit



This additional circuit provides tinkling effect for the musical note.

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### Auto Power Shut-Off Circuit



TL/DD/6921-30

This circuit automatically turns off the musical organ if none of the keys are pressed within approximately 30 seconds.