



COP224C/COP225C/COP226C/COP244C/COP245C Single-Chip 1k and 2k CMOS Microcontrollers

General Description

The COP224C, COP225C, COP226C, COP244C and COP245C fully static, Single-Chip CMOS Microcontrollers are members of the COPSTM family, fabricated using double-poly, silicon gate microCMOS technology. These Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The COP224C and COP244C are 28 pin chips. The COP225C and COP245C are 24-pin versions (4 inputs removed) and COP226C is 20-pin version with 15 I/O lines. Standard test procedures and reliable high-density techniques provide the medium to large volume customers with a customized microcontroller at a low end-product cost. These microcontrollers are appropriate choices in many demanding control environments especially those with human interface.

Features

- Lowest power dissipation (600 μ W typical)
- Fully static (can turn off the clock)
- Power saving IDLE state and HALT mode
- 4.4 μ s instruction time
- 2k x 8 ROM, 128 x 4 RAM (COP244C/COP245C)
- 1k x 8 ROM, 64 x 4 RAM (COP224C/COP225C/COP226C)
- 23 I/O lines (COP244C and COP245C)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- Single supply operation (4.5V to 5.5V)
- Programmable read/write 8-bit timer/event counter
- Internal binary counter register with MICROWIRE™ serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS output compatible
- Software/hardware compatible with COP400 family
- Military temperature (-55°C to $+125^{\circ}\text{C}$) operation

Block Diagram

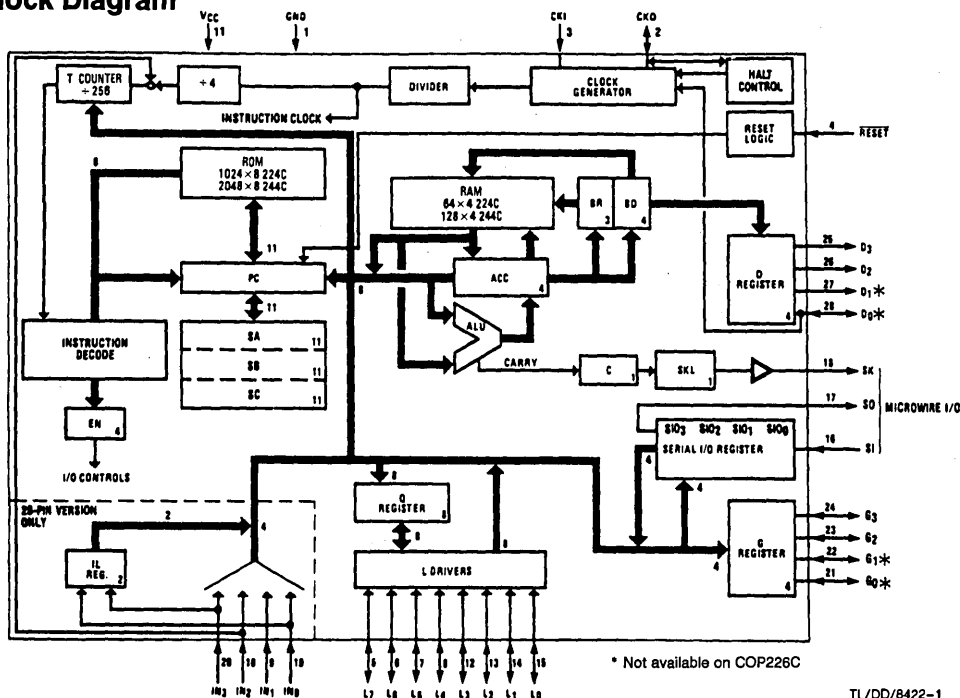


FIGURE 1

TL/DD/8422-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6V
Voltage at any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Total Allowable Source Current	25 mA
Total Allowable Sink Current	25 mA
Total Allowable Power Dissipation	150 mW

Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (soldering, 10 seconds)	300°C

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5V \leq V_{CC} \leq +5.5V$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage		4.5	5.5	V
Power Supply Ripple (Note 5)	Peak to Peak		$0.25 V_{CC}$	V
Supply Current (Note 1)	$V_{CC} = 5.0V$, $t_c = 4.4 \mu s$ (t_c is instruction cycle time)		5	mA
HALT Mode Current (Note 2)	$V_{CC} = 5.0V$, $F_{IN} = 0 \text{ kHz}$		200	μA
Input Voltage Levels RESET, CKI, D ₀ (clock input)				
Logic High		$0.9 V_{CC}$		V
Logic Low			$0.1 V_{CC}$	V
All Other Inputs				
Logic High		$0.7 V_{CC}$		V
Logic Low			$0.2 V_{CC}$	V
Hi-Z Input Leakage		-10	+10	μA
Input Capacitance (Note 4)			7	pF
Output Voltage Levels (except CKO) LSTTL Operation	Standard Outputs $V_{CC} = 5.0V \pm 10\%$			
Logic High	$I_{OH} = -100 \mu A$	2.7		V
Logic Low	$I_{OL} = 400 \mu A$		0.6	V
CMOS Operation				
Logic High	$I_{OH} = -10 \mu A$	$V_{CC} - 0.2$		V
Logic Low	$I_{OL} = 10 \mu A$		0.2	V
CKO Current Levels (As Clock Out)				
Sink $\left. \begin{array}{l} \div 4 \\ \div 8 \\ \div 16 \end{array} \right\}$	$CKI = V_{CC}$, $V_{OUT} = V_{CC}$	0.2 0.4 0.8		mA mA mA
Source $\left. \begin{array}{l} \div 4 \\ \div 8 \\ \div 16 \end{array} \right\}$	$CKI = 0V$, $V_{OUT} = 0V$	-0.2 -0.4 -0.8		mA mA mA
Allowable Sink/Source Current per Pin (Note 6)			5	mA
Allowable Loading on CKO (as HALT)			50	pF
Current Needed to Over-Ride HALT (Note 3)				
To Continue	$V_{IN} = 0.2 V_{CC}$		2.0	mA
To Halt	$V_{IN} = 0.7 V_{CC}$		3.0	mA
TRI-STATE or Open Drain Leakage Current		-10	+10	μA

AC Electrical Characteristics $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $+4.5\text{V} \leq V_{CC} \leq +5.5\text{V}$ unless otherwise specified.

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time (t_c)		4.4	DC	μs
Operating CKI $\div 4$ mode Frequency $\div 8$ mode $\div 16$ mode		DC DC DC	0.9 1.8 3.6	MHz MHz MHz
Duty Cycle (Note 4)	$f_1 = 3.6 \text{ MHz}$	40	60	%
Rise Time (Note 4)	$f_1 = 3.6 \text{ MHz}$ External Clock		60	ns
Fall Time (Note 4)	$f_1 = 3.6 \text{ MHz}$ External Clock		40	ns
Instruction Cycle Time RC Oscillator (Note 4)	$R = 30\text{k} \pm 5\%$ $C = 82 \text{ pF} \pm 5\%$ ($\div 4$ Mode)	6	18	μs
Inputs: (See Figure 3) (Note 4) t_{SETUP}	G Inputs SI Input All Others	$t_c/4 + 0.8$ 0.33 1.9		μs μs μs
t_{HOLD}		0.4		μs
Output Propagation Delay t_{PD1} , t_{PD0}	$V_{\text{OUT}} = 1.5\text{V}$, $C_L = 100 \text{ pF}$, $R_L = 5\text{k}$		1.4	μs

Note 1: Supply current is measured after running for 2000 cycle times with a square-wave clock on CKI, CKO open, and all other pins pulled up to V_{CC} with 5k resistors. See current drain equation on page 13.

Note 2: The HALT mode will stop CKI from oscillating in the RC and crystal configurations. Test conditions: all inputs tied to V_{CC} , L lines in TRI-STATE mode and tied to ground, all outputs low and tied to ground.

Note 3: When forcing HALT, current is only needed for a short time (approx. 200 ns) to flip the HALT flip-flop.

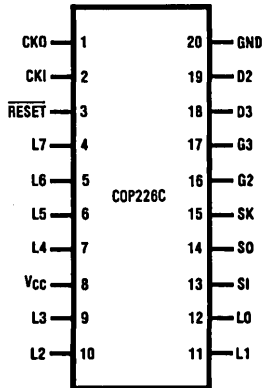
Note 4: This parameter is not tested but guaranteed by design. Variation due to the device included.

Note 5: Voltage change must be less than 0.25 volts in a 1 ms period.

Note 6: SO output sink current must be limited to keep V_{OL} less than 0.2 V_{CC} when part is running in order to prevent entering test mode.

Connection Diagrams

S.O. Wide and DIP



Top View

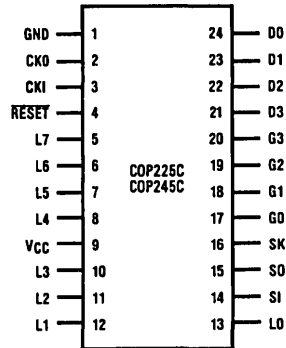
TL/DD/8422-2

Order Number COP226C-XXX/N
See NS Molded Package Number N20A

Order Number COP226C-XXX/D
See NS Hermetic Package Number D20A

Order Number COP226C-XXX/WM
See NS Surface Mount Package Number M20B

S.O. Wide and DIP



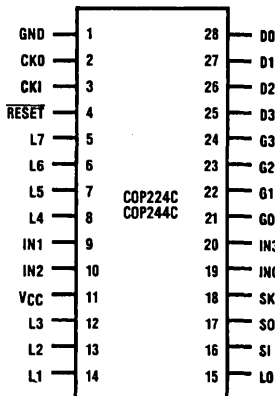
Top View

TL/DD/8422-3

Order Number COP225C-XXX/N
or COP245C-XXX/N
See NS Molded Package Number N24A

Order Number COP225C-XXX/D
or COP245C-XXX/D
See NS Hermetic Package Number D24C

DIP



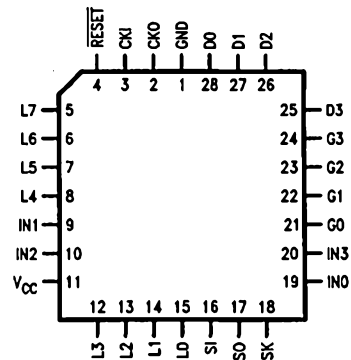
Top View

TL/DD/8422-4

Order Number COP224C-XXX/N
or COP244C-XXX/N
See NS Molded Package Number N28B

Order Number COP224C-XXX/D
or COP244C-XXX/D
See NS Hermetic Package Number D28C

28 PLCC



TL/DD/8422-13

Order Number COP224C-XXX/V
or COP244C-XXX/V
See NS PLCC Package Number V28A

FIGURE 2

Pin Descriptions

Pin	Description	Pin	Description
L7-L0	8-bit bidirectional port with TRI-STATE	SK	Logic controlled clock output
G3-G0	4-bit bidirectional I/O port	CKI	Chip oscillator input
D3-D0	4-bit output port	CKO	Oscillator output, HALT I/O port or general purpose input
IN3-IN0	4-bit input port (28 pin package only)	RESET	Reset input
SI	Serial Input or counter input	V _{CC}	Most positive power supply
SO	Serial or general purpose output	GND	Ground

Functional Description

The internal architecture is shown in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1", when a bit is reset, it is a logic "0".

Caution:

The output options available on the COP224C/225C/226C and COP244C/245C are not the same as those available on the COP324C/325C/326C, COP344C/345C, COP424C/425C/426C and COP444C/445C. Options not available on the COP224C/225C/226C and COP244C/245C are: Option 2 value 2; Option 4 value 0; Option 5 value 1; Option 9 value 0; Option 17 value 1; Option 30, Dual Clock, all values; Option 32, Microbus™, all values; Option 33 values 2, 4, and 6; Option 34 all values; and Option 35 all values.

PROGRAM MEMORY

Program Memory consists of ROM, 1024 bytes for the COP224C/225C/226C and 2048 bytes for the COP244C/245C. These bytes of ROM may be program instructions, constants or ROM addressing data.

ROM addressing is accomplished by an 11-bit PC register which selects one of the 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 11-bit binary count value.

Three levels of subroutine nesting are implemented by a three level deep stack. Each subroutine call or interrupt pushes the next PC address into the stack. Each return pops the stack back into the PC register.

DATA MEMORY

Data memory consists of a 512-bit RAM for the COP244C/245C, organized as 8 data registers of 16×4 -bit digits.

RAM addressing is implemented by a 7-bit B register whose upper 3 bits (Br) select 1 of 8 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. Data memory consists of a 256-bit RAM for the COP224C/225C/226C, organized as 4 data registers of 16×4 -bits digits. The B register is 6 bits long. Upper 2 bits (Br) select 1 of 4 data registers and lower 4 bits (Bd) select 1 of 16 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) are usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into or from the Q latches or T counter or loaded from the L ports. RAM addressing may also be performed directly by the LDD and XAD instructions based upon the immediate operand field of these instructions.

The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

INTERNAL LOGIC

The processor contains its own 4-bit A register (accumulator) which is the source and destination register for most I/O, arithmetic, logic, and data memory access operations. It can also be used to load the Br and Bd portions of the B register, to load and input 4 bits of the 8-bit Q latch or T counter, to input 4 bits of L I/O ports data, to input 4-bit G, or IN ports, and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions, storing the results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register in conjunction with the XAS instruction and the EN register, also serves to control the SK output.

The 8-bit T counter is a binary up counter which can be loaded to and from M and A using CAMT and CTMA instructions. This counter may be operated in two modes depending on a mask-programmable option: as a timer or as an external event counter. When the T counter overflows, an

Functional Description (Continued)

overflow flag will be set (see SKT and IT instructions below). The T counter is cleared on reset. A functional block diagram of the timer/counter is illustrated in Figure 7.

Four general-purpose inputs, IN3–IN0, are provided.

The D register provides 4 general-purpose outputs and is used as the destination register for the 4-bit contents of Bd.

The G register contents are outputs to a 4-bit general-purpose bidirectional I/O port.

The Q register is an internal, latched, 8-bit register, used to hold data loaded to or from M and A, as well as 8-bit data from ROM. Its contents are outputted to the L I/O ports when the L drivers are enabled under program control.

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O port. Also, the contents of L may be read directly into A and M.

The SIO register functions as a 4-bit serial-in/serial-out shift register for MICROWIRE I/O and COPS peripherals, or as a binary counter (depending on the contents of the EN register). Its contents can be exchanged with A.

The XAS instruction copies C into the SKL latch. In the counter mode, SK is the output of SKL; in the shift register mode, SK outputs SKL ANDed with the clock.

EN is an internal 4-bit register loaded by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register:

0. The least significant bit of the enable register, EN0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN0 set, SIO is an asynchronous binary counter, decrementing its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output equals the value of EN3. With EN0 reset, SIO is a serial shift register left shifting 1 bit each instruction cycle time. The data present at SI goes into the least significant bit of

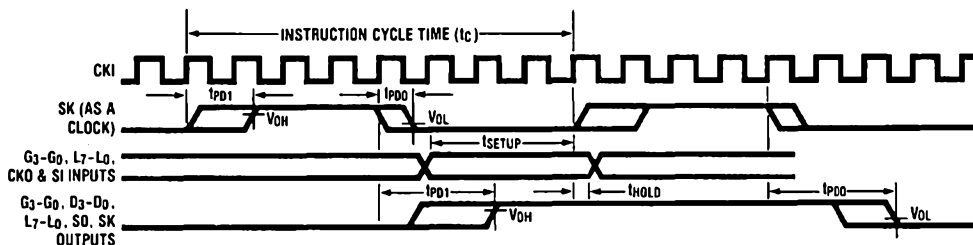
SIO. SO can be enabled to output the most significant bit of SIO each cycle time. The SK outputs SKL ANDed with the instruction cycle clock.

1. With EN1 set, interrupt is enabled. Immediately following an interrupt, EN1 is reset to disable further interrupts.
2. With EN2 set, the L drivers are enabled to output the data in Q to the L I/O port. Resetting EN2 disables the L drivers, placing the L I/O port in a high-impedance input state.
3. EN3, in conjunction with EN0, affects the SO output. With EN0 set (binary counter option selected) SO will output the value loaded into EN3. With EN0 reset (serial shift register option selected), setting EN3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN3 with the serial shift register option selected disables SO as the shift register output; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains set to "0".

INTERRUPT

The following features are associated with interrupt procedure and protocol and must be considered by the programmer when utilizing interrupts.

- a. The interrupt, once recognized as explained below, pushes the next sequential program counter address (PC+1) onto the stack. Any previous contents at the bottom of the stack are lost. The program counter is set to hex address 0FF (the last word of page 3) and EN1 is reset.
- b. An interrupt will be recognized only on the following conditions:
 1. EN1 has been set.
 2. A low-going pulse ("1" to "0") at least two instruction cycles wide has occurred on the IN₁ input.
 3. A currently executing instruction has been completed.



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FIGURE 3. Input/Output Timing Diagrams (divide by 8 mode)

TABLE I. Enable Register Modes — Bits EN0 and EN3

EN0	EN3	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Shift Register	Input to Shift Register	Serial out	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Binary Counter	Input to Counter	0	SK = SKL
1	1	Binary Counter	Input to Counter	1	SK = SKL

Functional Description (Continued)

4. All successive transfer of control instructions and successive LBIs have been completed (e.g. if the main program is executing a JP instruction which transfers program control to another JP instruction, the interrupt will not be acknowledged until the second JP instruction has been executed).
- c. Upon acknowledgement of an interrupt, the skip logic status is saved and later restored upon popping of the stack. For example, if an interrupt occurs during the execution of ASC (Add with Carry, Skip on Carry) instruction which results in carry, the skip logic status is saved and program control is transferred to the interrupt servicing routine at hex address 0FF. At the end of the interrupt routine, a RET instruction is executed to pop the stack and return program control to the instruction following the original ASC. At this time, the skip logic is enabled and skips this instruction because of the previous ASC carry. Subroutines should not be nested within the interrupt service routine, since their popping of the stack will enable any previously saved main program skips, interfering with the orderly execution of the interrupt routine.
- d. The instruction at hex address 0FF must be a NOP.
- e. An LEI instruction may be put immediately before the RET instruction to re-enable interrupts.

INITIALIZATION

The internal reset logic will initialize the device upon power-up if the power supply rise time is less than 1 ms and if the operating frequency at CKI is greater than 32 kHz, otherwise the external RC network shown in Figure 4 must be connected to the RESET pin (the conditions in Figure 4 must be met). The RESET pin is configured as a Schmitt trigger input. If not used, it should be connected to VCC. Initialization will occur whenever a logic "0" is applied to the RESET input, providing it stays low for at least three instruction cycle times.

Note: If CKI clock is less than 32 kHz, the internal reset logic (option #29 = 1) MUST be disabled and the external RC circuit must be used.

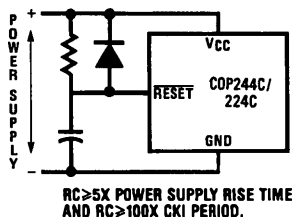


FIGURE 4. Power-Up Circuit

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, IL, T and G registers are cleared. The SKL latch is set, thus enabling SK as a clock output. Data Memory (RAM) is not cleared upon initialization. The first instruction at address 0 must be a CLRA (clear A register).

TIMER

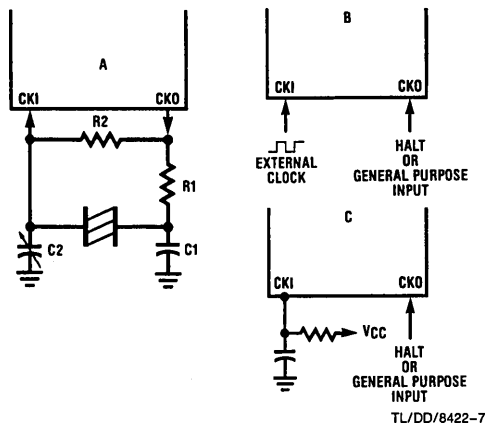
There are two modes selected by mask option:

- a. Time-base counter. In this mode, the instruction cycle frequency generated from CKI passes through a 2-bit divide-by-4 prescaler. The output of this prescaler increments the 8-bit T counter thus providing a 10-bit timer. The prescaler is cleared during execution of a CAMT instruction and on reset.

For example, using a 3.58 MHz crystal with a divide-by-16 option, the instruction cycle frequency of 223.70 kHz increments the 10-bit timer every 4.47 μ s. By presetting the counter and detecting overflow, accurate timeouts between 17.88 μ s (4 counts) and 4.577 ms (1024 counts) are possible. Longer timeouts can be achieved by accumulating, under software control, multiple overflows.

- b. External event counter. In this mode, a low-going pulse ("1" to "0") at least 2 instruction cycles wide on the IN2 input will increment the 8-bit T counter.

Note: The IT instruction is not allowed in this mode.



Crystal or Resonator

Crystal Value	Component Values			
	R1	R2	C1(pF)	C2(pF)
32 kHz	220k	20M	30	6-36
455 kHz	5k	10M	80	40
2.096 MHz	2k	1M	30	6-36
3.6 MHz	1k	1M	30	6-36

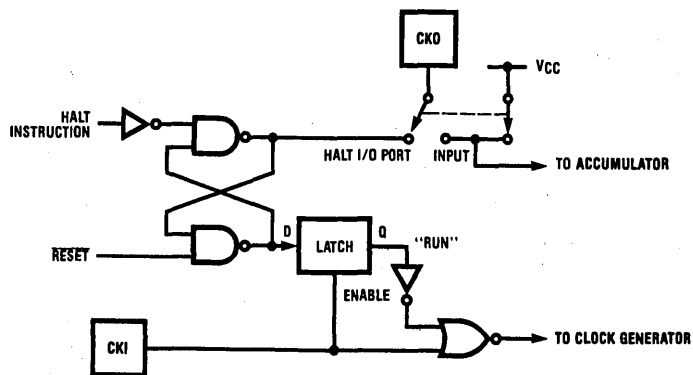
RC Controlled Oscillator

R	C	Cycle Time	VCC
30k	82 pF	6-18 μ s	≥ 4.5 V

Note: 15k $\leq$ R $\leq$ 150k
50 pF $\leq$ C $\leq$ 150 pF

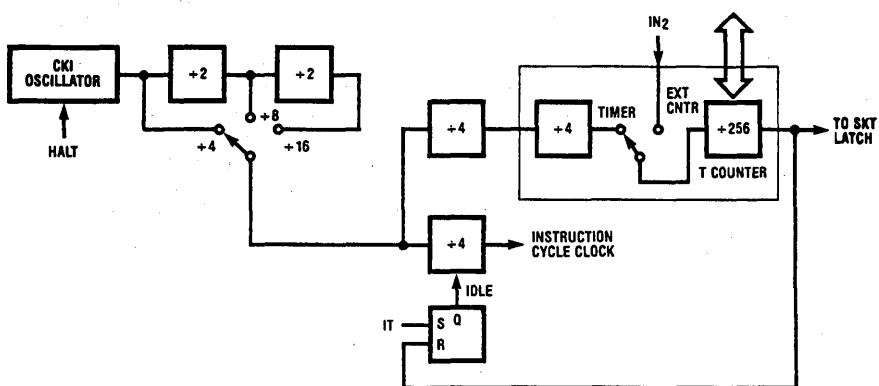
FIGURE 5. Oscillator Component Values

Block Diagrams (Continued)



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FIGURE 6b. Halt Mode—One-Pin Oscillator



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FIGURE 7. Clock and Timer

Instruction Set

Table II is a symbol table providing internal architecture, instruction operand and operation symbols used in the instruction set table.

TABLE II. Instruction Set Table Symbols

Symbol	Definition
Internal Architecture Symbols	
A	4-bit accumulator
B	7-bit RAM address register (6-bit for COP224C)
Br	Upper 3 bits of B (register address) (2-bit for COP224C)
Bd	Lower 4 bits of B (digit address)
C	1-bit carry register
D	4-bit data output port
EN	4-bit enable register
G	4-bit general purpose I/O port
IL	two 1-bit (IN0 and IN3) latches
IN	4-bit input port
L	8-bit TRI-STATE I/O port
M	4-bit contents of RAM addressed by B
PC	11-bit ROM address program counter
Q	8-bit latch for L port
SA,SB,SC	11-bit 3-level subroutine stack
SIO	4-bit shift register and counter
SK	Logic-controlled clock output
SKL	1-bit latch for SK output
T	8-bit timer

Instruction Operand Symbols

d	4-bit operand field, 0–15 binary (RAM digit select)
r	3(2)-bit operand field, 0–7(3) binary (RAM register select)
a	11-bit operand field, 0–2047 (1023)
y	4-bit operand field, 0–15 (immediate data)
RAM(x)	RAM addressed by variable x
ROM(x)	ROM addressed by variable x

Operational Symbols

+	Plus
–	Minus
→	Replaces
↔	Is exchanged with
=	Is equal to
$\bar{A}$	One's complement of A
⊕	Exclusive-or
:	Range of values

Table III provides the mnemonic, operand, machine code data flow, skip conditions and description of each instruction.

TABLE III. COP244C/245C Instruction Set

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
ARITHMETIC INSTRUCTIONS						
ASC		30	<u>0011</u> <u>0000</u>	$A + C + \text{RAM}(B) \rightarrow A$ $\text{Carry} \rightarrow C$	Carry	Add with Carry, Skip on Carry
ADD		31	<u>0011</u> <u>0001</u>	$A + \text{RAM}(B) \rightarrow A$	None	Add RAM to A
ADT		4A	<u>0100</u> <u>1010</u>	$A + 10_{10} \rightarrow A$	None	Add Ten to A
AISC	y	5–	<u>0101</u> <u>y</u>	$A + y \rightarrow A$	Carry	Add Immediate. Skip on Carry ($y \neq 0$)
CASC		10	<u>0001</u> <u>0000</u>	$\bar{A} + \text{RAM}(B) + C \rightarrow A$ $\text{Carry} \rightarrow C$	Carry	Complement and Add with Carry, Skip on Carry
CLRA		00	<u>0000</u> <u>0000</u>	$0 \rightarrow A$	None	Clear A
COMP		40	<u>0100</u> <u>0000</u>	$\bar{A} \rightarrow A$	None	Ones complement of A to A
NOP		44	<u>0100</u> <u>0100</u>	None	None	No Operation
RC		32	<u>0011</u> <u>0010</u>	"0" $\rightarrow C$	None	Reset C
SC		22	<u>0010</u> <u>0010</u>	"1" $\rightarrow C$	None	Set C
XOR		02	<u>0000</u> <u>0010</u>	$A \oplus \text{RAM}(B) \rightarrow A$	None	Exclusive-OR RAM with A

Instruction Set (Continued)

TABLE III. COP244C/245C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
TRANSFER CONTROL INSTRUCTIONS						
JID		FF	<u>1111</u> <u>1111</u>	ROM(PC _{10:8} A,M) → PC _{7:0}	None	Jump Indirect (Notes 1, 3)
JMP	a	6— —	<u>0110</u> <u>0</u> <u>a_{10:8}</u> <u>a_{7:0}</u>	a → PC	None	Jump
JP	a	— —	<u>1</u> <u>a_{6:0}</u> (pages 2, 3 only) or <u>11</u> <u>a_{5:0}</u> (all other pages)	a → PC _{6:0} a → PC _{5:0}	None	Jump within Page (Note 4)
JSRP	a	—	<u>10</u> <u>a_{5:0}</u>	PC + 1 → SA → SB → SC 00010 → PC _{10:6} a → PC _{5:0}	None	Jump to Subroutine Page (Note 5)
JSR	a	6— —	<u>0110</u> <u>1</u> <u>a_{10:8}</u> <u>a_{7:0}</u>	PC + 1 → SA → SB → SC a → PC	None	Jump to Subroutine
RET		48	<u>0100</u> <u>1000</u>	SC → SB → SA → PC	None	Return from Subroutine
RETSK		49	<u>0100</u> <u>1001</u>	SC → SB → SA → PC	Always Skip on Return	Return from Subroutine then Skip
HALT		33 38	<u>0011</u> <u>0011</u> <u>0011</u> <u>1000</u>		None	HALT Processor
IT		33 39	<u>0011</u> <u>0011</u> <u>0011</u> <u>1001</u>		None	IDLE till Timer Overflows then Continues
MEMORY REFERENCE INSTRUCTIONS						
CAMT		33 3F	<u>0011</u> <u>0011</u> <u>0011</u> <u>1111</u>	A → T _{7:4} RAM(B) → T _{3:0}	None	Copy A, RAM to T
CTMA		33 2F	<u>0011</u> <u>0011</u> <u>0010</u> <u>1111</u>	T _{7:4} → RAM(B) T _{3:0} → A	None	Copy T to RAM, A
CAMQ		33 3C	<u>0011</u> <u>0011</u> <u>0011</u> <u>1100</u>	A → Q _{7:4} RAM(B) → Q _{3:0}	None	Copy A, RAM to Q
CQMA		33 2C	<u>0011</u> <u>0011</u> <u>0010</u> <u>1100</u>	Q _{7:4} → RAM(B) Q _{3:0} → A	None	Copy Q to RAM, A
LD	r	—5	<u>00</u> <u>r</u> <u>0101</u> (r=0:3)	RAM(B) → A Br ⊕ r → Br	None	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	23 —	<u>0010</u> <u>0011</u> <u>0</u> <u>r</u> <u>d</u>	RAM(r,d) → A	None	Load A with RAM pointed to directly by r,d
LQID		BF	<u>1011</u> <u>1111</u>	ROM(PC _{10:8} A,M) → Q SB → SC	None	Load Q Indirect (Note 3)
RMB	0 1 2 3	4C 45 42 43	<u>0100</u> <u>1100</u> <u>0100</u> <u>0101</u> <u>0100</u> <u>0010</u> <u>0100</u> <u>0011</u>	0 → RAM(B) ₀ 0 → RAM(B) ₁ 0 → RAM(B) ₂ 0 → RAM(B) ₃	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	<u>0100</u> <u>1101</u> <u>0100</u> <u>0111</u> <u>0100</u> <u>0110</u> <u>0100</u> <u>1011</u>	1 → RAM(B) ₀ 1 → RAM(B) ₁ 1 → RAM(B) ₂ 1 → RAM(B) ₃	None	Set RAM Bit

Instruction Set (Continued)

TABLE III. COP244C/245C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description
MEMORY REFERENCE INSTRUCTIONS (Continued)						
STII	y	7—	0111 y	y → RAM(B) Bd + 1 → Bd	None	Store Memory Immediate 1 and Increment Bd
X	r	—6	00 r 0110 (r = 0:3)	RAM(B) ↔ A Br ⊕ r → Br	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	23 —	0010 0011 1 r d	RAM(r,d) ↔ A	None	Exchange A with RAM Pointed to Directly by r,d
XDS	r	—7	00 r 0111 (r = 0:3)	RAM(B) ↔ A Bd - 1 → Bd Br ⊕ r → Br	Bd decrements past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	—4	00 r 0100 (r = 0:3)	RAM(B) ↔ A Bd + 1 → Bd Br ⊕ r → Br	Bd increments past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS						
CAB		50	0101 0000	A → Bd	None	Copy A to Bd
CBA		4E	0100 1110	Bd → A	None	Copy Bd to A
LBI	r,d	— 33 —	00 r (d-1) (r = 0:3; d = 0,9:15) or 0011 0011 1 r d (any r, any d)	r,d → B	Skip until not a LBI	Load B Immediate with r,d (Note 6)
LEI	y	33 6—	0011 0011 0110 y	y → EN	None	Load EN Immediate (Note 7)
XABR		12	0001 0010	A ↔ Br	None	Exchange A with Br (Note 8)
TEST INSTRUCTIONS						
SKC		20	0010 0000		C = "1"	Skip if C is True
SKE		21	0010 0001		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	0011 0011 0010 0001		G _{3:0} = 0	Skip if G is Zero (all 4 bits)
SKGBZ		33	0011 0011	1st byte	G ₀ = 0	Skip if G Bit is Zero
	0	01	0000 0001	2nd byte	G ₁ = 0	
	1	11	0001 0001		G ₂ = 0	
	2	03	0000 0011		G ₃ = 0	
	3	13	0001 0011			
SKMBZ		01	0000 0001		RAM(B) ₀ = 0	Skip if RAM Bit is Zero
	1	11	0001 0001		RAM(B) ₁ = 0	
	2	03	0000 0011		RAM(B) ₂ = 0	
	3	13	0001 0011		RAM(B) ₃ = 0	
SKT		41	0100 0001		A time-base counter carry has occurred since last test	Skip on Timer (Note 3)

Instruction Set (Continued)

TABLE III. COP244C/245C Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Machine Language Code (Binary)	Data Flow	Skip Conditions	Description				
INPUT/OUTPUT INSTRUCTIONS										
ING		33 2A	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0010</td><td>1010</td></tr></table>	0011	0011	0010	1010	$G \rightarrow A$	None	Input G Ports to A
0011	0011									
0010	1010									
ININ		33 28	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0010</td><td>1000</td></tr></table>	0011	0011	0010	1000	$IN \rightarrow A$	None	Input IN Inputs to A (Note 2)
0011	0011									
0010	1000									
INIL		33 29	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0010</td><td>1001</td></tr></table>	0011	0011	0010	1001	$IL_3, CKO, "0", IL_0 \rightarrow A$	None	Input IL Latches to A (Note 3)
0011	0011									
0010	1001									
INL		33 2E	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0010</td><td>1110</td></tr></table>	0011	0011	0010	1110	$L_{7:4} \rightarrow RAM(B)$ $L_{3:0} \rightarrow A$	None	Input L Ports to RAM,A
0011	0011									
0010	1110									
OBD		33 3E	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0011</td><td>1110</td></tr></table>	0011	0011	0011	1110	$Bd \rightarrow D$	None	Output Bd to D Outputs
0011	0011									
0011	1110									
OGI	y	33 5—	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0101</td><td>y</td></tr></table>	0011	0011	0101	y	$y \rightarrow G$	None	Output to G Ports Immediate
0011	0011									
0101	y									
OMG		33 3A	<table><tr><td>0011</td><td>0011</td></tr><tr><td>0011</td><td>1010</td></tr></table>	0011	0011	0011	1010	$RAM(B) \rightarrow G$	None	Output RAM to G Ports
0011	0011									
0011	1010									
XAS		4F	<table><tr><td>0100</td><td>1111</td></tr></table>	0100	1111	$A \longleftrightarrow SIO, C \rightarrow SKL$	None	Exchange A with SIO (Note 3)		
0100	1111									

Note 1: All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.

Note 2: The ININ instruction is not available on the 24-pin packages since these devices do not contain the IN inputs.

Note 3: For additional information on the operation of the XAS, JID, LQID, INIL, and SKT instructions, see below.

Note 4: The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.

Note 5: A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.

Note 6: LBI is a single-byte instruction if $d = 0, 9, 10, 11, 12, 13, 14$, or 15. The machine code for the lower 4 bits equals the binary value of the "d" data *minus 1*, e.g., to load the lower four bits of B(Bd) with the value 9 (1001₂), the lower 4 bits of the LBI instruction equal 8 (1000₂). To load 0, the lower 4 bits of the LBI instruction should equal 15 (1111₂).

Note 7: Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (See Functional Description, EN Register.)

Note 8: For 2K ROM devices, $A \leftrightarrow Br$ ($0 \rightarrow A3$). For 1K ROM devices, $A \leftrightarrow Br$ ($0,0 \rightarrow A3, A2$).

Description of Selected Instructions

XAS INSTRUCTION

XAS (Exchange A with SIO) copies C to the SKL latch and exchanges the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. If SIO is selected as a shift register, an XAS instruction can be performed once every 4 instruction cycles to effect a continuous data stream.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 11-bit word PC10:PC8,A,M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC+1 → SA → SB → SC) and replaces the least significant 8 bits of the PC as follows: A → PC7:4, RAM(B) → PC3:0, leaving PC10, PC9 and PC8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SC → SB → SA → PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SB → SC, the previous contents of SC are lost.

Note: LQID uses 2 instruction cycles if executed, one if skipped.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the contents of ROM addressed by the 11-bit word, PC10:8,A,M. PC10,PC9 and PC8 are not affected by JID.

Note: JID uses 2 instruction cycles if executed, one if skipped.

SKT INSTRUCTION

The SKT (Skip On Timer) instruction tests the state of the T counter overflow latch (see internal logic, above), executing the next program instruction if the latch is not set. If the latch has been set since the previous test, the next program instruction is skipped and the latch is reset. The features associated with this instruction allow the processor to generate its own time-base for real-time processing, rather than relying on an external input signal.

Note: If the most significant bit of the T counter is a 1 when a CAMT instruction loads the counter, the overflow flag will be set. The following sample of codes should be used when loading the counter:

```
CAMT ; load T counter
SKT  ; skip if overflow flag is set and reset it
NOP
```

IT INSTRUCTION

The IT (idle till timer) instruction halts the processor and puts it in an idle state until the time-base counter overflows. This idle state reduces current drain since all logic (except the oscillator and time base counter) is stopped. IT instruction is not allowed if the T counter is mask-programmed as an external event counter (option #31 = 1).

INIL INSTRUCTION

INIL (Input IL Latches to A) inputs 2 latches, IL3 and IL0, CKO and 0 into A. The IL3 and IL0 latches are set if a low-going pulse ("1" to "0") has occurred on the IN3 and IN0 inputs since the last INIL instruction, provided the input

pulse stays low for at least two instruction cycles. Execution of an INIL inputs IL3 and IL0 into A3 and A0 respectively, and resets these latches to allow them to respond to subsequent low-going pulses on the IN3 and IN0 lines. If CKO is mask programmed as a general purpose input, an INIL will input the state of CKO into A2. If CKO has not been so programmed, a "1" will be placed in A2. A0 is input into A1. IL latches are cleared on reset. IL latches are not available on the COP245C/225C, and COP226C.

INSTRUCTION SET NOTES

- The first word of a program (ROM address 0) must be a CLRA (Clear A) instruction.
- Although skipped instructions are not executed, they are still fetched from the program memory. Thus program paths take the same number of cycles whether instructions are skipped or executed except for JID, and LQID.
- The ROM is organized into pages of 64 words each. The Program Counter is a 11-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID, or LQID is the last word of a page, it operates as if it were in the next page. For example: a JP located in the last word of a page will jump to a location in the next page. Also, a JID or LQID located in the last word of every fourth page (i.e. hex address 0FF, 1FF, 2FF, 3FF, 4FF, etc.) will access data in the next group of four pages.

Note: The COP224C/225C/226C needs only 10 bits to address its ROM. Therefore, the eleventh bit (P10) is ignored.

Power Dissipation

The lowest power drain is when the clock is stopped. As the frequency increases so does current. Current is also lower at lower operating voltages. Therefore, the user should run at the lowest speed and voltage that his application will allow. The user should take care that all pins swing to full supply levels to insure that outputs are not loaded down and that inputs are not at some intermediate level which may draw current. Any input with a slow rise or fall time will draw additional current. A crystal or resonator generated clock input will draw additional current. For example, a 500 kHz crystal input will typically draw 100 μ A more than a square-wave input. An R/C oscillator will draw even more current since the input is a slow rising signal.

If using an external squarewave oscillator, the following equation can be used to calculate operating current drain.

$$I_{CO} = I_Q + V \times 70 \times F_i + V \times 2400 \times F_i / D_v \quad \text{where:}$$

$$I_{CO} = \text{chip operating current drain in microamps}$$

$$I_Q = \text{quiescent leakage current (from curve)}$$

$$F_i = \text{CKI frequency in MegaHertz}$$

$$V = \text{chip } V_{CC} \text{ in volts}$$

$$D_v = \text{divide by option selected}$$

For example at 5 volts V_{CC} and 400 kHz (divide by 4)

$$I_{CO} = 120 + 5 \times 70 \times 0.4 + 5 \times 2400 \times 0.4 / 4$$

$$I_{CO} = 120 + 140 + 1200 = 1460 \mu A$$

Power Dissipation (Continued)

If an IT instruction is executed, the chip goes into the IDLE mode until the timer overflows. In IDLE mode, the current drain can be calculated from the following equation:

$$I_{ci} = I_Q + V \times 70 \times F_i$$

For example, at 5 volts V_{CC} and 400 kHz

$$I_{ci} = 120 + 5 \times 70 \times 0.4 = 260 \mu A$$

The total average current will then be the weighted average of the operating current and the idle current:

$$I_{ta} = I_{CO} \times \frac{T_o}{T_o + T_i} + I_{ci} \times \frac{T_i}{T_o + T_i}$$

where: I_{ta} = total average current

I_{CO} = operating current

I_{ci} = idle current

T_o = operating time

T_i = idle time

I/O OPTIONS

Outputs have the following optional configurations, illustrated in *Figure 8*:

- Standard — A CMOS push-pull buffer with an N-channel device to ground in conjunction with a P-channel device to V_{CC} , compatible with CMOS and LSTTL.
- Open Drain — An N-channel device to ground only, allowing external pull-up as required by the user's application.
- Standard TRI-STATE L Output — A CMOS output buffer similar to a. which may be disabled by program control.
- Open-Drain TRI-STATE L Output — This has the N-channel device to ground only.

All inputs have the following option:

- Hi-Z input which must be driven by the users logic.

All output drivers use two common devices numbered 1 to 2. Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in *Figure 9* for each of these devices to allow the designer to effectively use these I/O configurations.

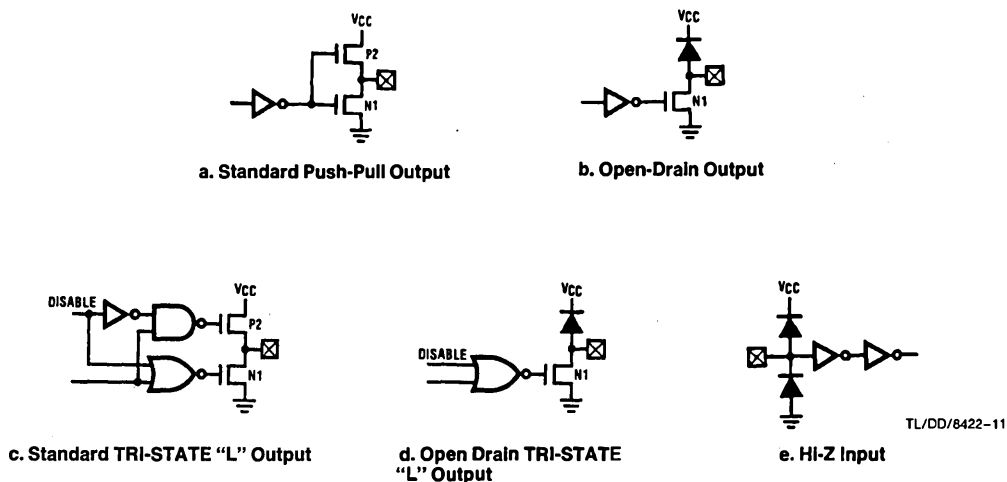
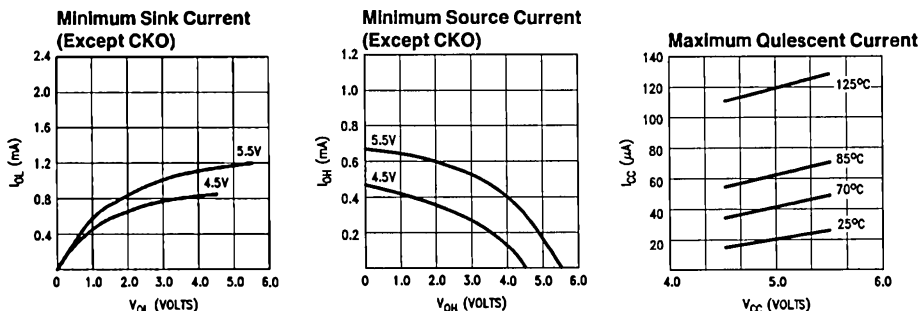


FIGURE 8. Input/Output Configurations

Power Dissipation (Continued)



TL/DD/8422-12

FIGURE 9. Input/Output Characteristics

Option List

The COP244C/245C/224C/225C/COP226C mask-programmable options are assigned numbers which correspond with the COP244C/224C pins.

The following is a list of options. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Caution:

The output options available on the COP224C/225C/226C and COP244C/245C are not the same as those available on the COP324C/325C/326C, COP344C/345C, COP424C/425C/426C and COP444C/445C. Options not available on the COP224C/225C/226C and COP244C/245C are: Option 2 value 2; Option 4 value 0; Option 5 value 1; Option 9 value 0; Option 17 value 1; Option 30, Dual Clock, all values; Option 32, Microbus, all values; Option 33 values 2, 4, and 6; Option 34 all values; and Option 35 all values.

PLEASE FILL OUT THE OPTION TABLE on the next page. Photocopy the option data and send it in with your disk or EPROM.

Option 1 = 0: Ground Pin — no options available

Option 2: CKO Pin

- = 0: clock generator output to crystal/resonator
- = 1: HALT I/O port
- = 3: general purpose input, high-Z

Option 3: CKI input

- = 0: Crystal controlled oscillator input divide by 4
- = 1: Crystal controlled oscillator input divide by 8
- = 2: Crystal controlled oscillator input divide by 16
- = 4: Single-pin RC controlled oscillator (divide by 4)
- = 5: External oscillator input divide by 4
- = 6: External oscillator input divide by 8
- = 7: External oscillator input divide by 16

Option 4: $\overline{\text{RESET}}$ input

- = 1: Hi-Z input

Option 5: L7 Driver

- = 0: Standard TRI-STATE push-pull output
- = 2: Open-drain TRI-STATE output

Option 6: L6 Driver — (same as option 5)

Option 7: L5 Driver — (same as option 5)

Option 8: L4 Driver — (same as option 5)

Option 9: IN1 input

- = 1: Hi-Z input, mandatory for 28 Pin Package
- = 2: Mandatory for 20 and 24 Pin Packages

Option 10: IN2 input — (same as option 9)

Option 11 = 0: V_{CC} Pin — no option available

Option 12: L3 Driver — (same as option 5)

Option 13: L2 Driver — (same as option 5)

Option 14: L1 Driver — (same as option 5)

Option 15: L0 Driver — (same as option 5)

Option 16: SI input — (same as option 4)

Option 17: SO Driver

- = 0: Standard push-pull output
- = 2: Open-drain output

Option 18: SK Driver — (same as option 17)

Option 19: IN0 Input — (same as option 9)

Option 20: IN3 Input — (same as option 9)

Option 21: G0 I/O Port — (same as option 17)

Option 22: G1 I/O Port — (same as option 17)

Option 23: G2 I/O Port — (same as option 17)

Option 24: G3 I/O Port — (same as option 17)

Option 25: D3 Output — (same as option 17)

Option 26: D2 Output — (same as option 17)

Option 27: D1 Output — (same as option 17)

Option List (Continued)

Option 28: D0 Output — (same as option 17)

Option 29: Internal Initialization Logic

= 0: Normal operation

= 1: No internal initialization logic

Option 30 = 0: No Option Available

Option 31: Timer

= 0: Time-base counter

= 1: External event counter

Option 32 = 0: No Option Available

Option 33: COP bonding. See note.

(1k and 2k Microcontroller)

= 0: 28-pin package

= 1: 24-pin package

(1k Microcontroller only)

= 3: 20-pin package

= 5: 24- and 20-pin package

Note:—If opt. #33=0 then opt. #9, 10, 19, and 20 must=1.

If opt. #33=1 then opt. #9, 10, 19 and 20 must=2, and option #31 must=0.

If opt. #33=3 or 5 then opt. #9, 10, 19, 20 must=2 and opt. #21, 22, 31 must=0.

Option 34 = 0: No Option Available

Option 35 = 0: No Option Available

Option Table

The following option information is to be sent to National along with the EPROM.

OPTION DATA		
OPTION 1	VALUE = <u>0</u>	IS: GROUND PIN
OPTION 2	VALUE = _____	IS: CKO PIN
OPTION 3	VALUE = _____	IS: CKI INPUT
OPTION 4	VALUE = <u>1</u>	IS: RESET INPUT
OPTION 5	VALUE = _____	IS: L7 DRIVER
OPTION 6	VALUE = _____	IS: L6 DRIVER
OPTION 7	VALUE = _____	IS: L5 DRIVER
OPTION 8	VALUE = _____	IS: L4 DRIVER
OPTION 9	VALUE = _____	IS: IN1 INPUT
OPTION 10	VALUE = _____	IS: IN2 INPUT
OPTION 11	VALUE = <u>0</u>	IS: VCC PIN
OPTION 12	VALUE = _____	IS: L3 DRIVER
OPTION 13	VALUE = _____	IS: L2 DRIVER
OPTION 14	VALUE = _____	IS: L1 DRIVER
OPTION 15	VALUE = _____	IS: L0 DRIVER
OPTION 16	VALUE = <u>1</u>	IS: SI INPUT
OPTION 17	VALUE = _____	IS: SO DRIVER
OPTION 18	VALUE = _____	IS: SK DRIVER

OPTION DATA		
OPTION 19	VALUE = _____	IS: IN0 INPUT
OPTION 20	VALUE = _____	IS: IN3 INPUT
OPTION 21	VALUE = _____	IS: G0 I/O PORT
OPTION 22	VALUE = _____	IS: G1 I/O PORT
OPTION 23	VALUE = _____	IS: G2 I/O PORT
OPTION 24	VALUE = _____	IS: G3 I/O PORT
OPTION 25	VALUE = _____	IS: D3 OUTPUT
OPTION 26	VALUE = _____	IS: D2 OUTPUT
OPTION 27	VALUE = _____	IS: D1 OUTPUT
OPTION 28	VALUE = _____	IS: D0 OUTPUT
OPTION 29	VALUE = _____	IS: INT INIT LOGIC
OPTION 30	VALUE = <u>0</u>	IS: N/A
OPTION 31	VALUE = _____	IS: TIMER
OPTION 32	VALUE = <u>0</u>	IS: N/A
OPTION 33	VALUE = _____	IS: COP BONDING
OPTION 34	VALUE = <u>0</u>	IS: N/A
OPTION 35	VALUE = <u>0</u>	IS: N/A