TOPAZ SEMICONDUCTOR

CDG4460

6-BIT VIDEO FREQUENCY DIGITAL CONTROLLED ATTENUATOR

ORDERING INFORMATION

16-Pin Ceramic Package	CDG4460J

FEATURES

- Data Latch
- Attenuation Range of 0 to 15.75dB
- Precise Attenuation, Selectable in 0.25dB steps
- Wide Frequency Range, up to 40MHz
- Wide Power Supply Range, ±6.0 to ±15V
- Lower Power Consumption, 0.5μW typ. with ±15V Power Supplies

APPLICATIONS

- Video Attenuation
- Wide Band Amplifier Gain Control
- Variable Burst Generation
- IF Amplifier Attenuation
- Frequency Synthesizers

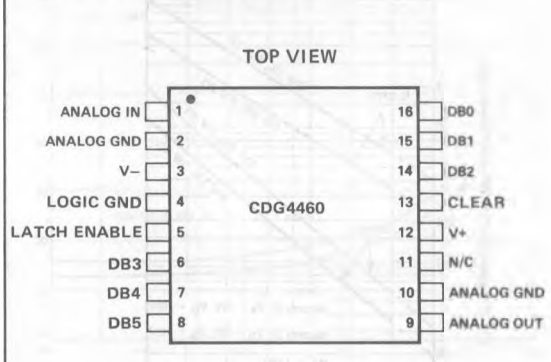
DESCRIPTION

CDG4460J remote controlled Video Attenuators feature Integrated Circuits with high OFF Isolation Lateral D-MOS FETs and low-power CMOS logic with data latches. CMOS/D-MOS ICs are mounted on ceramic substrates along with precision, trimmed resistors. A feature of this circuit is the ability to latch in the attenuator setting for easy microprocessor interfacing.

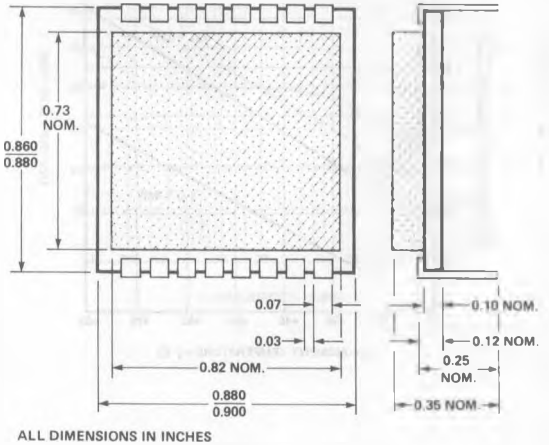
NOTE

All devices contain diodes to protect logic inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed maximum recommended logic or analog input voltages. All unused logic inputs must be connected to logic ground.

PIN CONFIGURATION

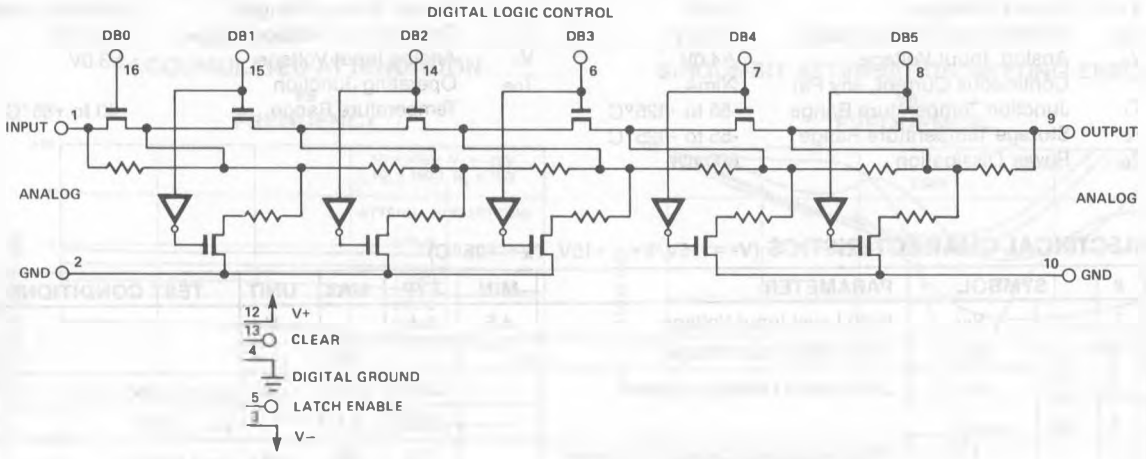


PACKAGE DIMENSIONS



ALL DIMENSIONS IN INCHES

SCHEMATIC DIAGRAM



ATTENUATOR SETTING TABLE

Note: Examples only. Added attenuation can be set to any value between 0 and 15.75dB in 0.25dB steps.

ADDED ATTENUATION (dB)	DATA BIT #—LOGIC SETTING					
	DB0	DB1	DB2	DB3	DB4	DB5
0	0	0	0	0	0	0
0.25	1	0	0	0	0	0
0.50	0	1	0	0	0	0
1.00	0	0	1	0	0	0
2.00	0	0	0	1	0	0
4.00	0	0	0	0	1	0
8.00	0	0	0	0	0	1

EXAMPLES OF OTHER ATTENUATION SETTINGS

0.75	1	1	0	0	0	0
1.75	1	1	1	0	0	0
3.75	1	1	1	1	0	0
7.75	1	1	1	1	1	0
15.25	1	0	1	1	1	1
15.75	1	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS

V-, V+	Supply Voltages	±20V
V_{IN}	Control Input Voltage Range	V- to V+
V_A	Analog Input Voltage	±4.0V
I	Continuous Current, any Pin	20mA
T_J	Junction Temperature Range	-55 to +125°C
T_s	Storage Temperature Range	-55 to +125°C
P_D	Power Dissipation	600mW

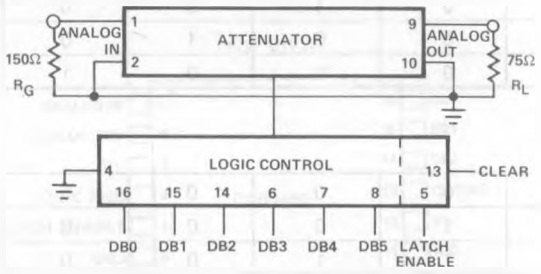
RECOMMENDED OPERATING CONDITIONS

V-, V+	Supply Voltage Ranges	±6.0V to ±15V
V_{IN}	Control Input Voltage Range	0 to +5V
V_A	Analog Input Voltage	±3.0V
T_{OP}	Operating Junction Temperature Range	-40 to +85°C

ELECTRICAL CHARACTERISTICS ($V_- = -15V$, $V_+ = +15V$, $T_A = +25°C$)

#	SYMBOL		PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS
1	STATIC	V_{IH}	High Level Input Voltage		4.5	3.4		V	
2	STATIC	V_{IL}	Low Level Input Voltage				1.0		
3	STATIC	I_{IN}	Logic Input Leakage Current			0.01	0.1	μA	V_{IN} = +5.0V
4						0.02	0.1		V_{IN} = +15V
5	STATIC	I-	Negative Supply Quiescent Current			-0.5	-100	μA	V_{IN} = 0 or V+
6	STATIC	I+	Positive Supply Quiescent Current			0.5	100		
7	DYNAMIC		Insertion Loss			6.0		dB	R_G = 150 Ω, R_L = 75 Ω Attenuation Setting=0dB
8	DYNAMIC	t_{PD}	Propagation Delay	Data to Attn. Set		140	250	nS	V_{IN} = 5.0V
9	DYNAMIC	t_{PC}		Clear to Attn. Reset		100	220		
10	DYNAMIC	t_S	Set Up Time, Data to Latch Enable		150			nS	
11	DYNAMIC	t_H	Hold Time Latch Enable to Data OFF		150			nS	

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

LATCH ENABLE	CLEAR	ATTENUATOR
0	0	Holds data pattern already set.
x	1	Sets all data bits high-max. attenuation
1	0	Latch transparent, attenuation per setting

x = don't care, Logic '0' ≤ 1.0V, Logic '1' ≥ 4.5V

NOTES:

1. Analog Input Ground (pin 2) and Analog Output Ground (pin 10) must be connected to a common point.
2. Logic Ground (pin 4) must be isolated from Analog Ground (pins 2 & 10).

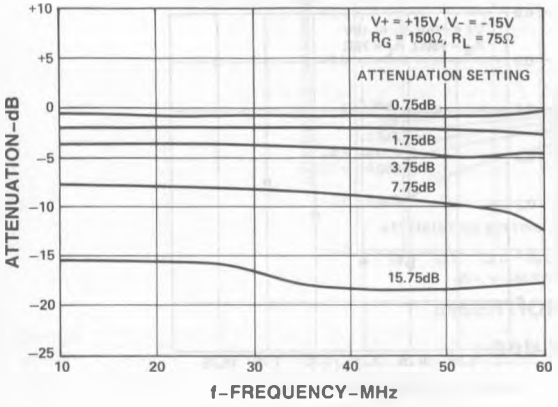
LATCH DATA

If Clear is High (Logic '1' on pin 13) all Data Bits are set to logic '1' for maximum attenuation.

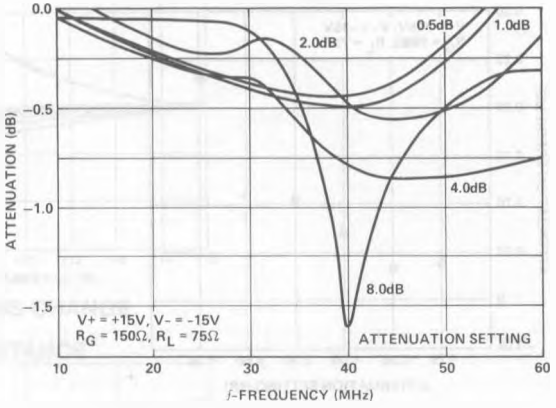
If Latch Enable is High (logic '1' on pin 5) then Latch is transparent.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C)

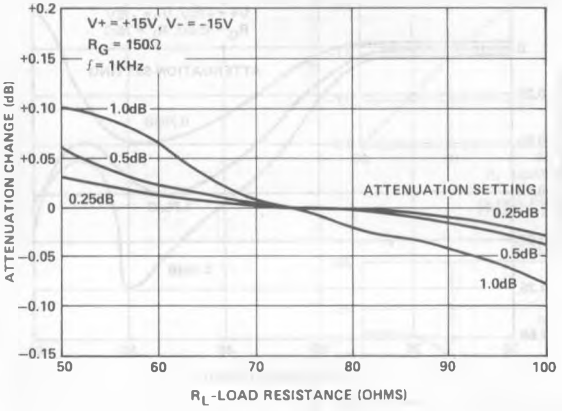
ACCUMULATED ATTENUATION vs FREQUENCY



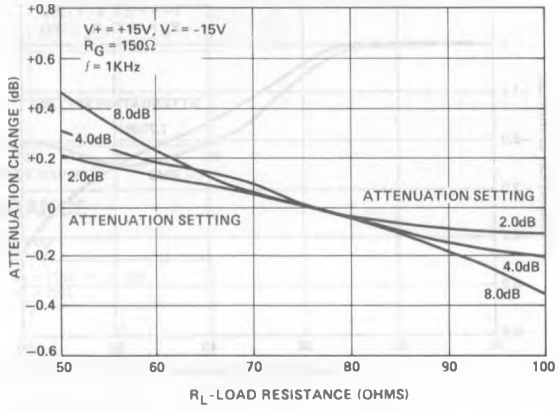
SINGLE-BIT ATTENUATION SETTING ERROR vs FREQUENCY



SINGLE-BIT ATTENUATION CHANGE vs LOAD RESISTANCE



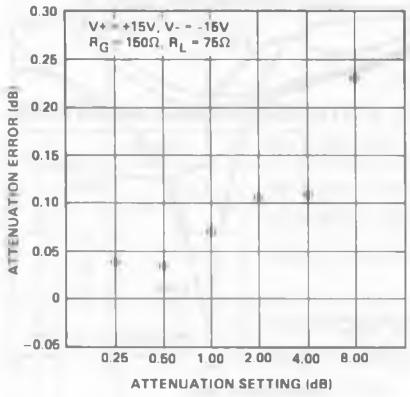
SINGLE-BIT ATTENUATION CHANGE vs LOAD RESISTANCE



NOTE– Attenuation settings are normalized to exclude insertion loss in all curves.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C)

SINGLE-BIT ATTENUATION ERROR vs ATTENUATION SETTING



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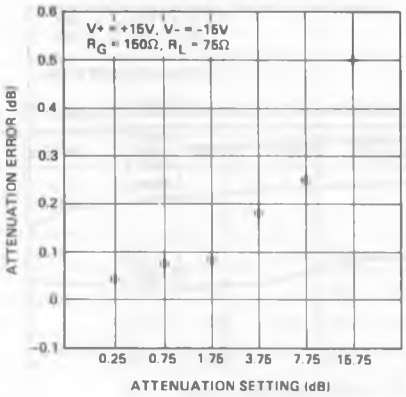

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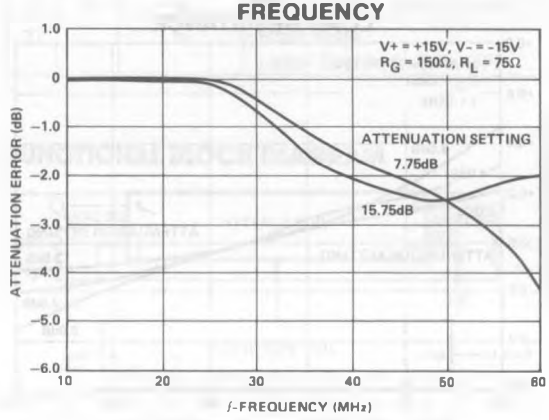

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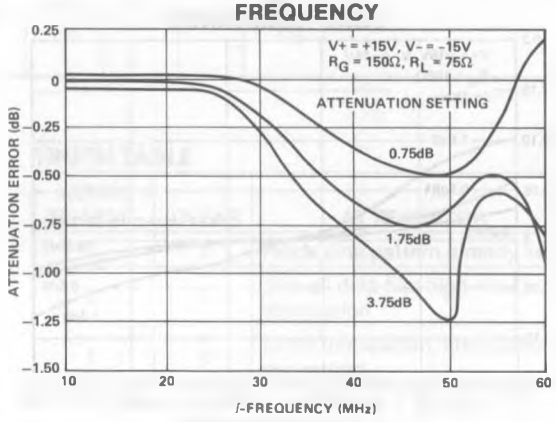
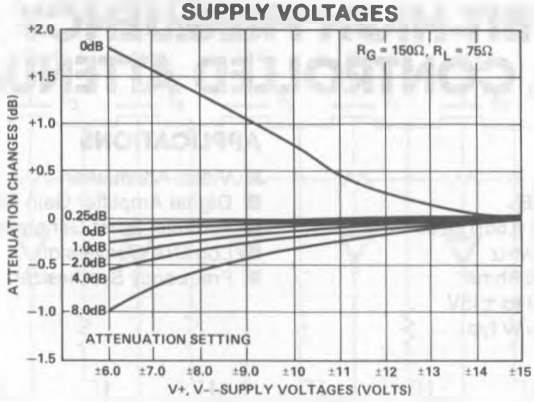
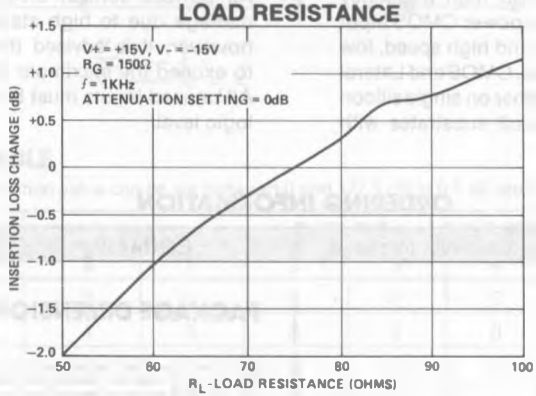


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C)

SINGLE-BIT ATTENUATION CHANGES vs SUPPLY VOLTAGES



INSERTION LOSS CHANGE vs LOAD RESISTANCE



INPUT IMPEDANCE vs FREQUENCY