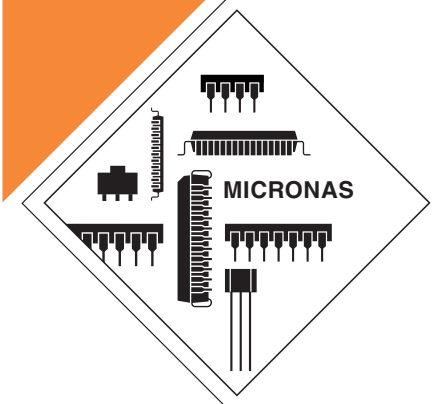

PRELIMINARY DATA SHEET

CDC 32xxG-B Automotive Controller Family User Manual

CDC 3205G-B Automotive Controller

ARM® POWERED

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1. Introduction

The device is a microcontroller for use in automotive applications. The on-chip CPU is ARM® processor ARM7TDMI™ with 32bit data and address bus, which supports Thumb™ format instructions.

The chip contains timer/counters, interrupt controller, multi channel AD converter, stepper motor and LCD driver, CAN interfaces and PWM outputs and a crystal clock multiplying PLL.

1.1. Features

Table 1–1: CDC32xxG-B Family Feature List

	This Device:			
Item	**CDC3205G-A EMU**	**CDC3205G-B EMU**	**CDC3207G-B MCM-Flash**	**CDC3272G-B Mask ROM**
Core				
CPU	32bit ARM7TDMI™			
CPU operation modes	DEEP SLOW, SLOW, FAST and PLL			
CPU clock multiplication	PLL delivering up to 24MHz	PLL delivering up to 50MHz		
EMI Reduction Mode	-	selectable in PLL mode		
Quartz oscillator	4 to 5MHz			
RAM, 32bit wide	16kByte	32kByte	32kByte	12kByte
ROM	ROMless, ext. up to 4M x 32/8M x 16, int. 8-KByte Boot ROM	ROMless, ext. up to 4M x 32/ 8M x 16, int. 8-KByte Boot ROM	512-kByte Flash (256K x 16) top boot conf., int. 8-KByte Boot ROM	384kByte (96K x 32/ 192K x 16), + 8-KByte Test ROM
Digital Watchdog	✔			
Central Clock Divider	✔			
Interrupt Controller expanding IRQ	40 inputs,16 priority levels			
Port Interrupts including Slope Selection	6 inputs			
Patch Module	-			10 ROM locations
Boot System	allows in-system downloading of external code to Flash memory via JTAG			-

Table 1–1: CDC32xxG-B Family Feature List

	This Device:			
Item	**CDC3205G-A EMU**	**CDC3205G-B EMU**	**CDC3207G-B MCM-Flash**	**CDC3272G-B Mask ROM**
Analog				
Reset/Alarm	Combined Input for Regulator Input Supervision			
Clock and Supply Supervision	✔			
10 Bit ADC, charge balance type	16 channels (6 selectable as digital input)	16 channels (each selectable as digital input)		
ADC Reference	VREF Pin	VREF Pin, P1.0 Pin, P1.1 Pin or VREFINT Internal Bandgap selectable		
Comparators	P06COMP with 1/2 AVDD reference	P06COMP with 1/2 AVDD reference, WAITCOMP with Internal Bandgap reference		
LCD	Internal processing of all analog voltages for the LCD driver			
Communication				
DMA	1 DMA Channel for servicing a port or an SPI	3 DMA Channels, one each for servicing the Graphics Bus interface, SPI0 and SPI1		
UART	2: UART0 and UART1			
Synchronous Serial Peripheral Interfaces	2: SPI0 and SPI1			
Full CAN modules V2.0B	3: CAN0, CAN1 and CAN2 with 256bytes of object RAM each (LCAN0009)	3: CAN0, CAN1 and CAN2 with 512bytes of object RAM each (LCAN0009)		2: CAN0 and CAN1 with 512bytes of object RAM each (LCAN0009)
DIGITbus	1 master module			
I^2C	2 master modules: I2C0 and I2C1			
Input & Output				
Universal Ports selectable as 4:1 mux LCD Segment/Backplane lines or Digital I/O Ports	up to 54 I/O or 50 LCD segment lines (=200 segments)	up to 52 I/O or 48 LCD segment lines (=192 segments), individually configurable as I/O or LCD		
Universal Port Slew Rate	Mask selectable	SW selectable		
Stepper Motor Control Modules with high current ports	7 Modules, 32 dI/dt controlled ports			
PWM Modules, each configurable as two 8Bit PWMs or one 16Bit PWM	6 Modules: PWM0/1, PWM2/3, PWM4/5, PWM6/7, PWM8/9 and PWM10/11			
Phase-Frequency Modulator	-	1: PFM0		
Audio Module with auto-decay	✔			
SW selectable Clock outputs	2			

Table 1–1: CDC32xxG-B Family Feature List

	This Device:			
Item	**CDC3205G-A EMU**	**CDC3205G-B EMU**	**CDC3207G-B MCM-Flash**	**CDC3272G-B Mask ROM**
Timers & Counters				
16bit free running counters with Capture/Compare modules	CCC0 with 4 CAPCOM CCC1 with 2 CAPCOM			
16bit timers	1: T0			
8bit timers	4: T1, T2, T3 and T4			
Miscellaneous				
Scalable layout in CAN, RAM and ROM	-		✔	
Various randomly selectable HW options	Set by copy from user program storage during system start-up			
JTAG test interface	✔		allows Flash programming	✔
On Chip Debug Aids	Embedded Trace Module, JTAG		JTAG	
Core Bond-Out	✔		-	
Supply Voltage	4.5 to 5.5V	3.5 to 5.5V (limited I/O performance below 4.5V)		
Case Temperature Range	0 to +70C		-40 to +105C	
Package				
Type	Ceramic 257PGA		Plastic 128QFP 0.5mm pitch	
Bonded Pins	256		128	126

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1.2. Abbreviations

AM	Audio Module
CAN	Controller Area Network Module
CAPCOM	Capture/Compare Module
CCC	Capture/Compare Counter
CPU	Central Processing Unit
DMA	Direct Memory Access Module
ERM	EMI Reduction Mode
ETM	Embedded Trace Module
ICU	Interrupt Controller
I2C	I^2C Interface Module
LCD	Liquid Crystal Display Module
P06COMP	P0.6 Alarm Comparator
PINT	Port Interrupt Module
PWM	8Bit Pulse Width Modulator Module
SM	Stepper Motor Control Module
SPI	Serial Synchronous Peripheral Interface
T	Timer
UART	Universal Asynchronous Receiver Transmitter
WAITCOMP	Wait Comparator

1.3. Block Diagram

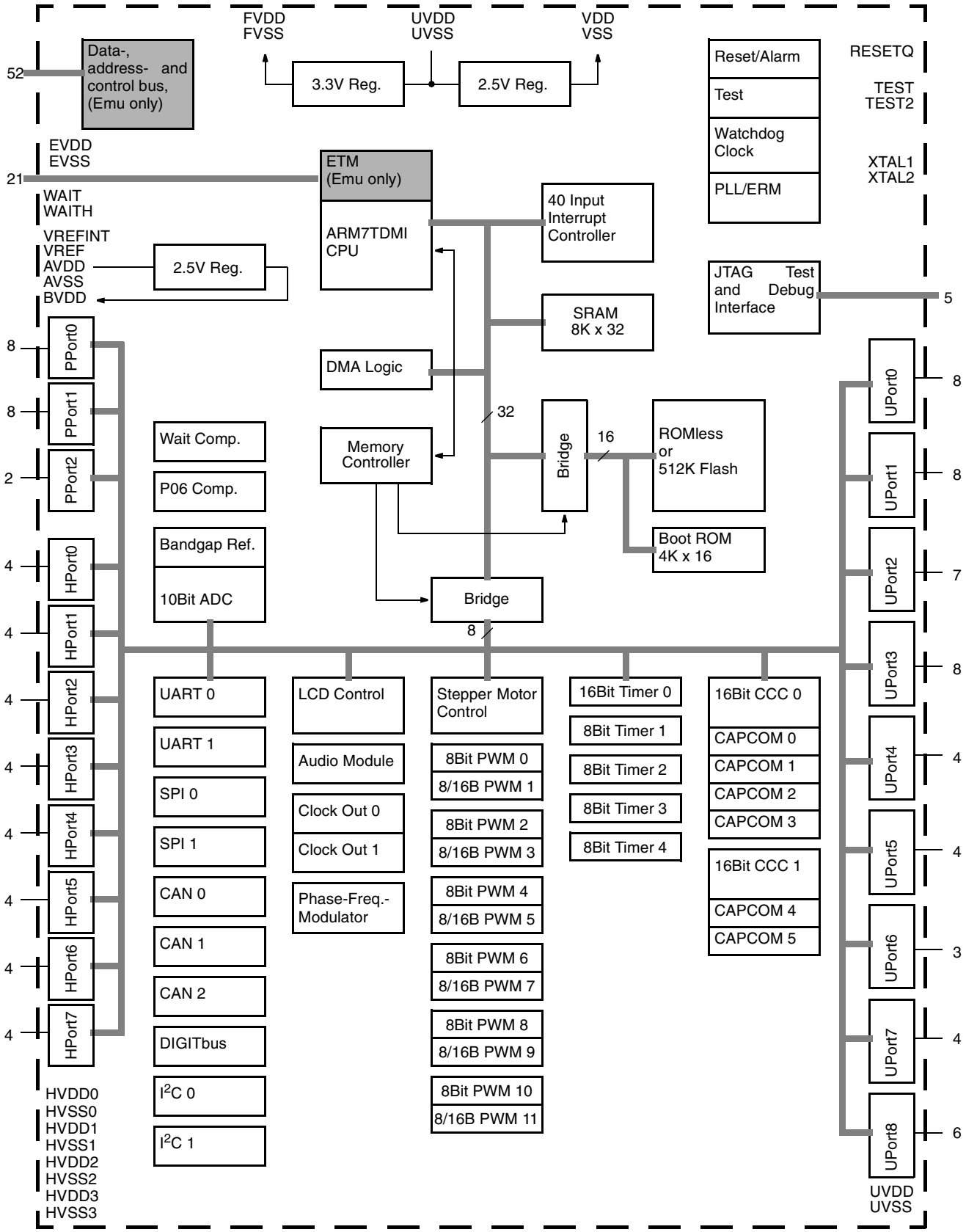


Fig. 1–1: CDC3205G-B block diagram

2. Packages and Pins

2.1. Pin Assignment

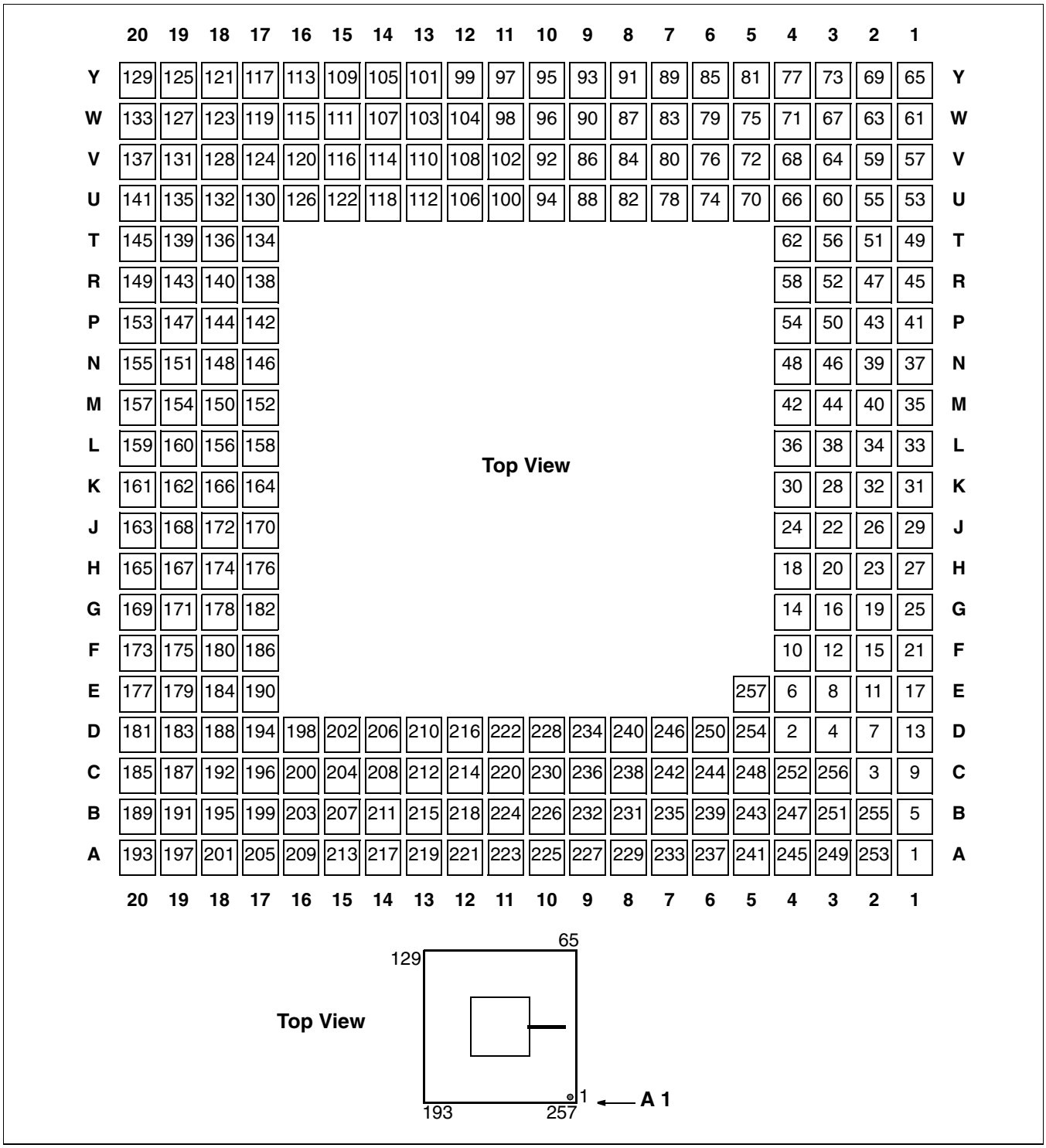


Fig. 2–1: Pin Map of CPGA257 Package

Table 2–1: Pin Assignment for **CPGA257** Package

Pin No.	Co-ord.	Pin Functions			
		Basic Function	Port Special In	Port Special Out	LCD Mode
1	A1	U5.3/GD3	CC4-IN	CC4-OUT	SEG5.3
2	D4	U5.2/GD2	SDA1	SDA1	SEG5.2
3	C2	U5.1/GD1	SCL1	SCL1	SEG5.1
4	D3	U5.0/GD0		PFM0	SEG5.0
5	B1	U2.1	SDA0/CAN0-RX	SDA0	SEG2.1
6	E4	U2.0	SCL0	SCL0/CAN0-TX	SEG2.0
7	D2	U1.7	PINT0	PFM0	SEG1.7
8	E3	U1.6	PINT1	CO0/INTRES	SEG1.6
9	C1	U1.5	PINT2	CO0Q/CO1	SEG1.5
10	F4	TEST			
11	E2	RESETQ/ALARMQ			
12	F3	XTAL2			
13	D1	XTAL1			
14	G4	VSS			
15	F2	VDD			
16	G3	U1.4		ITSTOUT/AM-OUT	SEG1.4
17	E1	U1.3		MTO/AM-PWM	SEG1.3
18	H4	U1.2	MTI/ITSTIN	T0-OUT/INTRES	SEG1.2
19	G2	U1.1		T1-OUT	SEG1.1
20	H3	U1.0		T2-OUT	SEG1.0
21	F1	U0.7		T3-OUT	SEG0.7
22	J3	U0.6	CC3-IN	T4-OUT/CC3-OUT	SEG0.6
23	H2	U0.5	PINT4	CC3-OUT	SEG0.5
24	J4	U0.4	PINT5	CO1	SEG0.4
25	G1	U0.3		PWM0	SEG0.3
26	J2	U0.2		PWM1	SEG0.2
27	H1	U0.1		PWM2	SEG0.1
28	K3	U0.0		PWM3	SEG0.0
29	J1	D31			
30	K4	D30			
31	K1	D29			
32	K2	D28			
33	L1	D27			
34	L2	D26			
35	M1	D25			
36	L4	EVDD8			
37	N1	EVSS8			
38	L3	D24			
39	N2	D23			
40	M2	D22			
41	P1	D21			
42	M4	D20			
43	P2	D19			
44	M3	D18			
45	R1	D17			
46	N3	D16			
47	R2	D15			
48	N4	D7			
49	T1	D14			
50	P3	EVDD7			
51	T2	EVSS7			
52	R3	D6			
53	U1	D13			
54	P4	D5			
55	U2	D12			
56	T3	D4			
57	V1	D11			
58	R4	D3			
59	V2	D10			
60	U3	D2			
61	W1	D9			
62	T4	D1			
63	W2	D8			
64	V3	EVDD6			

Table 2–1: Pin Assignment for **CPGA257** Package

Pin No.	Co-ord.	Pin Functions			
		Basic Function	Port Special In	Port Special Out	LCD Mode
65	Y1	EVSS6			
66	U4	D0			
67	W3	OEQ			
68	V4	CE0Q			
69	Y2	BWQ3			
70	U5	BWQ2			
71	W4	BWQ1			
72	V5	BWQ0			
73	Y3	EMUTRI			
74	U6	ABORT			
75	W5	EXTERN0			
76	V6	EXTERN1			
77	Y4	H7.3		SME1+/PWM4	
78	U7	H7.2		SME1-/PWM6	
79	W6	H7.1		SME2+/PWM8	
80	V7	H7.0	SME-COMP	SME2-/PWM9	
81	Y5	HVDD2			
82	U8	HVSS2			
83	W7	H6.3		PWM8	
84	V8	H6.2		PWM9	
85	Y6	H6.1		PWM10	
86	V9	H6.0		PWM11	
87	W8	H5.3		SMD1+	
88	U9	H5.2		SMD1-	
89	Y7	HVDD0			
90	W9	HVSS0			
91	Y8	H5.1		SMD2+	
92	V10	H5.0	SMD-COMP	SMD2-	
93	Y9	H4.3		SMA1+	
94	U10	H4.2		SMA1-	
95	Y10	H4.1		SMA2+	
96	W10	H4.0	SMA-COMP	SMA2-	
97	Y11	H3.3		SMB1+	
98	W11	H3.2		SMB1-	
99	Y12	H3.1		SMB2+	
100	U11	H3.0	SMB-COMP	SMB2-	
101	Y13	H2.3		SMC1+	
102	V11	H2.2		SMC1-	
103	W13	HVDD1			
104	W12	HVSS1			
105	Y14	H2.1		SMC2+	
106	U12	H2.0	SMC-COMP	SMC2-	
107	W14	H1.3		SMF1+	
108	V12	H1.2		SMF1-	
109	Y15	H1.1		SMF2+	
110	V13	H1.0	SMF-COMP	SMF2-	
111	W15	HVDD3			
112	U13	HVSS3			
113	Y16	H0.3		SMG1+/PWM1	
114	V14	H0.2		SMG1-/PWM3	
115	W16	H0.1		SMG2+/PWM5	
116	V15	H0.0	SMG-COMP	SMG2-/PWM7	
117	Y17	nTRST			
118	U14	ETDI			
119	W17	ETMS			
120	V16	ETCK			
121	Y18	ETDO			
122	U15	ABE			
123	W18	CE1Q			
124	V17	FBUSQ			
125	Y19	AMCS1			
126	U16	AICU2			
127	W19	AICU3			
128	V18	EVSS5			

Table 2–1: Pin Assignment for **CPGA257** Package

Pin No.	Coord.	Pin Functions			
		Basic Function	Port Special In	Port Special Out	LCD Mode
129	Y20	EVDD5			
130	U17	AICU4			
131	V19	AICU5			
132	U18	AICU6			
133	W20	AICU7			
134	T17	A8			
135	U19	A18			
136	T18	A19			
137	V20	EVDD4			
138	R17	EVSS4			
139	T19	WEQ/RWQ			
140	R18	A9			
141	U20	A10			
142	P17	A11			
143	R19	A12			
144	P18	A13			
145	T20	A14			
146	N17	A15			
147	P19	EVDD3			
148	N18	EVSS3			
149	R20	A16			
150	M18	A17			
151	N19	A20			
152	M17	A21			
153	P20	A22			
154	M19	A23			
155	N20	AMCM21			
156	L18	AMCM22			
157	M20	EVDD2			
158	L17	EVSS2			
159	L20	AMCM23			
160	L19	SEQ			
161	K20	nMREQ			
162	K19	MAS0			
163	J20	MAS1			
164	K17	nRESET			
165	H20	P1.7	PINT5		
166	K18	P1.6	PINT4		
167	H19	P1.5	PINT3		
168	J19	P1.4	PINT2		
169	G20	P1.3	PINT1		
170	J17	P1.2	PINT0		
171	G19	P1.1	VREF1		
172	J18	P1.0	VREF0		
173	F20	VREF			
174	H18	VREFINT			
175	F19	AVDD			
176	H17	AVSS			
177	E20	BVDD			
178	G18	WAIT			
179	E19	WAITH			
180	F18	P0.7			
181	D20	P0.6	P0.6 Comp.		
182	G17	P0.5			
183	D19	P0.4			
184	E18	P0.3			
185	C20	P0.2			
186	F17	P0.1			
187	C19	P0.0	CC4-IN		
188	D18	P2.1			
189	B20	P2.0			
190	E17	U6.2		GWEQ	SEG6.2
191	B19	U6.1	CAN1-RX	GOEQ	SEG6.1
192	C18	U6.0		CAN1-TX	SEG6.0

Table 2–1: Pin Assignment for **CPGA257** Package

Pin No.	Coord.	Pin Functions			
		Basic Function	Port Special In	Port Special Out	LCD Mode
193	A20	U8.5	CAN2-RX/PINT3	LCD-SYNC-OUT	SEG8.5
194	D17	U8.4	LCD-SYNC-IN	CAN2-TX	SEG8.4
195	B18	U8.3	(CAN3-RX)	LCD-CLK-OUT	SEG8.3
196	C17	U8.2	LCD-CLK-IN	(CAN3-TX)	SEG8.2
197	A19	U8.1		CC3-OUT	SEG8.1
198	D16	U8.0		CC4-OUT	SEG8.0
199	B17	U4.3	CAN0-RX	TO2	BP3
200	C16	U4.2		CAN0-TX	BP2
201	A18	U4.1	CC0-IN	SPI1-D-OUT	BP1
202	D15	U4.0	SPI1-D-IN	CC0-OUT	BP0
203	B16	U3.7	SPI1-CLK-IN	SPI1-CLK-OUT	SEG3.7
204	C15	U3.6		SPI0-D-OUT	SEG3.6
205	A17	U3.5	SPI0-D-IN	TO3	SEG3.5
206	D14	U3.4	SPI0-CLK-IN	SPI0-CLK-OUT	SEG3.4
207	B15	U3.3		CO0/TDO	SEG3.3
208	C14	U3.2	CC0-IN / TCK	CC0-OUT	SEG3.2
209	A16	U3.1	CC1-IN / TMS	CC1-OUT	SEG3.1
210	D13	U3.0	CC2-IN / TDI	CC2-OUT	SEG3.0
211	B14	TEST2			
212	C13	UVDD1			
213	A15	UVSS1			
214	C12	TRACEPKT0 / TBIT			
215	B13	TRACEPKT1 / nM0			
216	D12	TRACEPKT2 / nM1			
217	A14	TRACEPKT3 / nM2			
218	B12	TRACEPKT4 / nM3			
219	A13	TRACEPKT5 / nM4			
220	C11	EVDD1			
221	A12	EVSS1			
222	D11	TRACEPKT6 / LOCK			
223	A11	TRACEPKT7 / nEXEC			
224	B11	TRACEPKT8 / nOPC			
225	A10	TRACEPKT9 / nTRANS			
226	B10	TRACEPKT10 / A5			
227	A9	TRACEPKT11 / A6			
228	D10	TRACEPKT12 / RANGEOUT0			
229	A8	TRACEPKT13 / RANGEOUT1			
230	C10	TRACEPKT14 / A7			
231	B8	TRACEPKT15 / BREAKPT			
232	B9	PIPESTAT0 / nRW			
233	A7	PIPESTAT1 / A0			
234	D9	PIPESTAT2 / A1			
235	B7	EVDD0			
236	C9	EVSS0			
237	A6	TRACESYNC/A2			
238	C8	TRACECLK/A3			
239	B6	EXTTRIG/A4			
240	D8	FSYS			
241	A5	nWAIT			
242	C7	DBGACK			
243	B5	DBGRQ			
244	C6	UVDD			
245	A4	UVSS			
246	D7	U2.6	DIGIT-IN	DIGIT-OUT	SEG2.6
247	B4	U2.5	UART0-RX	CC1-OUT	SEG2.5
248	C5	U2.4	CC1-IN	UART0-TX	SEG2.4
249	A3	U2.3	UART1-RX	CC2-OUT	SEG2.3
250	D6	U2.2	CC2-IN	UART1-TX	SEG2.2
251	B3	U7.7/GD7		CO0	SEG7.7
252	C4	U7.6/GD6		CO1	SEG7.6
253	A2	U7.5/GD5		LCK(/PFM1)	SEG7.5
254	D5	U7.4/GD4	CC5-IN	CC5-OUT	SEG7.4
255	B2	FVDD			
256	C3	FVSS			
257	E5	Extra insertion Pin: connect to system ground			

2.2. Package Outline Dimensions

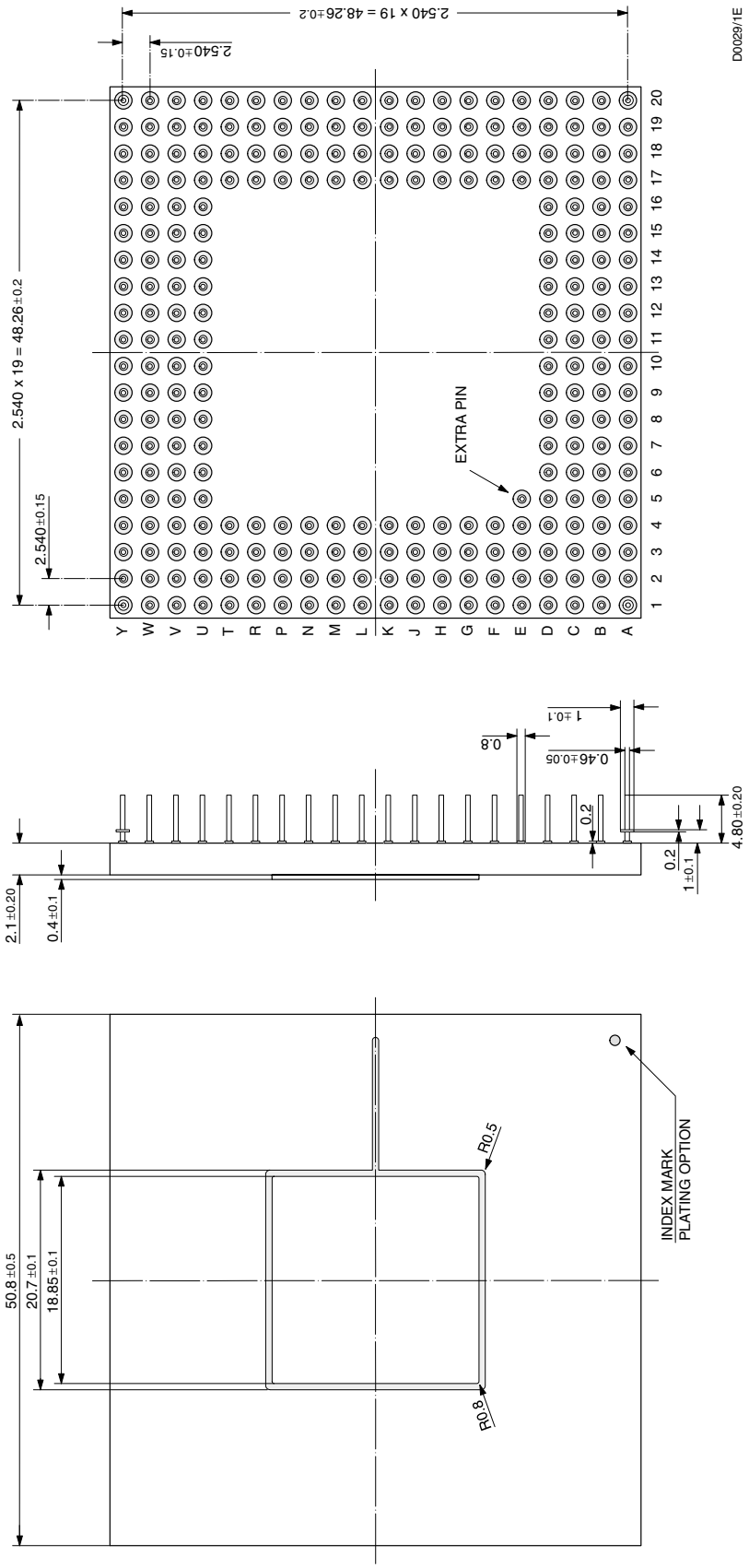


Fig. 2–2: CPGA257 Ceramic Pin Grid Array 257-Pin (Weight approx. 32g. Dimensions in mm)

2.3. Multiple Function Pins

2.3.1. U-Ports

Beside their basic function (digital I/O), Universal Ports (prefix “U”) have overlaid alternative functions (see Table 2–1 on page 12).

How to enable Basic Function, Special In and Special Out mode is explained in the functional description of the U-Ports. How to enable LCD mode is explained in the functional descriptions of LCD module and U-Ports.

2.3.2. H-Ports

Beside their basic function (digital I/O), High Current Ports (prefix “H”) have overlaid alternative functions (see Table 2–1 on page 12).

How to enable Basic Function, Special In and Special Out mode is explained in the functional description of the H-Ports.

2.3.3. Emulator Bus

In contrast to the PQFP128 standard package, the CPGA257 package has additional pins (Emulator Bus) which serve as memory interface, Emulation JTAG interface or connection to an external emulation or trace hardware (Trace Bus).

The functionality of the memory interface and the Trace Bus is controlled by register CR. Refer to section “Control Word” for more information.

Some of the following pins are marked as being ARM or ETM signals. For details of the functionality please refer to ARM7TDMI Data sheet (Document Number: ARM DDI 0029) or Embedded Trace Macro Cell (Document Number: ARM IHI 0014 and ARM DDI 0158).

2.4. Pin Function Description

A0 to A7 (ARM) 1)
A8 to A23 (ARM) 4)
These 24 lines are the original CPU addresses. Some are used for external memory access on the Emulator Bus. The function is controlled by register CR.

ABE (ARM) 1) 2)
This pin outputs the “Address bus enable” signal of the ARM. It indicates that the CPU does not access the data and address bus when low. It is not possible to influence the CPU via this pin.

ABORT (ARM) 3)
This is an input which allows the memory system to tell the processor that a requested access is not allowed.

AICU2 to AICU7 4)
These pins correspond to the ARM address bus lines A2 to A7 but can be modified by the ICU. In the latter case AICUx and Ax are not equal.

ALARMQ
This is the second input comparator level on the RESETQ pin.

AMCM21 to AMCM23 4)
These pins correspond to the ARM address bus lines A21 to A23 but can be modified by the memory controller. In the latter case AMCMx and Ax are not equal.

AMCS1 4)
This pin corresponds to the ARM address bus line A1 but can be modified by the memory controller. In the latter case AMCS1 and A1 are not equal.

AM-OUT
This is the output signal of the Audio Module.

AM-PWM
This is the output signal of the 8-bit PWM of the Audio Module. It is intended for testing only.

AVDD
This is the positive power supply for ADC, P06COMP, WAITCOMP and BVDD regulator. AVDD should be kept at UVDD ±0.5V. It must be buffered by an external capacitor to analog ground

AVSS
This is the negative reference for the ADC and the negative power supply for ADC, P06COMP, WAITCOMP and PLL. Connect to analog ground.

BP0 to BP3
These pin functions serve as Backplane drivers for a 4:1 multiplexed LCD.

BREAKPT (ARM) 3)
This is the input pin for the ARM BREAKPT signal in Full Trace mode. It allows external hardware to halt the execution of the processor for debug purposes.

BVDD
This is the output of the internal 2.5V regulator for the PLL. It must be buffered by an external capacitor to analog ground.

BWQ0 to BWQ3 4)
This is the byte write control signal to an external 32bit memory.

CAN0-RX, CAN1-RX, CAN2-RX
These signals provide the input lines for the CAN0, CAN1, CAN2 and CAN3 modules.

CAN0-TX, CAN1-TX, CAN2-TX
These signals provide the output lines for the CAN0, CAN1, CAN2 and CAN3 modules.

CC0-IN, CC1-IN, CC2-IN, CC3-IN, CC4-IN, CC5-IN
These signals are the capture inputs of the CAPCOM0 to CAPCOM5 modules.

CC0-OUT, CC1-OUT, CC2-OUT, CC3-OUT, CC4-OUT, CC5-OUT

These signals are the compare outputs of the CAPCOM0 to CAPCOM5 modules.

CE0Q 4)
Chip Enable output signal connects to external program memory's CEQ pin. With CR.EFLA set it serves to reduce program memory's power consumption when CPU operates in slow mode. Active LOW.

CE1Q 4)
Chip Enable output signal connects to external RAM or Boot ROM memory's CEQ pin and reduces it's power consumption when CPU operates in slow mode. Active LOW.

CO0, CO0Q, CO1
These signals provide frequency outputs. They are connected to internal prescaler and multiplexer. They can be hard wired by HW Option. Refer to section "Hardware Options" for setting the CO0/CO1 options and section "CPU and Clock System" setting the Clock Out 0 Selection register.

For testing purposes it is possible to drive clocks and other signals of internal peripheral modules out of CO0 and CO1. Selection is done via register TST2.

D0 to D31 (ARM) 4)
These 32 signals are the original CPU bidirectional Data Bus lines. They provide the 32bit data bus for use during data exchanges between the microprocessor and external memory or peripherals.

DBGACK (ARM)
This is the debug acknowledge output signal of the ARM. When high indicates ARM is in debug state.

DBGRQ (ARM) 3)
This is the debug request input of the ARM. It is a level-sensitive input, which when high causes ARM to enter debug state after executing the current instruction.

DIGIT-IN
This is the receive input line of the DIGITbus module.

DIGIT-OUT
This is the transmit output line of the DIGITbus module.

EMUTRI
This input signal allows to tristate (= high) the interface pins to external memory (A8 to A23, AMCS1, AICU2 to AICU7, AMCM21 to AMCM23, CE1Q, FBUSQ and WEQ/RWQ).

ETCK (ARM)
This pin is the ARM "Test clock" input (TCK) of the Emulation JTAG interface.

ETDI (ARM)
This pin is the ARM "Test data input" (TDI) of the Emulation JTAG interface.

ETDO (ARM)
This pin is the ARM "Test data output" (TDO) of the Emulation JTAG interface.

ETMS (ARM)
This pin is the ARM "Test mode select" (TMS) input of the Emulation JTAG interface.

EVDD0 to EVDD8
These 9 lines form the positive power supply of the Emulator and Trace Bus drivers. EVDD0 to EVDD8 may be connected to any voltage between 3 to 5.5V. Normally they are connected to FVDD.

EVSS0 to EVSS8
These 9 lines form the negative supply of the Emulator Bus and Trace drivers. EVSS0 to EVSS8 have to be hard wired to system ground.

EXTERN0, EXTERN1 (ARM) 3)
These are inputs to the ICEBreaker logic of the ARM which allows breakpoints and/or watch points to be dependent on an external condition.

EXTTRIG (ETM) 2)
This is a trigger input to the ETM.

FBUSQ 4)
This signal is the reference for access to external synchronous memory. It is active for memory access only.

FSYS
This signal provides the system frequency clock f_{SYS}. It is the PLL output frequency if PLL is enabled.

FVDD
This is the output of the internal 3.3V regulator for the external Flash chip. It must be buffered by an external capacitor to FVSS.

FVSS
This is the ground reference of the internal 3.3V regulator for the external Flash chip.

GD0 to GD7
These eight Graphics IC Data lines provide an 8-bit DMA controlled data link to an external IC.

GOEQ
This Graphics IC Read line provides the control signal for read accesses via the GD7 to GD0 bus. Active LOW.

GWEQ
This Graphics IC Write line provides the control signal for write accesses via the GD7 to GD0 bus. Active LOW.

H0.0 to H7.3
The High Current Ports are intended for use as digital I/O which can drive higher currents than the Universal Ports.

HVDD0 to HVDD3
The pins HVDD0 to HVDD3 are the positive power supply of the high current ports H0.0 to H7.3. HVDD0 to HVDD3 should be kept at UVDD ±0.5V. Be careful to design the PCB traces for carrying the considerable operating current on these pins.

HVSS0 to HVSS3
The pins HVSS1 to HVSS3 are the negative power supply for the high current ports H0.0 to H7.3. HVSS0 to HVSS3 have to be hard wired to system ground. Be careful to layout sufficient PCB traces for carrying the considerable operating current on these pins.

INTRES
Test output of internal reset signal. Only for testing and available only in test mode.

ITSTIN
Test input signal for Interrupt Controller. Only for testing and available only in test mode.

ITSTOUT
Test output signal of internal peripheral modules. Only for testing and available only in test mode.

LCD-CLK-IN
The Clock input of the LCD module receives the clock of an optional external LCD master driver which is used to extend

the LCD driver capability. This input is active if the internal LCD module is configured as slave and the external LCD driver operates as master.

LCD-CLK-OUT
The Clock output of the LCD module provides a clock signal to optional external LCD slave drivers if the internal LCD module is configured as master and the other LCD drivers are slaves.

LCD-SYNC-IN
The Synchronization input of the LCD module receives the sync signal from an optional external LCD master driver. This input is active if the internal LCD module is configured as slave and the external LCD driver serves as master.

LCD-SYNC-OUT
The Synchronization output of the LCD module provides a sync signal to optional external LCD slave drivers if the internal LCD module is configured as master and the other LCD drivers are slaves.

LCK
This output signal indicates that the PLL has locked.

LOCK (ARM) 1)
This is the LOCK output signal of the ARM indicating that the processor is performing a “locked” memory access when high.

MAS0, MAS1 (ARM) 1) 2)
These are ARM output signals used by the processor to indicate to the external memory system when a word transfer or a half-word or a byte length is required.

MTI
This is a test input line. It is intended for factory test only. The application should not use this signal.

MTO
This is a test output line. It is intended for factory test only. The application should not use this signal.

nEXEC (ARM) 1)
This is the “Not executed” signal of the ARM indicating that the instruction in the execution unit is not being executed when high.

nM0 to nM4 (ARM) 1)
These pins output the “Not processor mode” signal of the ARM.

nMREQ (ARM) 1) 2)
This pin outputs the “Not memory request” signal of the ARM. The processor requires memory access during the following cycle when low.

nOPC (ARM) 1)
This pin outputs the “Not op-code fetch” signal of the ARM. The processor is fetching an instruction from memory when low.

nRESET (ARM)
This pin outputs the “Not reset” signal of the ARM. This pin is not an input.

nRW (ARM) 1)
This pin outputs the “Not read/write” signal of the ARM. High indicates a processor write cycle, low a read cycle.

nTRANS (ARM) 1)
This pin outputs the “Not memory translate” signal of the ARM. When low it indicates that the processor is in user mode.

nTRST (ARM)
This pin is the “Not test reset” signal of the ARM. It resets the boundary scan logic of the CPU when low. It is also the reset for the Emulation JTAG interface (not for the application JTAG interface).

nWAIT (ARM) 1) 2)
This pin outputs the “Not wait” signal of the ARM. It is not possible to cause a wait via this pin.

OEQ 4)
The Output Enable signal connects to the OEQ pin of external memory for read access. Active LOW.

P0.0 to P0.7, P1.0 to 1.7 and P2.0 to P2.1
P0.0 to P1.7 are 16 analog ports that are the multiplexed input channels of the ADC. All analog ports P0.0 to P2.1 can also be used as digital input lines. The analog ports P1.2 to P1.7 can also be used as port interrupts.

P06 Comp.
The analog port P0.6 is additionally input to the P06 comparator.

PFM0
This is the output of the Pulse Frequency Module, PFM.

PINT0 to PINT5
The Port Interrupt 0 to 5 inputs serves as inputs to the interrupt controller via the port interrupt module. HW option PM.PINT has to be set to determine which of the possible input pins are used as source of PINT0 to 5.

PIPESTAT0 to PIPESTAT2 (ETM) 2)
These signals indicate the pipeline status of the ETM.

PWM0 to PWM11
These are the outputs of the PWM module. Some of these PWM signals are directed to two pins.

RANGEOUT0, RANGEOUT1 (ARM) 1)
These pins output the “ICEBreaker rangeout” signals of the ARM. They indicate that ICEBreaker watch point register 0 or 1 has matched the conditions currently present on the address, data and control busses.

RESETQ
This bidirectional signal is used to initialize all modules and start program execution.

Two comparators distinguish three input levels:

– A low level resets all internal modules.

– A medium level activates all internal modules and starts program execution. An alarm signal is generated which can be directed to the interrupt controller.

– A high level keeps all internal modules active and cancels the alarm signal.

The RESETQ input signal must be held low for at least two clock cycles after VDD reaches operating voltage.

Internal reset sources output their reset request on the RESETQ pin via an internal open drain pull-down transistor. Thus RESETQ can be wire-ored with external reset sources. The internally limited pull-down current allows direct connection to large capacitors. The connection of such a capacitor (e.g. 10nF) is recommended to reduce the capacitive influence of the neighboring XTAL2 pin.

RESETQ must be pulled up by an external pull-up resistor (e.g. 10kΩ).

RWQ 4)
This is an interface signal to external memory.

SCL0 to SCL1
These are the serial clock lines of the I2C modules.

SDA0 to SDA1
These are the serial data lines of the I2C modules.

SEG0.0 to SEG8.5
These pin functions serve as Segment drivers for a 4:1 multiplexed LCD.

SEQ (ARM) 1) 2)
This pin outputs the “Sequential address” signal of the ARM. High indicates that the address of the next memory cycle will be related to that of the last memory access.

SMA to SMG
These lines are intended for driving stepper motors. They are the outputs of the SM. Two of these lines together with an external coil form an H-bridge. Thus each of the signals SMA to SMG can drive a two phase bipolar stepper motor.

SMA-COMP to SMG-COMP
These lines are comparator inputs that connect to one line each of the SMA to SMG lines. They serve to distinguish rotation from stand-still during zero detection in each stepper motor.

SPI0-CLK-IN, SPI1-CLK-IN
The Serial Synchronous Peripheral Interface Clock input receives the bit clock from an external master, to shift data in or out of SPI0 resp. SPI1 in slave mode. This means that the external master controls the bit stream.

SPI0-CLK-OUT, SPI1-CLK-OUT
The Serial Synchronous Peripheral Interface Clock output supplies the bit clock of SPI0 resp. SPI1 to an external slave, to shift data in or out of SPI0 resp. SPI1 in master mode. This means that the internal SPI controls the bit stream.

SPI0-D-IN, SPI1-D-IN
These are the data input lines of the SPI0 and SPI1 modules.

SPI0-D-OUT, SPI1-D-OUT
These are the data output lines of the SPI0 and SPI1 modules.

T0-OUT
The Timer 0 output is connected to the zero output of T0 by a divide by 2 scaler. The scaler generates a 50% pulse duty factor.

T1-OUT to T4-OUT
These signals are connected to the overflow outputs of T1 to T4.

TBIT (ARM) 1)
This pin outputs the TBIT signal of the ARM. High indicates that the processor is executing the THUMB instruction set.

TCK (ARM)
This pin is the ARM “Test clock” input of the application JTAG interface.

TDI (ARM)
This pin is the ARM “Test data input” of the application JTAG interface.

TDO (ARM)
This pin is the ARM “Test data output” of the application JTAG interface.

TEST, TEST2
Pins TEST and TEST2 define the source for the Control Word fetch during reset. Please refer to section “Core Logic” for detailed information.

TEST2 serves to enable the JTAG interface. Refer to section “JTAG Interface“ for detailed information.

For normal operation with internal code connect TEST and TEST2 to System Ground or leave it floating (internal pull-down).

TMS (ARM)
This pin is the ARM “Test mode select” input of the application JTAG interface.

TO2 and TO3
Test outputs.

TRACECLK (ETM) 2)
This is the output of the modified CLK signal of the ETM.

TRACEPKT0 to TRACEPKT15 (ETM) 2)
This is the trace packet port of the ETM.

TRACEPKT15 is pulled low to prevent floating, when full trace mode is enabled.

TRACESYNC (ETM) 2)
This is the synchronization signal from the ETM, indicating the start of a branch sequence on the trace packet port.

U0.0 to U8.5
Universal ports are intended for use as digital I/O or as LCD driver outputs.

UART0-RX, UART1-RX
These are the Receive input lines of UART0 and UART1. Polarity of the signals is settable by HW options UA0 resp. UA1.

UART0-TX, UART1-TX
These are the data output lines of UART0 and UART1. Polarity of signals is settable by HW options UA0 resp. UA1.

UVDD, UVDD1
The pins UVDD and UVDD1 are the positive 5V supply for the U-Port output stages, for the VDD regulator and the FVDD regulator. (see Fig. 2–3 for external connection). It must be buffered by an external capacitor to UVSS resp. UVSS1.

UVSS, UVSS1
The pins UVSS and UVSS1 are the negative power supply for the U-Port output stages, and the ground reference for the VDD and FVDD regulators. They have to be connected to system ground (see Fig. 2–3).

VDD
This is the output of the internal 2.5V regulator for the internal digital modules (see Fig. 2–3 for external connection). It must be buffered by an external capacitor to VSS.

VREF, VREF0, VREF1
These pins are selectable as positive reference inputs for the ADC. The voltage on these pins should be set to a level between 2.56 Volts and AVDD.

VREFINT
This pin is the positive reference output of the ADC. The voltage at this pin is generated internally (approx. 2.5V) and must be buffered by an external capacitor to AVSS. No DC load is allowed.

VSS
The pin VSS is the negative supply terminal of the internal digital modules (see Fig. 2–3 for external connection).

WAIT
This is the positive input to the WAIT comparator. The negative input is VREFINT. The comparator level can be adjusted by an external voltage divider.

WAITH
This is the output of the WAIT comparator. The hysteresis can be adjusted by an external feedback resistor to the voltage divider connected to the WAIT pin.

WEQ 4)
The output signal Write Enable connects to the external memory's WEQ pin and activates it for write access. Active LOW.

XTAL1
This is the quartz oscillator or clock input pin (see Fig. 2–3 for external connection).

XTAL2
This is the quartz oscillator output pin for two pin oscillator circuits (see Fig. 2–3 for external connection).

1) Trace Bus output. Active in Analyzer mode.
2) Trace Bus output. Active in ETM mode.
3) Trace Bus input. Always active.
4) Memory interface signal. Tristate if EMUTRI is high.
Please refer to section "Memory Interface" (see Table 32–1 on page 219) for details about interfaces and Trace Bus modes.

2.5. External Components

To provide effective decoupling and to improve EMC behaviour, the small decoupling capacitors must be located as close to the supply pins as possible. The self-inductance of these capacitors and the parasitic inductance and capacitance of the interconnecting traces determine the self-resonant frequency of the decoupling network. Too low a frequency will reduce decoupling effectiveness, will increase RF emissions and may adversely affect device operation.

XTAL1 and XTAL2 quartz connections are especially sensitive to capacitive coupling from other pc board signals. It is strongly recommended to place quartz and oscillation capacitors as close to the pins as possible and to shield the XTAL1 and XTAL2 traces from other signals by embedding them in a VSS trace.

The RESETQ pin adjacent to XTAL2 should be supplied with a small capacitor, to prevent fast RESETQ transients from being coupled into XTAL2, and to prevent XTAL2 from coupling into RESETQ.

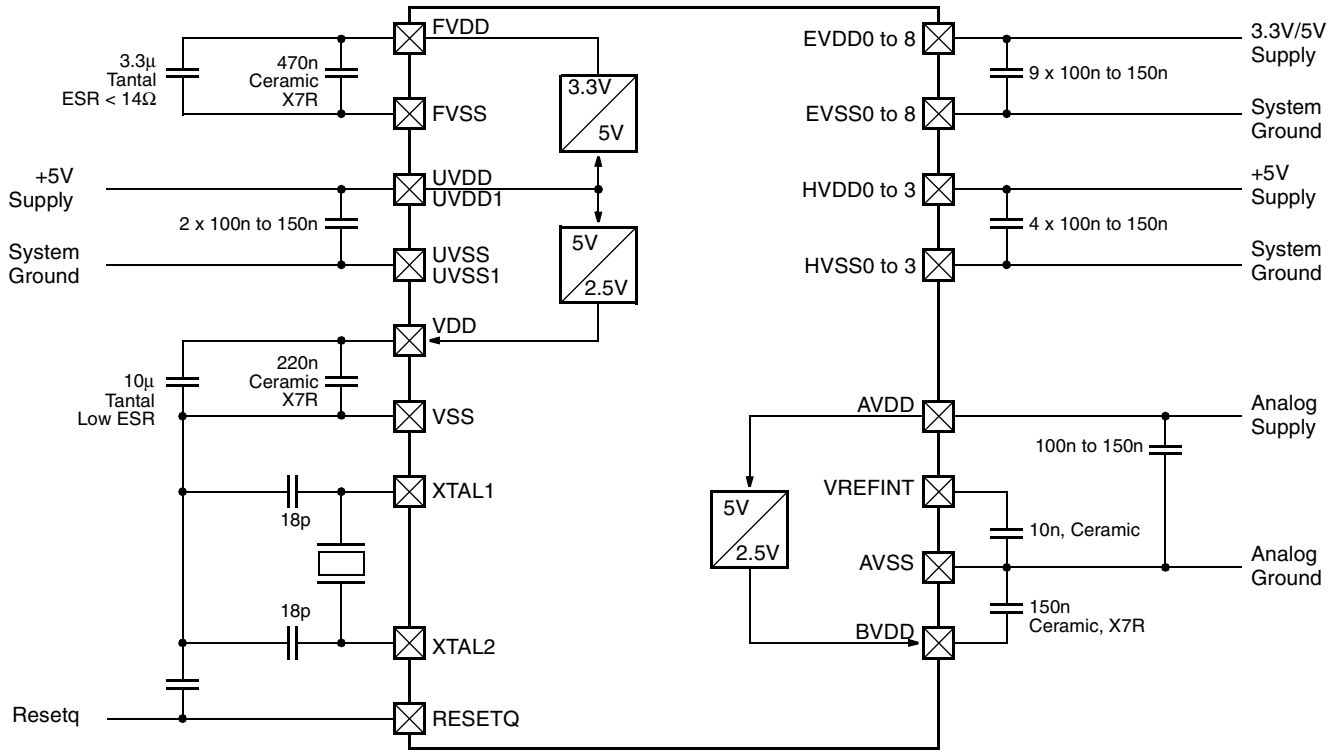


Fig. 2–3: CDC3205G-B: Recommended external supply and quartz connection.

2.6. Pin Circuits

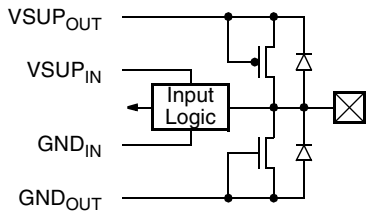


Fig. 2–4: Input Pins

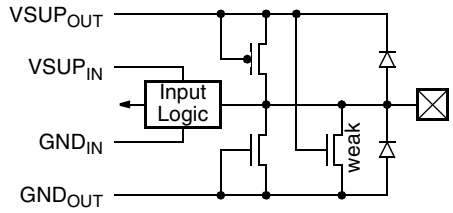


Fig. 2–5: Input Pins with Pull-Down

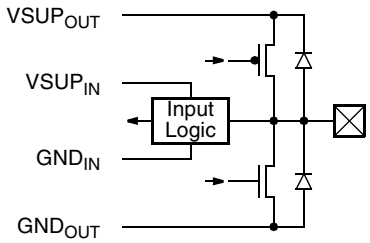


Fig. 2–6: Push Pull I/O Pins

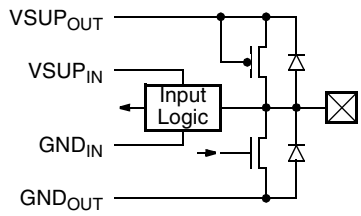


Fig. 2–7: Open Drain I/O

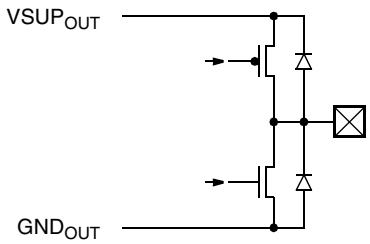


Fig. 2–8: Push Pull Output Pins

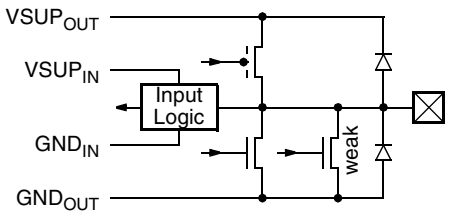


Fig. 2–9: Push Pull I/O Pins with switchable Pull-Down

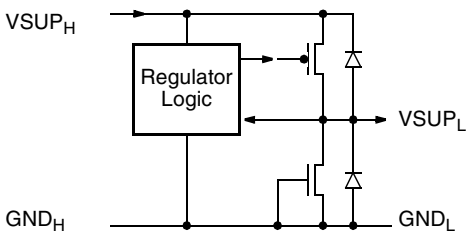


Fig. 2–10: Regulator Pins

Table 2–2: I/O Supply Catalog

Pin Names	Figure	$VSUP_{OUT}$	GND_{OUT}	$VSUP_{IN}$	GND_{IN}
XTAL1, XTAL2	2–4	UVDD	UVSS	UVDD	UVSS
WAIT		AVDD	AVSS	AVDD	AVSS
TCK, TDI, TMS		EVDD	EVSS	EVDD	EVSS
EMUTRI, ABORT, EXTERN0, EXTERN1, DBGRQ	2–5				
TEST, TEST2		UVDD	UVSS	UVDD	UVSS
U-Ports	2–6				
H-Ports		HVDD	HVSS	HVDD	HVSS
P-Ports		AVDD	AVSS	AVDD	AVSS
A31 to A0, ABE, AICU7 to 2, AMCM21 to 23, AMCS1, BWQ0 to 3, CE0Q, CE1Q, D31 to D0, DBGACK, EXTTRIG, FBUSQ, FSYS, MAS0, MAS1, nMREQ, nRESET, nTRST, nWAIT, OEQ, PIPSTAT0 to 2, SEQ, TDO, TRACECLK, TRACEPKT0 to 14, TRACESYNC		EVDD	EVSS	EVDD	EVSS
RESETQ	2–7	UVDD	UVSS	UVDD	UVSS
WAITH	2–8	AVDD	AVSS		
TRACEPKT15	2–9	EVDD	EVSS	EVDD	EVSS

Table 2–3: Regulator Pin Supply Catalog

Regulator	Figure	$VSUP_{H}$	GND_{H}	$VSUP_{L}$	GND_{L}
VDD	2–10	UVDD	UVSS	VDD	VSS
FVDD		UVDD	UVSS	FVDD	FVSS
BVDD		AVDD	AVSS	BVDD	AVSS

3. Electrical Data

3.1. Absolute Maximum Ratings

Table 3–1: $UV_{SS}=UV_{SS1}=HV_{SSn}=FV_{SS}=EV_{SSn}=AV_{SS}=0V$

Symbol	Parameter	Pin Name	Min.	Max.	Unit
V_{SUP}	Main Supply Voltage Analog Supply Voltage SM Supply Voltage Flash Port Supply Voltage	UVDD, UVDD1 AVDD HVDD0 .. HVDD3 EVDD0 .. EVDD8	-0.3	6.0	V
V_{REG}	Flash Supply Voltage	FVDD	-0.3	4.0	V
	Core Supply Voltage PLL Supply Voltage	VDD BVDD	-0.3	3.0	V
I_{SUP}	Core Supply Current Main Supply Current	VDD, VSS, UVDD, UVDD1, UVSS, UVSS1	-100	100	mA
	Flash Port Supply Current	EVDD0 .. EVDD8 EVSS0 .. EVSS8	-100	100	mA
	Analog Supply Current	AVDD, AVSS	-20	20	mA
	SM Supply Current @T_{CASE}=105C, Duty Factor=0.71 [1])	HVDD0 .. HVDD3 HVSS0 .. HVSS3	-250	250	mA
	Flash Supply Current	FDD, FVSS	-50	50	mA
	PLL Supply Current	BVDD	-20	20	mA
V_{in}	Input Voltage	U-Ports, XTAL, RESETQ, TEST, TEST2	UV_{SS}-0.5	UV_{DD}+0.7	V
		P-Ports, VREF	UV_{SS}-0.5	AV_{DD}+0.7	V
		H-Ports	HV_{SS}-0.5	HV_{DD}+0.7	V
		E-Ports	EV_{SS}-0.5	EV_{DD}+0.7	V
I_{in}	Input Current	all Inputs	0	2	mA
I_o	Output Current	U-Ports, E-Ports, RESETQ, WAITH	-5	5	mA
		H-Ports	-60	60	mA
t_{oshsl}	Duration of Short Circuit to UVSS or UVDD, Port SLOW Mode enabled	U-Ports, except in DP Mode		indefinite	s
T_j	Junction Temperature under Bias		-45	115	°C
T_s	Storage Temperature		-45	125	°C
P_{max}	Maximum Power Dissipation			0.8	W

[1]) This condition represents the worst case load with regard to the intended application

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2. Recommended Operating Conditions

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply.

Keep UV_{DD}=UV_{DD1}=AV_{DD} during all power-up and power-down sequences.

Failure to comply with the above recommendations will result in unpredictable behaviour of the device and may result in device destruction..

Table 3–2: UV_{SS}=UV_{SS1}=FV_{SS}=HV_{SSn}=EV_{SSn}=AV_{SS}=0V

Symbol	Parameter	Pin Name	Min.	Typ	Max.	Unit
V_{SUP}	Main Supply Voltage Analog Supply Voltage	UVDD=UVDD1 =AVDD	3.5	5	5.5	V
	Flash Port Supply Voltage	EVDDn	3		5.5	V
HV_{SUP}	SM Supply Voltage	HVDDn	4.75	5	5.25	V
V_{EXT}	External Flash Supply Voltage	FVDD	3	3.3	3.6	V
	External Core Supply Voltage External PLL Supply Voltage	VDD BVDD	2.25	2.5	2.75	V
dV_{DD}	Ripple, Peak to Peak	UVDD AVDD BVDD FVDD VDD			200	mV
dV_{DD}/dt	Supply Voltage Up/Down Ramping Rate	UVDD AVDD			20	V/µs
f_{XTAL}	XTAL Clock Frequency	XTAL1	4	4	5	MHz
f_{SYS}	CPU Clock Frequency, PLL on		For a list of available settings see Tables 4–5 and 4–6.			
f_{BUS}	Program Storage Clock Frequency, PLL on					
V_{il} (see Table 2-2 for a list of input types and their supply voltages)	Automotive Low Input Voltage	U-Ports H-Ports P-Ports			$0.5*xV_{DD}$	V
	CMOS Low Input Voltage	U-Ports, TEST, TEST2 H-Ports P-Ports			$0.3*xV_{DD}$	V
	TTL Low Input Voltage	E-Ports			0.8	V
V_{ih} (see Table 2-2 for a list of input types and their supply voltages)	Automotive High Input Voltage	U-Ports H-Ports P-Ports	$0.86*xV_{DD}$			V
	CMOS High Input Voltage	U-Ports,TEST, TEST2 H-Ports P-Ports	$0.7*xV_{DD}$			V
	TTL High Input Voltage	E-Ports	2.2			V
RV_{il}	Reset Active Input Voltage	RESETQ			0.75	V
RV_{im}	Reset Inactive and Alarm Active Input Voltage	RESETQ	1.5		2.3	V
RV_{ih}	Reset Inactive and Alarm Inactive Input Voltage	RESETQ	3.2			V

Table 3–2: $UV_{SS}=UV_{SS1}=FV_{SS}=HV_{SSn}=EV_{SSn}=AV_{SS}=0V$

Symbol	Parameter	Pin Name	Min.	Typ	Max.	Unit
V_{REFi}	Ext. ADC Reference Input Voltage	VREF	2.56		AV_{DD}	V
PV_i	ADC Port Input Voltage referenced to ext. VREF Reference	P-Ports	0		V_{REF}	V
	ADC Port Input Voltage referenced to int. VREFINT Reference		0		V_{REFINT}	

3.3. Characteristics

Table 3–3: $UV_{SS}=UV_{SS1}=FV_{SS}=HV_{SSn}=EV_{SSn}=AV_{SS}=0V$, $3.5V<AV_{DD}=UV_{DD}=UV_{DD1}<5.5V$, $4.75V<HV_{DDn}<5.25V$, $3V<EV_{DDn}<5.5V$, $T_{CASE}=0$ to +70C, $f_{XTAL}=5MHz$, external components according to Fig. 2–3 (unless otherwise noted)

Symbol	Parameter	Pin Name	Min.	Typ [1]	Max.	Unit	Test Conditions
Package							
R_{thjc}	Thermal Resistance from Junction to Case			15		C/W	
Supply Currents (CMOS levels on all inputs, i.e. $V_{il}=xV_{SS}\pm0.3V$ and $V_{ih}=xV_{DD}\pm0.3V$, no loads on outputs)							
UI_{DDp}	UVDD PLL Mode Supply Current	UVDD+ UVDD1			35	mA	f_{SYS}=24MHz, ETM off
UI_{DDpe}	UVDD PLL Mode Supply Current	UVDD+ UVDD1			45	mA	f_{SYS}=24MHz, ETM on
UI_{DDf}	UVDD FAST Mode Supply Current	UVDD+ UVDD1			10	mA	all Modules OFF, [2]
UI_{DDs}	UVDD SLOW Mode Supply Current	UVDD+ UVDD1			1.2	mA	all Modules OFF, [2] [6]
UI_{DDd}	UVDD DEEP SLOW Mode Supply Current	UVDD+ UVDD1			0.7	mA	all Modules OFF, [6]
AI_{DDa}	AVDD Active Supply Current	AVDD		0.35	0.6	mA	ADC ON, PLL OFF
				1	2	mA	ADC, Buffer and PLL ON, f_{SYS}=24MHz
AI_{DDq}	Quiescent Supply Current	AVDD			10	µA	ADC and PLL OFF
EI_{DDq}		EVDDn			10	µA	no Output Activity
HI_{DDq}		Sum of all HVDDn			40	µA	no Output Activity, SM Module OFF

[1] Typical values describe typical behaviour at room temperature (25C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).

Table 3–3: $UV_{SS}=UV_{SS1}=FV_{SS}=HV_{SSn}=EV_{SSn}=AV_{SS}=0V$, $3.5V<AV_{DD}=UV_{DD}=UV_{DD1}<5.5V$, $4.75V<HV_{DDn}<5.25V$, $3V<EV_{DDn}<5.5V$, $T_{CASE}=0$ to +70C, $f_{XTAL}=5MHz$, external components according to Fig. 2–3 (unless otherwise noted)

Symbol	Parameter	Pin Name	Min.	Typ [1]	Max.	Unit	Test Conditions
Inputs							
V_{ilha}	Automotive Input Low to High Threshold Voltage	U-Ports H-Ports P-Ports	0.68* xV_{DD}	0.76* xV_{DD}	0.84* xV_{DD}	V	$4.5V<xV_{DD}<5.5V$, [3] (see Table 2-2 for a list of input types and their supply voltages)
V_{ihla}	Automotive Input High to Low Threshold Voltage		0.53* xV_{DD}	0.61* xV_{DD}	0.69* xV_{DD}	V	
V_{ilha}-V_{ihla}	Automotive Input Hysteresis		0.1* xV_{DD}	0.15* xV_{DD}	0.2* xV_{DD}	V	
V_{ilhc}	CMOS Input Low to High Threshold Voltage	U-Ports H-Ports P-Ports TEST, TEST2	0.5* xV_{DD}	0.6* xV_{DD}	0.7* xV_{DD}	V	$4.5V<xV_{DD}<5.5V$, [3] (see Table 2-2 for a list of input types and their supply voltages)
V_{ihlc}	CMOS Input High to Low Threshold Voltage		0.3* xV_{DD}	0.4* xV_{DD}	0.5* xV_{DD}	V	
V_{ilhc}-V_{ihlc}	CMOS Input Hysteresis		0.1* xV_{DD}	0.2* xV_{DD}	0.3* xV_{DD}	V	
I_i	Input Leakage Current	U-Ports H-Ports P-Ports P06, WAIT VREF E-Ports	-1 -10 -1 -0.2 -1 -1		1 10 1 0.2 1 1	µA	$0<V_i<UV_{DD}$ $0<V_i<HV_{DD}$ $0<V_i<AV_{DD}$ $0<V_i<AV_{DD}$ $0<V_i<AV_{DD}$ $0<V_i<EV_{DD}$
I_{pd}	Input Pull-Down Current	TEST, TEST2 E-Ports	10 10	100 100	220 220	µA	$V_i=UV_{DD}$ $V_i=EV_{DD}$, when unused
I_{pu}	Input Pull-Up Current	E-DB	-220	-100	-10	µA	$V_i=0$, when unused
Outputs ($4.5V<UV_{DD}=EV_{DD}<5.5V$)							
V_{ol}	Port Low Output Voltage	U-Ports, E-Ports RESETQ			0.4	V	$I_o=2mA$
		H-Ports	0.125		0.45	V	$I_o=27mA$ $I_o=40mA@T_{CASE}=-40C$ $I_o=30mA@T_{CASE}=25C$
ΔV_{ol}	Spread of V_{ol} Values within one SM Driver Module	H-Ports	-50		50	mV	
V_{oh}	Port High Output Voltage	U-Ports E-Ports	UV_{DD}-0.4 EV_{DD}-0.4			V	$I_o=-2mA$
		H-Ports	HV_{DD}-0.55		HV_{DD}-0.125	V	$I_o=-27mA$ $I_o=-40mA@T_{CASE}=-40C$ $I_o=-30mA@T_{CASE}=25C$
ΔV_{oh}	Spread of V_{oh} Values within one SM Driver Module	H-Ports	-50		50	mV	

[1] Typical values describe typical behaviour at room temperature (25C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).

Table 3–3: UV_{SS}=UV_{SS1}=FV_{SS}=HV_{SSn}=EV_{SSn}=AV_{SS}=0V, 3.5V<AV_{DD}=UV_{DD}=UV_{DD1}<5.5V, 4.75V<HV_{DDn}<5.25V, 3V<EV_{DDn}<5.5V, T_{CASE}=0 to +70C, f_{XTAL}=5MHz, external components according to Fig. 2–3 (unless otherwise noted)

Symbol	Parameter	Pin Name	Min.	Typ [1]	Max.	Unit	Test Conditions
dV_{oH}/dt	H-Port Slew Rate with Inductive Load	H-Ports	by first order approximation defined by the quotient of the inductive load current and the external capacitances on the port pin			V/ns	
LV_{ol}	LCD Port Zero Output Voltage	U-Ports	-0.05		0.05	V	no load
LV_{o1}	LCD Port Low Output Voltage	U-Ports	1/3 *UV_{DD} -0.05		1/3 *UV_{DD} +0.05	V	no load
LV_{o2}	LCD Port High Output Voltage	U-Ports	2/3 *UV_{DD} -0.05		2/3 *UV_{DD} +0.05	V	no load
LV_{oh}	LCD Port Full Output Voltage	U-Ports	UV_{DD} - 0.05		UV_{DD} +0.05	V	no load
ΣLI_{o1}	Internal LCD-Low Supply Short Circuit Current	U-Ports	0.3		-0.3	mA	Pin Short to 2/3*UV_{DD} Pin Short to UV_{SS}
ΣLI_{o2}	Internal LCD-High Supply Short Circuit Current	U-Ports	0.3		-0.3	mA	Pin short to UV_{DD} Pin short to 1/3*UV_{DD}
I_{shf}	Port FAST Short Circuit Current	U-Ports		14	23	mA	Pin Short to UV_{DD} or UV_{SS}, Port FAST Mode
I_{shs}	Port SLOW Short Circuit Current	U-Ports		3.7	5.5	mA	Pin Short to UV_{DD} or UV_{SS}, Port SLOW Mode
I_{shsd}	Port SLOW Short Circuit Current, DP Mode	U-Ports		7.5	11	mA	Pin Short to UV_{DD}, Port SLOW and Double Pull-Down Modes
References and Comparators, AVDD Section							
V_{REFINT}	VREFINT Generator Reference Output Voltage	VREFINT	2.38		2.51	V	External load current < 1uA
t_{REFINT}	VREFINT Generator Setup Time after Power-Up on AV_{DD}, or on leaving SLOW or DEEP SLOW mode	VREFINT			500	µs	
V_{REFP06}	P06 Comparator Reference Voltage	P06	0.49* AV_{DD}		0.51* AV_{DD}	V	
$P06V_{lh}$-$P06V_{hl}$	P06 Comparator Hysteresis, symmetrical to V_{REFP06}	P06	0.02 * AV_{DD}		0.05 * AV_{DD}	V	[3]
V_{REFW}	WAIT Comparator Reference Voltage	WAIT	0.98* V_{REFINT}		1.02* V_{REFINT}	V	
VW_{ol}	WAIT Comparator Low Output Voltage	WAITH			0.4	V	4.5V<xV_{DD}<5.5V I_o=50uA

[1] Typical values describe typical behaviour at room temperature (25C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).

Table 3–3: UV_{SS}=UV_{SS1}=FV_{SS}=HV_{SSn}=EV_{SSn}=AV_{SS}=0V, 3.5V<AV_{DD}=UV_{DD}=UV_{DD1}<5.5V, 4.75V<HV_{DDn}<5.25V, 3V<EV_{DDn}<5.5V, T_{CASE}=0 to +70C, f_{XTAL}=5MHz, external components according to Fig. 2–3 (unless otherwise noted)

Symbol	Parameter	Pin Name	Min.	Typ [1]	Max.	Unit	Test Conditions
VW_{oh}	WAIT Comparator High Output Voltage	WAITH	AV_{DD}-0.4V			V	4.5V<xV_{DD}<5.5V I_o=-50uA
t_{ACDEL}	P06, WAIT Comparator Delay Time	P06 WAIT			1	µs	Overdrive=50mV
References and Comparators, UVDD Section							
V_{BG}	VBG Generator Reference Output Voltage		2.25	2.5	2.75	V	
V_{REFR}	RESET Comparator Reference Voltage	RESETQ	0.45* V_{BG}		0.45* V_{BG}	V	
RV_{lh}-RV_{hl}	RESET Comparator Hysteresis, symmetrical to V_{REFR}	RESETQ	0.25		0.375	V	[3]
V_{REFA}	ALARM Comparator Reference Voltage	RESETQ	1.1* V_{BG}		1.1* V_{BG}	V	
AV_{lh}-AV_{hl}	ALARM Comparator Hysteresis, symmetrical to V_{REFA}	RESETQ	0.1		0.2	V	[3]
V_{REFPOR}	UV_{DD} Power On Reset Threshold	UVDD	1.125* V_{BG}		1.125* V_{BG}	V	
t_{UCDEL}	RESET, ALARM, Comparator Delay Time	RESETQ			1	µs	Overdrive=50mV
References and Comparators, HVDD Section							
V_{REFSM}	SM Comparator Reference Voltage	H00, H04, H20, H24, H32, H40, H70	1/9* HV_{DD} -0.07		1/9* HV_{DD} +0.07	V	
t_{HCDEL}	SM Comparator Delay Time	H00, H04, H20, H24, H32, H40, H70			100	ns	Overdrive=50mV
VDD Regulator							
V_{DD_ro}	Regulator Output Voltage	VDD	1.02* V_{BG} -30mV		1.02* V_{BG} +30mV	V	DEEP SLOW Mode
			1.02* V_{BG} - 105mV		1.02* V_{BG} - 0mV	V	PLL Mode, f_{SYS}=50MHz
I_{DD_rlim}	Regulator Internal Output Current Limit	VDD	120	275	460	mA	
t_{VDD_su}	Regulator Setup Time after Power-Up on UVDD	VDD		120	400	µs	FAST Mode

[1] Typical values describe typical behaviour at room temperature (25C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).

Table 3–3: UV_{SS}=UV_{SS1}=FV_{SS}=HV_{SSn}=EV_{SSn}=AV_{SS}=0V, 3.5V<AV_{DD}=UV_{DD}=UV_{DD1}<5.5V, 4.75V<HV_{DDn}<5.25V, 3V<EV_{DDn}<5.5V, T_{CASE}=0 to +70C, f_{XTAL}=5MHz, external components according to Fig. 2–3 (unless otherwise noted)

Symbol	Parameter	Pin Name	Min.	Typ [1]	Max.	Unit	Test Conditions
BVDD Regulator							
BV_{DD_ro}	Regulator Output Voltage	BVDD	$V_{RE-FINT}$ -25mV		$V_{RE-FINT}$ +25mV	V	PLLC.PMF > 0
BI_{DD_rlim}	Regulator Internal Output Current Limit	BVDD	17	40	70	mA	PLLC.PMF > 0
t_{BVDD_su}	Regulator Setup Time after setting PLLC.PMF > 0	BVDD		70	230	µs	
FVDD Regulator							
$FV_{DD\_}ro$	Regulator Output Voltage	FVDD	V_{BG} *1.34 -40mV		V_{BG} *1.34 +40mV	V	no load
			V_{BG} *1.34 -170m		V_{BG} *1.34 -40mV	V	I_{FVDD}=-40mA
$FI_{DD\_}rl_{im}$	Regulator Internal Output Current Limit	FVDD	52	120	200	mA	
t_{FVDD_su}	Regulator Setup Time after Power-Up on UV_{DD}	FVDD		100	330	µs	I_{FVDD}=-40mA
ADC (conversion reference V_{REFC} either equal to external reference V_{REF} or internal reference V_{REFINT})							
LSB	LSB Value			V_{REFC} /1024		V	
INL	Integral Non-Linearity: difference between the output of an actual ADC and the line best fitting the output function (best-fit line)		-2.5		2.5	LSB	2.4V<V_{REFC}<AV_{DD}, 4.5V<AV_{DD}<5.5V
ZE	Zero Error: difference between the output of an ideal and an actual ADC for zero input voltage		-1		1	LSB	2.4V<V_{REFC}<AV_{DD}, 4.5V<AV_{DD}<5.5V
FSE	Full-Scale Error: difference between the output of an ideal and an actual ADC for full-scale input voltage		-1		1	LSB	2.4V<V_{REFC}<AV_{DD}, 4.5V<AV_{DD}<5.5V
TUE	Total Unadjusted Error: maximum sum of integral non-linearity, zero error and full-scale error		-3.5		3.5	LSB	2.4V<V_{REFC}<AV_{DD}, 4.5V<AV_{DD}<5.5V
QE	Quantization Error: uncertaincy because of ADC resolution		-0.5		0.5	LSB	2.4V<V_{REFC}<AV_{DD}, 4.5V<AV_{DD}<5.5V

[1] Typical values describe typical behaviour at room temperature (25C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).

Table 3–3: UV_{SS}=UV_{SS1}=FV_{SS}=HV_{SSn}=EV_{SSn}=AV_{SS}=0V, 3.5V<AV_{DD}=UV_{DD}=UV_{DD1}<5.5V, 4.75V<HV_{DDn}<5.25V, 3V<EV_{DDn}<5.5V, T_{CASE}=0 to +70C, f_{XTAL}=5MHz, external components according to Fig. 2–3 (unless otherwise noted)

Symbol	Parameter	Pin Name	Min.	Typ [1]	Max.	Unit	Test Conditions
AE	Absolute Error: difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included		-4		4	LSB	2.4V<V_{REFC}<AV_{DD}, 4.5V<AV_{DD}<5.5V
R	Conversion Range	P-Ports	AV_{SS}		V_{REFC}	V	2.4V<V_{REFC}<AV_{DD}
A	Conversion Result			INT (V_{in}/ LSB)		hex	AV_{SS}<V_{in}<V_{REFC}
			000			hex	V_{in}<=AV_{SS}
					3FF	hex	V_{in}>=V_{REFC}
t_c	Conversion Time		4			µs	T_{SAMP}=0, f_{IO}=10MHz
t_s	Sample Time		2			µs	
C_i	Internal Sampling Capacitance during Sampling Period			7.5 2.5		pF	Buffer off Buffer on
R_i	Internal Serial Resistance during Sampling Period			7		kOhm	Buffer off
PLL and ERM							
t_{SUPLL}	PLL Locking Time				100	µs	@f_{XTAL}=4 MHz, f_{SYS}=16MHz
dt_{PLL}	I/O Clock Uncertainty due to PLL Jitter, short term and long term			±2.5		ns	ERM off
dt_{ERM}	I/O Clock Modulation due to ERM action, short term and long term		0 0 0		7.5 12.5 20	ns	ERM on, WEAK setting ERM on, NORMAL setting ERM on, STRONG setting
Clock Supervision							
F_{SUP}	Clock Supervision Threshold Frequency	XTAL1	70		350	kHz	
SPI (Fig. 3–1, Fig. 3–2)							
t_{soci}	Data out Setup Time with internal clock	SPI-D-OUT			60 [4]	ns	@C_l=30pF, Port FAST mode
t_{hoci}	Data out Hold Time with internal clock	SPI-D-OUT	-60		60 [4]	ns	@C_l=30pF, Port FAST mode
t_{soce}	Data out Setup Time with external clock	SPI-D-OUT			3/ f_{IO} +60 [4]	ns	@C_l=30pF, Port FAST mode

[1] Typical values describe typical behaviour at room temperature (25C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).

Table 3–3: UV_{SS}=UV_{SS1}=FV_{SS}=HV_{SSn}=EV_{SSn}=AV_{SS}=0V, 3.5V<AV_{DD}=UV_{DD}=UV_{DD1}<5.5V, 4.75V<HV_{DDn}<5.25V, 3V<EV_{DDn}<5.5V, T_{CASE}=0 to +70C, f_{XTAL}=5MHz, external components according to Fig. 2–3 (unless otherwise noted)

Symbol	Parameter	Pin Name	Min.	Typ [1]	Max.	Unit	Test Conditions
t_{hoce}	Data out Hold Time with external clock	SPI-D-OUT	2/ f_{IO} - 60			ns	@C_l=30pF, Port FAST mode
t_{si}	Data in Setup Time with external clock	SPI-D-IN	1/ f_{IO}+60 [4]			ns	
t_{hi}	Data in Hold Time with external clock	SPI-D-IN	1/ f_{IO}+60 [4]			ns	
CAN (Fig. 3–3)							
t_{srx}	rx-strobe Time	CAN rx	0		10 [4]	ns	reference is XTAL1 rising edge
t_{dtx}	tx-drive Time	CAN tx	15		60 [4]	ns	reference is XTAL1 falling edge @C_l=30pF, Port FAST mode
DIGITbus (Fig. 3–4)							
t_{btj}	Bit Time jitter	DIGIT-OUT			±10 [4]	ns	rising edges, internal clock master
t_{fed}	Falling edge delay	DIGIT-OUT	15 [5]		t_{BIT}/64 +60 [4]	ns	reference is nominal falling edge

[1] Typical values describe typical behaviour at room temperature (25C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).

[2]) Value may be exceeded with unusual Hardware Option setting

[3]) Design value only, the actually observable hysteresis may be lower due to system activity and related supply noise

[4]) When ERM is active, this time value is increased by 7.5ns with WEAK ERM setting, by 12.5ns with NORMAL ERM setting and by 20ns with STRONG ERM setting.

[5]) When ERM is active, this time value is decreased by 7.5ns with WEAK ERM setting, by 12.5ns with NORMAL ERM setting and by 20ns with STRONG ERM setting.

[6]) Measured with external clock. Add 120µA for operation on typical quartz with SR0.XTAL=0 (Oscillator RUN mode).

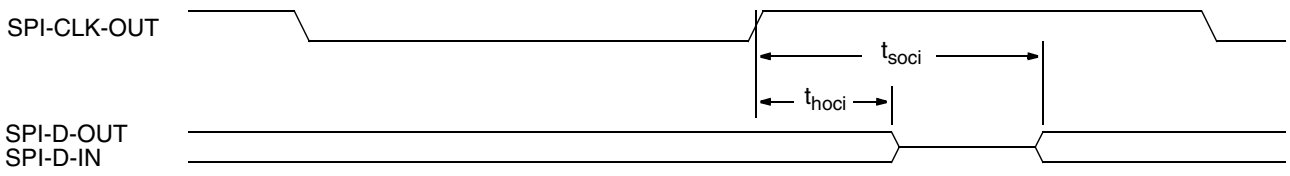


Fig. 3–1: SPI: Send and Receive Data with Internal Clock. Timing is valid for inverted clock too (Data valid at positive edge).

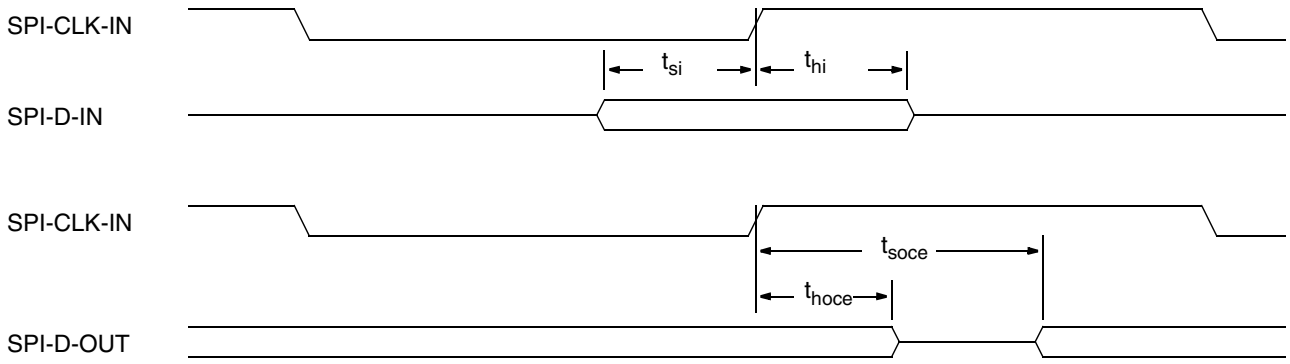


Fig. 3–2: SPI: Send and Receive Data with External Clock. Timing is valid for inverted clock too (Data valid at positive edge).

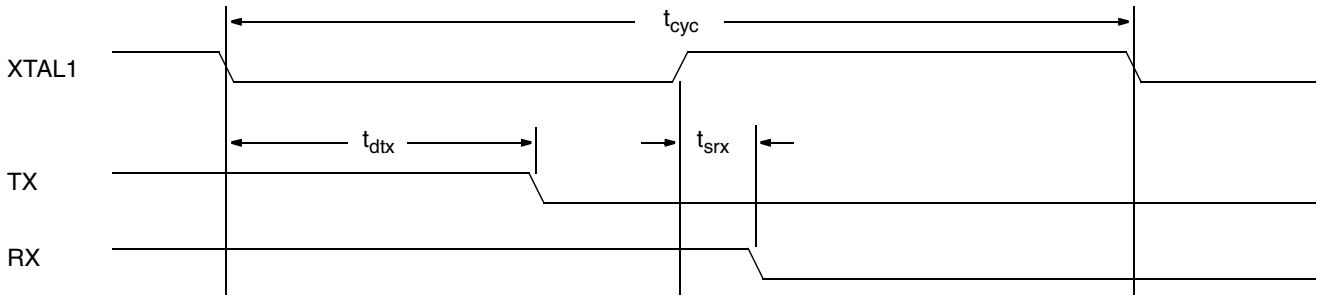
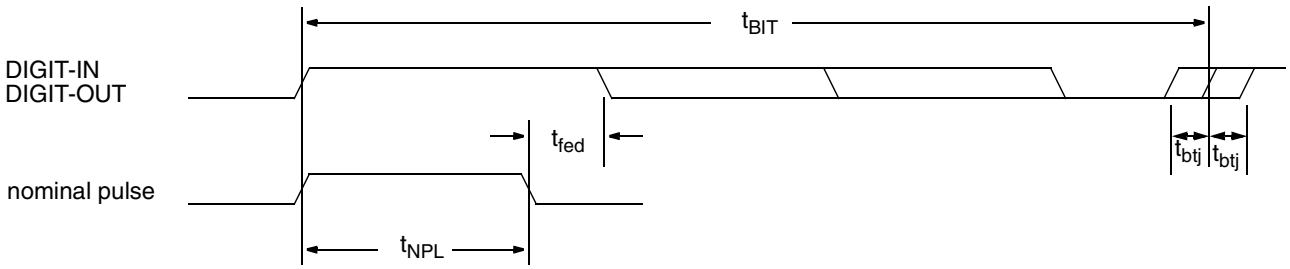


Fig. 3–3: CAN I/O Timing.



t_{NPL}: Nominal programmed Pulse Length. Depends on programmed phase, Baudrate and transmitted sign (0, 1, T). Should be 1/4 for sign 0, 1/2 for sign 1 and 3/4 for sign T of t_{BIT}.

Fig. 3–4: DIGITbus I/O Timing

3.4. Recommended Quartz Crystal Characteristics

Table 3–4: 3.5V<UV_{DD}<5.5V, external components according to Fig. 2–3, unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
f_P	Parallel Resonance Frequency @ C_L=12pF	4		5	MHz	
R_1	Series Resonance Res. for 50ms Oscillation Start-Up Time and Proper Function @ C_L=12pF					
	@ f_P=4MHZ			340	Ohm	START-UP
				380		START-UP, 4.5V<UV_{DD}<5.5V
				210		RUN
				270		RUN, 4.5V<UV_{DD}<5.5V
	@ f_P=5MHz			240		START-UP
				280		START-UP, 4.5V<UV_{DD}<5.5V
				140		RUN
				180		RUN, 4.5V<UV_{DD}<5.5V
C_{EXT}	External Oscillation Capacitances, connected to V_{SS}		18		pF	

4. CPU and Clock System

4.1. ARM7TDMI™ CPU

The CPU is an ARM7TDMI 32-bit RISC processor. This is a member of the Advanced RISC Machines (ARM) family. The ARM7TDMI is a 3 stage pipeline machine and supports a 4 Gbit address range. Besides the 32bit standard ARM instruction set the ARM7TDMI supports the 16bit Thumb instruction set which allows a higher code density. It includes a 64bit result multiplier and a JTAG interface with an embedded debug module.

4.1.1. CPU States

The ARM7TDMI CPU allows operation in two states:

– ARM state: 32bit instructions

– Thumb state: 16bit instructions

After reset and exceptions, ARM state is active.

4.2. CPU Modes

The CPU can be operated in four different clock modes (Table 4–2). Core modules that are also affected by CPU speed modes are:

1. Interrupt Controller with all internal and external interrupts

2. RAM, ROM/Flash and DMA

3. Watchdog

Table 4–1 shows the operability of the peripheral modules in the various clock modes.

4.2.1. FAST Mode

After reset the CPU is in FAST mode. The CPU clock and the I/O clock both equal the oscillator frequency f_{XTAL}.

Internal clock frequencies higher than f_{XTAL} are not available in this mode. Modules requiring $f_0 = 2f_{XTAL}$ for operation will not work properly, as f_0 is set to $f_1 = f_{XTAL}$.

Returning CPU from any other mode to FAST mode is done by selecting the appropriate mode in the standby registers field SR1.CPUM (Table 4–2).

4.2.2. PLL Modes

To increase CPU performance, a PLL allows to multiply f_{XTAL}. The CPU will operate at this higher frequency f_{SYS} and its speed is automatically reduced only for accesses to slower modules (ROM/Flash, I/O).

Table 4–5 gives recommended settings for control registers and the various resulting operating frequencies for the PLL mode. These recommended settings achieve $f_0 = 2*f_{XTAL}$, $f_1 = f_{XTAL}$ and so forth, for unlimited operation of peripheral modules.

A PLL2 mode allows bypassing of the first stage of the divider chain. It allows a clock system with $f_{SYS} = n*f_{XTAL}$ and $f_0 = f_1 = f_{XTAL}$ for special applications, where the unlimited operation of peripheral circuits has to be sacrificed (see Table 4–6 for settings).

In both PLL modes, the EMI Reduction Module (ERM) can be operated, which reduces electromagnetic energy emission (see Section 4.4. on page 40).

Activating the PLL modes is done in FAST mode by the following routine:

1. For initialization, choose a pair of settings for the clock multiplication factor and the clock prescaler from Tables 4–5 or 4–6 and write them to PLLC.PMF and IOC.IOP.

2. When coming from SLOW or DEEP SLOW mode, allow t_{REFINT} to elapse for VREFINT and BVDD to set up. In all other cases, wait the time of t_{BVDD_su} for BVDD to set up.

3. Wait for at least t_{SUPLL} before checking PLLC.LCK to be set, to make sure that the PLL has locked.

4. Disable ICU and DMA, if active.

5. Enable PLL mode by writing 0x03, or PLL2 mode by writing 0x07 to SR1.CPUM (32-bit access only).

6. As the System Frequency Divider and the Prescaler need some time to synchronize, the PLL mode is not active until PLLC.PLLM reads as 1.

7. At this point the ERM may be activated (see Section 4.4.3. on page 40) and ICU and DMA may be (re-)enabled.

Returning to FAST mode is done by the following routine:

1. Deactivate the ERM, if active (see Section 4.4.4. on page 40).

2. Disable ICU and DMA, if active.

3. Return to FAST mode by setting SR1.CPUM to 0x01 (32-bit access only).

4. Wait for PLLC.PLLM to read as 0.

5. Now the ICU and DMA may be (re-)enabled and the program may resume.

Attention: The PLL modes must be entered and left only via FAST mode. The registers PLLC.PMF and IOC.IOP may only be changed in FAST mode.

To reduce the power consumption in other modes than PLL modes, the registers PLLC.PMF and IOC.IOP should be programmed to zero.

4.2.3. SLOW Mode

To considerably reduce power consumption, the user can reduce the internal CPU clock frequency to 1/128 of the nor-

Table 4–1: CPU-Active Modes and their effect on peripheral modules

Module	PLL	PLL2	FAST	SLOW	DEEP SLOW
Core					
Digital Watchdog	✔	✔	✔	✔	✔
IRQ Interrupt Controller Unit	✔	✔	✔	✔	✔
FIQ Interrupt Logic	✔	✔	✔	✔	✔
Port Interrupts	✔	✔	✔	✔	✔
Analog					
A/D Converter	✔	✔ 1)	✔ 1)	✔ 1)	
ALARM, P06 and WAIT Comparators	✔	✔	✔	✔	✔
LCD Module	✔	✔ 1)	✔ 1)	✔ 1)	✔ 3)
Communication					
DMA	✔	✔	✔	✔	✔
DMA Timer, GBus	✔	✔ 1)	✔ 1)	✔ 1)	✔ 3)
UART	✔	✔ 1)	✔ 1)	✔ 1)	
SPI	✔	✔ 1)	✔ 1)	✔ 1)	
CAN	✔	✔ 1)	✔ 1)	✔ 1) 4)	
DIGITbus	✔	✔ 1)	✔ 1)	✔ 1) 4)	✔ 3) 4)
I^2C	✔	✔	✔	✔	
Input & Output					
Ports	✔	✔	✔	✔	✔
Stepper Motor Module	✔	✔ 1)	✔ 1)		
PWM	✔	✔ 1)	✔ 1)	✔ 1)	
PFM	✔	✔ 1)	✔ 1)	✔ 1)	✔ 3)
Audio Module	✔	✔ 1)	✔ 1)		
Clock Outputs	✔	✔ 1)	✔ 1)	✔ 1)	✔ 3)
Timers & Counters					
Capture Compare Module	✔	✔ 1)	✔ 1)	✔ 2)	✔ 3) 4)
Timers	✔	✔ 1)	✔ 1)	✔ 1)	✔ 3)
Miscellaneous					
JTAG	✔	✔	✔	✔	✔
Embedded Trace Module	✔	✔	✔	✔	✔

1) Possibly affected by f_0 equaling f_1
2) Avoid write access to CCxI
3) Only clocks f5 and slower are available from Clock Divider
4) Don't access registers or CAN RAM

mal f_{XTAL} value. In this CPU SLOW mode, program execution is reduced to 1/128 of f_{XTAL}.

Some modules must not be operated during CPU SLOW mode (e.g. CAN). Refer to module sections for details (see Table 4–1 on page 36).

Internal clock frequencies higher than f_{XTAL} are not available in this mode. Modules requiring $f_0 = 2*f_{XTAL}$ for operation will not work properly, as f_0 is set to $f_1 = f_{XTAL}$.

For switching between SLOW and FAST modes, use the following routine:

1. Select the desired mode in the standby registers field CPUM (Table 4–2). The new f_{BUS} is effective after 2 f_{XTAL} cycles at most.

2. Now the program may resume.

4.2.4. DEEP SLOW Mode

To further reduce power consumption beyond SLOW mode, DEEP SLOW mode also disables most of the internal peripheral clocking system. Table 4–1 shows which peripheral modules can be operated in DEEP SLOW mode.

Only peripheral module clocks f_5 and slower are available from the divider chain. T0 can be operated only with this limitation.

For switching between DEEP SLOW and FAST modes, use the routine given for SLOW mode.

4.3. Clock System

The IC contains a quartz oscillator circuit that only requires external connection of a quartz and of 2 oscillation capacitors. Its start-up and run properties are controllable by SW. See section “Core Logic” for details.

The oscillator clock f_{XTAL} drives a clock system that supplies the various modules with its specific clock.

A frequency multiplying PLL allows to select the system clock f_{SYS} to be higher than f_{XTAL} for high speed CPU and module operation.

A divider chain divides f_{IO} down to supply peripheral module clocks f_0 to f_{17}. Module clock selection is software defined in some cases, hardware or HW option defined in other cases. The module descriptions give details.

The standby register field SR1.CPUM selects the CPU mode (Table 4–2).

Table 4–2: Clock Selection

SR1.CPUM			CPU Mode	f_{BUS}	f_{IO}	f_0	f_1
0	0	0	SLOW	f_{XTAL}/128	f_{XTAL}/128	f_{XTAL}	f_{XTAL}
0	0	1	FAST	f_{XTAL}	f_{XTAL}	f_{XTAL}	f_{XTAL}
0	1	0	DEEP SLOW	f_{XTAL}/128	f_{XTAL}/128	f0 to f4 = 0	
0	1	1	PLL	n f_{XTAL}	n/m f_{XTAL}	n/m f_{XTAL}	n/2m f_{XTAL}
1 1	0 1	x 0	Don’t use				
1	1	1	PLL2	n f_{XTAL}	n/m f_{XTAL}	n/m f_{XTAL}	n/m f_{XTAL}

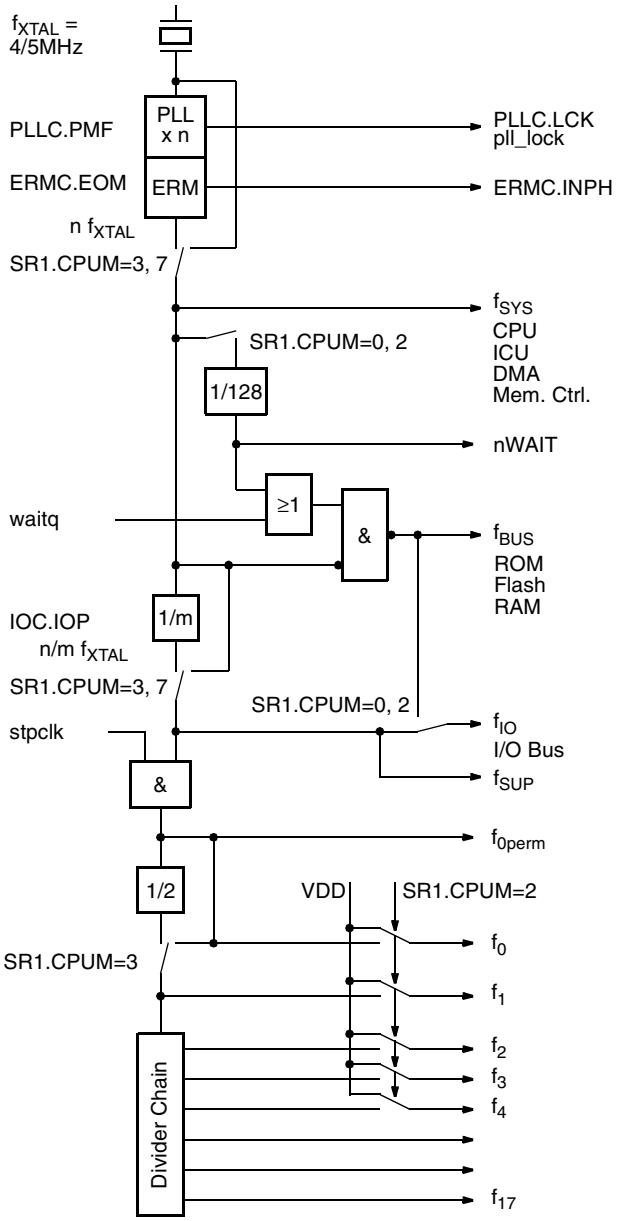


Fig. 4–1: Clock System

4.3.1. PLL

The PLL is composed of a Phase Comparator, a Voltage Controlled Oscillator VCO, a Frequency Divider and an internal bypass. The Phase Comparator compares the input frequency f_{XTAL} with the output frequency of the Frequency Divider, f_{REF}. It outputs the voltage V_P, which is proportional to the phase difference of the two input frequencies. V_P controls the VCO which outputs the desired frequency. This frequency is fed back by the Frequency Divider to the Phase Comparator. The Frequency Divider divides the input frequency down to f_{REF} which ideally is the same as f_{XTAL}.

The phase-locked state of the PLL is signaled by a lock signal. It is available as flag PLLC.LCK. It may be routed to the LCK special output by selection in field ANAU.LS (UVDD Analog Section).

The block multiplies f_{XTAL} by n = PMF+1 to achieve f_{SYS}. PLL Control register PLLC allows to set the desired value.

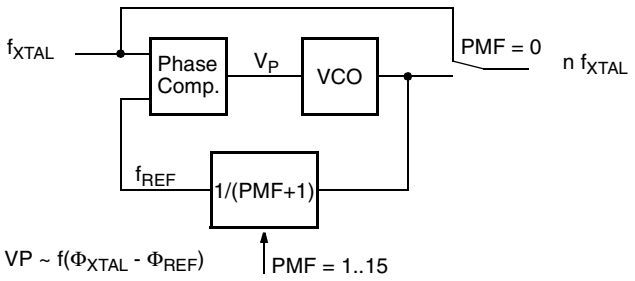


Fig. 4–2: PLL Block Diagram

4.3.2. I/O Clock Prescaler

This prescaler derives the clock for the peripheral modules (the I/O clock f_{IO}) from the system clock f_{SYS}. It divides f_{SYS} by an integer number m. I/O Clock Control register IOC allows to set the desired value. m is recommended to be set equal to n/2.

4.3.3. Divider Chain and Clock Outputs CO0 and CO1

The peripheral module divider chain receives f_{SYS}/m and supplies the various modules with their specific clocks. Each stage of the divider chain divides its input clock by two. Thus only powers of two of the divider chain input clock are obtainable for the peripheral modules.

Table 4–2 shows the effect of CPU mode selection on the divider output frequencies f_0 through f_{17}. Note that in modes FAST, PLL and SLOW, with n = 2m (which is recommended), f_1 always equals f_{XTAL}. Thus f1 and all further subdivided clocks are unaffected by switching between these modes.

Section “HW Options” gives details about HW option controlled clocks, their selection and their activation.

Note that specifying 1/1.5 and 1/2.5 prescaled clocks result in clock signals with 33% resp. 20% duty factor.

Two Clock Output signals CO0 and CO1 provide external visibility of internal clocks (Figure 4–3). Clocks are selected by register CO0SEL.

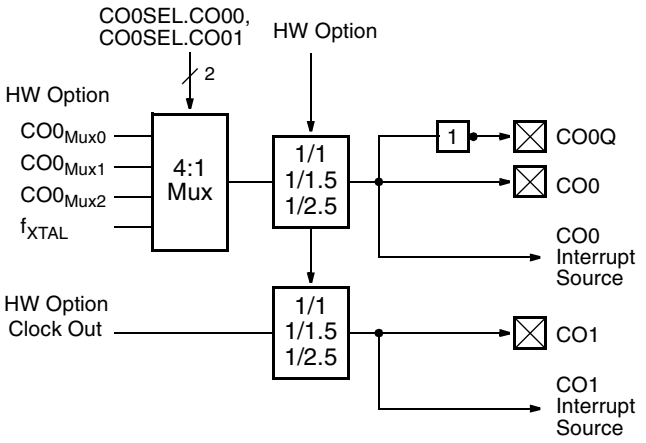


Fig. 4–3: Clock Outputs Diagram

Signal CO0 is the output of a prescaler and a 4 to 1 multiplexer. Prescaler and input for the multiplexer are selectable by HW options (see Table 4–3). The output selection of the multiplexer is done by register CO0SEL, bits CO01 and CO00. The outputs of the pre scalers are fed not only to the ports, but may also serve as interrupt source. The U-Ports assigned to function as clock outputs (see Table 4–3) have to be configured Special Out.

The interrupt source output of this module is routed to the Interrupt Controller logic. But this does not necessarily select it as input to the Interrupt Controller. Check section “Interrupt Controller” for the actually selectable sources and how to select them.

CO0 and CO1 are not affected by CPU SLOW mode.

Table 4–3: HW Options and Ports

Signal	HW Options		Initialization	
	Item	Address	Item	Setting
CO0	CO0 Prescaler	CO00C	CO0 output	U1.6, U3.3 or U7.7 special out
	$CO0_{Mux0}$		CO0Q output	U1.5 special out 1)
	$CO0_{Mux1}$	CO01C		
	$CO0_{Mux2}$	CO02C		
CO1	CO1 Prescaler	CO1C	CO1 output	U0.4, U1.5 or U7.6 special out1)
	Clock Out			
1) HW Options register flag PM.U15 switches between CO0Q and CO1 at U1.5 special out.				

4.4. EMI Reduction Module (ERM)

The IC contains an EMI Reduction Module (ERM), which is capable of reducing electromagnetic radiation that might cause interference to other electronic equipment. The concept of this circuit uses precisely defined time offsets of the master clock phases as generated by the PLL. Thus, the module is only available in PLL modes.

All internal clock signals except f_{XTAL} are affected. Thus also the sampling time points of clocked inputs and outputs of all internal modules are modulated. To avoid a possible performance degradation of, e.g., communication modules in a user environment, the maximum possible delay of the sampling clock phase can be controlled with the parameters given in table 4–5. In critical applications, I/O sampling time point modulation and EMI reduction can thus be compromised. Section 4.7.gives application hints.

Features

- Strong suppression of electromagnetic radiation
- Precisely controlled effect on sampling time points of clocked I/O (ADC, CAN, UART, SPI etc.)
- All parameters fully controllable and reproducible
- Three operation modes for different purposes
- Works for clock frequencies of up to 48 MHz
- No degradation of CPU performance

4.4.1. Modes

The ERM has 4 modes of operation:

- Mode 0, ERM off.
- Mode 1 is intended for the low f_{SYS} frequencies of 8 MHz or 10 MHz with a clock multiplier of n = 2 (PLLC.PMF = 1). Mode 1 with a clock tolerance of 7 has a similar harmonics suppression as the formerly used EMI Reduction Module V3.1.
- Mode 2. This mode is primarily intended for the deactivation process of mode 3 but may also be used for operation. It performs best at high clock frequencies.
- Mode 3 gives best results at medium and high f_{SYS} frequencies. At medium frequencies it is even capable of a certain suppression of the fundamental.

In each of the three operation modes the parameters may be particularly chosen with the help of registers ERMC.SUP and ERMC.TOL, to achieve an optimum suppression while keeping phase modulation of f_{IO} as low as possible. In Table 4–5, three sets of parameters with maximum f_{IO} sampling delays of:

- 7.5 ns (weak),
- 12.5 ns (normal) and
- 20 ns (strong)

are given as examples. However, other individual settings are possible (see section 4.4.2.).

At f_{SYS} frequencies of 40 MHz and above only a limited EMI suppression is possible. At an f_{SYS} of 50 MHz the ERM must be switched off (mode 0).

4.4.2. Rules for Setting Parameters

Each f_{SYS} multiplier n and each mode requires its own set of parameters. For individual settings other than those given in Table 4–5 the rules are given below.

For mode 1 the limits are:

- The suppression strength has no effect and should be kept at 0.
- The clock tolerance must not exceed the values given in the columns for strong settings.

For modes 2 and 3 the limits are:

- Numbers must not exceed the values given in the columns for strong settings.
- The clock tolerance must be equal to or less than (suppression strength +1)/2.
- In mode 2 the suppression strength must not exceed 43.
- In mode 3 the sum of clock tolerance and suppression strength must not exceed 43.

4.4.3. Initialization

For operation of the ERM, the clock system has to be in one of the PLL modes. After Reset, the ERM is in mode 0. All internal registers are reset to their default values.

The initialization must be done in the following order:

1. Set the clock tolerance (ERMC.TOL) to 1.

2. Set the suppression strength (ERMC.SUP) to 1 (modes 2 and 3 only).

3. Select the desired mode (1...3) in ERMC.EOM according to Table 4–5.

4. Select the desired suppression strength (ERMC.SUP).

5. Select the desired clock tolerance (ERMC.TOL).

4.4.4. Deactivation

To deactivate the ERM, the following sequence must be observed:

1. If in mode 3, enter mode 2 by writing 2 to field ERMC.EOM.

2. Set the clock tolerance parameter (ERMC.TOL) to 1 (steps 1. and 2. must not be done in one operation).

3. Set the suppression strength (ERMC.SUP) to 1 (modes 2 and 3 only).

4. Wait at least 8 f_{SYS} cycles (e.g. CPU NOPs) before checking the In-Phase flag ERMC.INPH.

5. Wait for flag ERMC.INPH to be set (may take up to 80 f_{SYS} cycles), then clear the field ERMC.EOM to return to mode 0 This will turn off the ERM.

4.5. Memory Controller

The Memory Controller connects the CPU to the complex memory system. It controls the various types of access and wait states.

Features

- support of one synchronous- and up to three different asynchronous memory areas
- different wait state values for sequential and nonsequential accesses to asynchronous memory
- allows 8, 16 and 32bit memory accesses from CPU
- supports access to 8, 16 and 32bit wide memory
- allows big or little endianness.

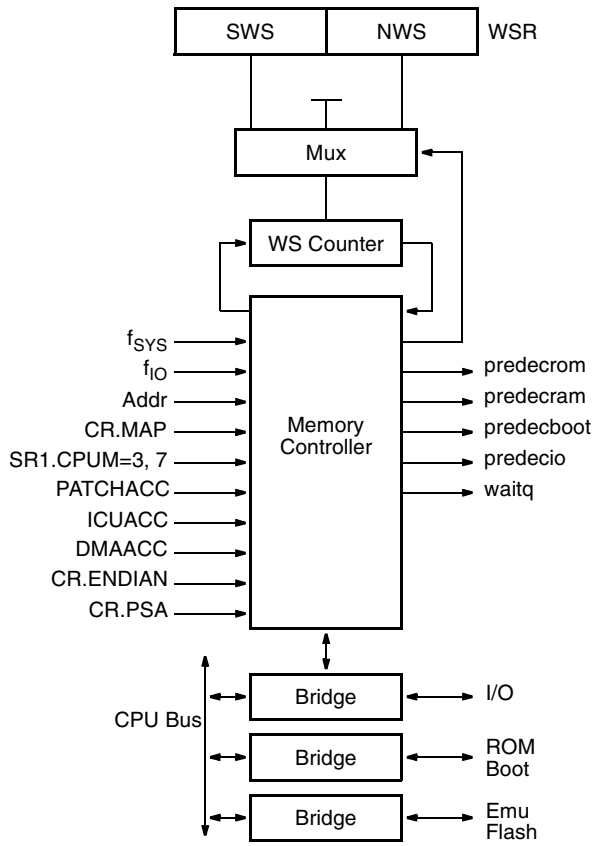


Fig. 4–4: Memory Controller Block Diagram

4.5.1. Principle of Operation

4.5.1.1. General

The Memory Controller contains a Memory Mapping Unit (MMU) to control the mapping of the whole memory system, a Wait State Register (WSR) to initialize the various wait states, a Final State Machine and a Wait State Counter to control the various types of access and wait states.

4.5.1.2. Initialization

After reset, the CPU runs in CPU FAST mode, the Wait State Counter is disabled due to SR1.CPUM=1 and no wait states for access to asynchronous memory are programmed. The access to the synchronous memory (I/O) works right after reset, independent from any setting by software. Endian mode is set by the Control Word via bit CR.ENDIAN.

First, initialize the wait state register WSR (cf. Table 4–5). Then the PLL or PLL2 mode may be enabled, if desired. Don't change the wait state register while in PLL mode, this may lead to a memory access with undetermined wait state count in the following cycle.

4.5.1.3. Operation

With proper SW initialization, the Memory Controller is also ready to access the asynchronous memory systems (ROM/Flash, RAM, Boot ROM).

The MMU decides from the address and the CR setting, which area in memory space contains a 8, 16 or 32bit memory system. It preselects the different types of memory (ROM/Flash, RAM, Boot ROM and I/O-Pages) and computes the address for ROM/Flash minus 200000hex, if ROM/Flash should be mapped to base address 200000hex.

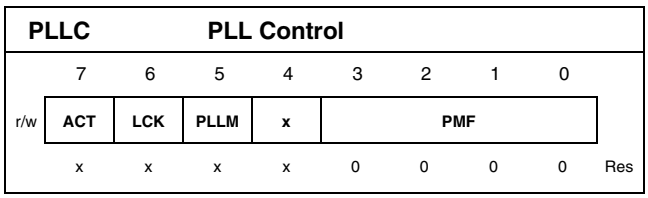
In presence of a Patch Module, the PATCHACC signal from the Patch Module signals to the MMU that the next access will be an access to the Patch Module instead to normal ROM/Flash, RAM or Boot ROM.

The DMAACC signal from the DMA Module signals, that the next address value will be driven by DMA and not by CPU. Due to the fact that DMA always reads a location in ROM/Flash, RAM or Boot ROM and writes to a location in the I/O area within the same bus cycle, the MMU also preselects the I/O area and the Memory Controller times the whole DMA cycle to the restrictions of the slow synchronous I/O area.

4.5.1.4. Inactivation

Returning the Memory Controller to CPU FAST mode (SR1.CPUM=1) will immediately switch the CPU to FAST mode and change any further access to asynchronous memory to non-wait-state operation.

4.6. Registers



ACT **PLL Active**
r1: PLL started (PMF > 0)
r0: PLL not activated (PMF = 0)

LCK **PLL Locked**
r1: PLL locked
r0: PLL not locked

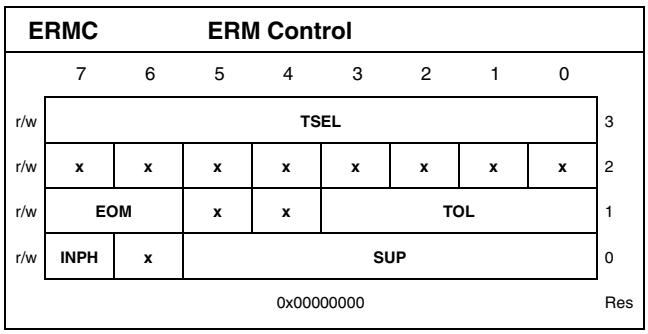
PLLM **PLL Mode Acknowledge**
r1: The clock chain has switched to PLL mode
r0: Not PLL mode

PMF **PLL Multiplication Factor (Table 4–5)**
w0: PLL is switched off and internally bypassed. This is the standby mode for the PLL.
w15-1: Starts PLL with the corresponding frequency. If not active anyway, the VREFINT Generator and BVDD Regulator are enabled

PMF is a write only field. Don't modify PMF in PLL mode.

$$f_{SYS} = n \cdot f_{XTAL} = (PMF + 1) \cdot f_{XTAL}$$

Above formula relates to PLL mode.



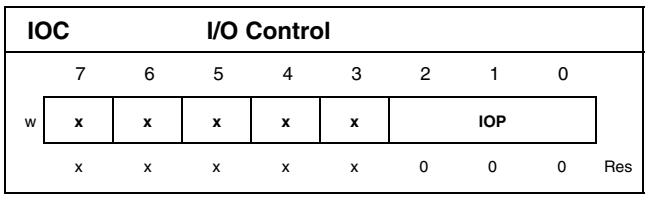
TSEL **Test Select**
r/w Factory use only.

EOM **ERM Operation Mode**
r/w3: Mode 3
r/w2: Mode 2
r/w1: Mode 1
r/w0: Off

TOL **Clock Tolerance**
r/w15-0: (see Table 4–5 and 4–6)

INPH **In Phase (during deactivation)**
r1: Phase is 0 or 1
r0: Phase > 1

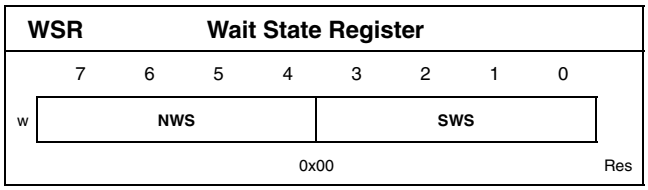
SUP **Suppression Strength**
r/w63-0 (see Table 4–5 and 4–6)



IOP **I/O Clock Prescaler (Table 4–5)**
w IOP is a write only field.

$$f_0 = \frac{f_{SYS}}{m} = \frac{f_{SYS}}{IOP + 1} = \frac{PMF + 1}{IOP + 1} \cdot f_{XTAL}$$

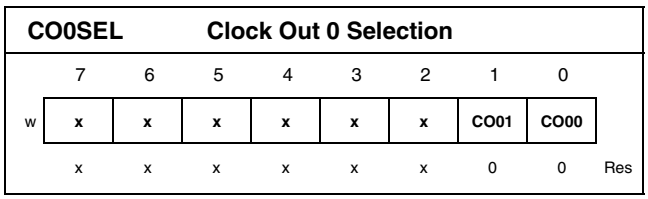
Above formula relates to PLL mode.



NWS **Nonsequential Wait State Bits**
w: Number of wait states at nonsequential memory access.

SWS **Sequential Wait State Bits**
w: Number of wait states at sequential access.

The WSR influences access to ROM, Flash and Boot ROM.



CO00, CO01 **Clock Out Bit 0 and 1**
w: Clock selection

Table 4–4: CO00 and CO01 Usage

CO01	CO00	Selection
0	0	$CO0_{Mux0}$
0	1	$CO0_{Mux1}$
1	0	$CO0_{Mux2}$
1	1	f_{XTAL}

4.6.1. Recommended Settings

Tables 4–5 and 4–6 list settings available for the EMU device. **When emulating a specific target device (MCM or mask ROM), use the Recommended Settings of that device only**. Settings **differing** from these two lists shall not be used and may result in undefined behaviour.

It is required not to operate I/O faster than Flash.

Suppression Strength (SUP) and Clock Tolerance (TOL) may be varied between zero and the values for strong settings according to the rules in Section 4.4.2. The given limits must not be exceeded

Table 4–5: PLL and ERM Modes: Recommended Settings and Resulting Operating Frequencies (MHz)

f_{XTAL}	CPU		Program Storage		I/O		ERMC.EOM = 1						ERMC.EOM = 2 or 3					
							Weak		Normal		Strong		Weak		Normal		Strong	
	f_{SYS}	PLLC. PMF	f_{BUS}	WSR	f_{IO}= f_0	IOC. IOP	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL
4	8	1	8	0x00	8	0	0	4	0	7	0	11	4	2	7	4	11	6
	16	3	16	0x00		1	0	8	0	13	0	13	8	4	14	6	22	6
			8	0x11			0	8	0	14	0	15	8	4	14	7	22	11
	24	5	12	0x11		2	0	12	0	13	0	13	12	6	21	11	31	12
			8	0x22			0	12	0	13	0	13	12	6	21	11	31	12
	32	7	16	0x11		3	0	6	0	6	0	6	16	6	28	6	37	6
			10.7	0x22			0	6	0	6	0	6	16	6	28	6	37	6
5	10	1	10	0x00	10	0	0	5	0	8	0	14	5	3	8	4	14	7
	20	3	20	0x00		1	set ERMC.EOM=0						set ERMC.EOM=0					
			10	0x11			0	10	0	15	0	15	10	5	17	9	28	12
	30	5	15	0x11		2	0	8	0	8	0	8	15	8	26	8	35	8
			10	0x22			0	8	0	8	0	8	15	8	26	8	35	8

Table 4–6: PLL2 and ERM Modes: Settings Sacrificing Unlimited Operation of Peripheral Modules and Resulting Operating Frequencies (MHz)

f_{XTAL}	CPU		Flash		I/O		ERMC.EOM = 1						ERMC.EOM = 2 or 3					
							Weak		Normal		Strong		Weak		Normal		Strong	
	f_{SYS}	PLLC. PMF	f_{BUS}	WSR	f_{IO}= f_0	IOC. IOP	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL
4	12	2	6	0x11	4	2	0	6	0	10	0	15	6	3	10	5	16	8
			12	0x00			0	5	0	5	0	5	6	2	10	2	16	2
	20	4	10	0x11		4	0	10	0	15	0	15	10	5	17	8	28	8
5	15	2	7.5	0x11	5	2	0	7	0	13	0	15	7	4	13	7	21	11

4.7. PLL/ERM Application Notes

4.7.1. PLL Jitter

The embedded PLL synchronizes every n-th f_{SYS} cycle to the externally applied f_{XTAL} signal. This synchronization smoothly tries to cancel out influences from power supply noise and f_{XTAL} fluctuations. Depending on the application, this permanent re-synchronization process is expected to introduce some nanoseconds of phase jitter to f_{IO}.

It is important to note that PLL jitter does not introduce a noticeable frequency error, because the phase stays locked to the f_{XTAL} reference and fluctuates, even over long times, only within the same tight limits. Even with a PLL induced f_{IO} jitter of ±10ns, the maximum observable frequency error between two f_{IO} clocks
– spaced 1us apart is (1us±2∗10ns)/1us=±2%,
– spaced 1ms apart is (1ms±2∗10ns)/1ms=±20ppm,
– spaced 1s apart is (1s±2∗10ns)/1s=±0.02ppm,
and so forth.

4.7.2. ERM "Jitter"

The effect of the ERM on f_{IO} phase and frequency is similar to that of PLL jitter in that it adds limited phase modulation. However, this ERM induced jitter is especially tailored to improve the electromagnetic emission properties of the device. Section 4.4.1. gives details on setting the maximum phase delay:
– 7.5ns (weak) translates to ±3.75ns of f_{IO} jitter,
– 12.5ns (normal) translates to ±6.25ns of f_{IO} jitter,
– 20ns (strong) translates to ±10ns of f_{IO} jitter.

From these figures it is evident, that ERM introduces a jitter that, in its extent, is comparable to PLL jitter. Both influences may be added to estimate the combined PLL/ERM effect on I/O module operation.

4.7.3. Influence of PLL/ERM on Module Operation

DIGITbus, SPI and I2C synchronize external devices to one master clock. Their operation is hardly impeded by PLL/ERM jitter.

Modules like UART and CAN communicate with external fixed-frequency devices, and there is a maximum frequency offset between transmitting and receiving station, that can be tolerated without transmission error.

Viewed from the receiving station, a frequency offset of the transmitting station is tolerable, as long as over the length of a complete telegram, every bit can still be detected unambiguously. Once the tolerable frequency offset is exceeded, communication is fatally disturbed. This tolerable offset is dependent on the capability of the involved circuitry to detect and compensate for frequency offset.

In the further discussion, the clock tolerance TOL is defined as percentage offset of the actual from the nominal frequency

$$TOL = \frac{|f_{act} - f_{nom}|}{f_{nom}}$$

Note that each transmitting and receiving station are allowed this same tolerance from nominal:
$f_{trans}=f_{nom}\pm TOL$ and $f_{rec}=f_{nom}\pm TOL$
The resulting maximum offset between transmitter and receiver thus is 2 x TOL.

4.7.3.1. UART

Let's consider the tolerable frequency offset in the case of the UART.

The Baud Rate frequency is always the sample clock frequency, divided by 8. The max. telegram length is 12 bit. A transmitter frequency offset is tolerable as long as 12*8 ± 3 receiver sample clocks equal 12*8 transmitter sample clocks, which gives a transmitter frequency of $f_{Trans}=f_{Rec}(12*8/(12*8\pm3))=f_{Rec}\pm3.23\%$ and TOL=±1.61%.

PLL and ERM jitter claim a certain portion of this tolerable offset. Let's assume that both influences add up to ±20ns of f_{IO} jitter, and that $f_{IO}=f_0$=8MHz.

With the Baud rate set to 1MBaud, f_{SAMPLE} equals 8MHz. With this setting, PLL and ERM jitter consume
2*20ns/375ns=10.7%
of the tolerable transmitter frequency offset and reduce TOL to 1.44%.

With the Baud Rate set to 19.23kBaud, f_{SAMPLE} equals 153.84kHz. With this setting, PLL and ERM jitter consume
2*20ns/19.5us=0.2%
of the tolerable transmitter frequency offset and reduce TOL only slightly to 1.605%.

4.7.3.2. CAN

The CAN Module contains logic that re-synchronizes a receiver to a transmitter several times during a telegram. By these means, a receiver is able to adapt to the transmitter frequency within narrow limits.

Two situations have to be distinguished:

1. Bit stuffing guarantees a maximum of 10 bit periods between two consecutive re-synchronization edges. Therefore the accumulated phase error must be less than the programmed re-synchronization jump width (SJW). The limitation that this situation imposes on the maximum TOL can be expressed as:

$$2 \times TOL \leq \frac{t_{SJW}}{10 \times t_{Bit}}$$

or

$$TOL \leq \frac{t_{SJW}}{2 \times 10 \times t_{Bit}}$$

2. Another limit on the maximum TOL is set by the situation where the CAN logic must be able to correctly sample the first bit after an error frame. This is the 13th bit after the last re-synchronization. This limitation can be expressed as:

$$2 \times TOL \leq \frac{\min(t_{Phase\ Seg1}, t_{Phase\ Seg2})}{13 \times t_{Bit} - t_{Phase\ Seg2}}$$

or

$$TOL \leq \frac{\min(t_{Phase\ Seg1}, t_{Phase\ Seg2})}{2 \times (13 \times t_{Bit} - t_{Phase\ Seg2})}$$

Example (f_0 = 10MHz)

With the Baud rate set to 1MBd, t_{Bit} equals 1µs and is divided into 10 time quants (t_Q = 100ns). t_{SJW} and t_{TSEG2} are programmed to 3 t_Q (= $t_{Phase\ Seg1}$ = $t_{Phase\ Seg2}$). 3 t_Q are reserved for the propagation delay segment. In the first case the maximum tolerance TOL is 1.5% (edge to edge):

$$TOL \leq \frac{3}{2 \times 10 \times 10} = 0{,}015$$

In the second case, TOL is 1.2% (edge to sample point):

$$TOL \leq \frac{3}{2 \times (13 \times 10 - 3)} = 0{,}012$$

The smaller value of the above (1.2%) is relevant.

Following the UART example, PLL/ERM jitter consumes up to 2*20ns of 300ns (SJW = 3 time quants). This makes 40ns/300ns=13.3% of this tolerance, thus reducing TOL to ±1.04%.

With the Baud rate set to 500kBd, t_{Bit}=2µs and t_Q=200ns. The maximum tolerance TOL of 1.2% reduces by 2*20ns/600ns=6.7% to ±1.12%.

Example (f_0 = 8MHz)

With the Baud rate set to 1MBd, t_{Bit} equals 1µs and is divided into 8 time quants (t_Q = 125ns). t_{SJW} and t_{TSEG2} are programmed to 2 t_Q (= $t_{Phase\ Seg1}$ = $t_{Phase\ Seg2}$). 3 t_Q are reserved for the propagation delay segment. In the first case the maximum tolerance TOL is 1.25% (edge to edge):

$$TOL \leq \frac{2}{2 \times 10 \times 8} = 0{,}0125$$

In the second case, TOL is 0.98% (edge to sample point):

$$TOL \leq \frac{2}{2 \times (13 \times 8 - 2)} = 0{,}0098$$

The smaller value of the above (0.98%) is relevant.

Following the UART example, PLL/ERM jitter consumes up to 2*20ns of 250ns (SJW = 2 time quants). This gives 40ns/250ns=16% of this tolerance, thus reducing TOL to ±0.82%.

With the Baud rate set to 500kBd, t_{Bit}=2µs and t_Q=250ns. The maximum tolerance TOL of 0.98% reduces by 2*20ns/500ns=8.0% to ±0.9%.

4.7.3.3. DIGITbus

The DIGITbus master synchronizes with external devices via the serial data line. The slave node recovers the transmission clock from the data signal via an own PLL. This PLL will lock to the long-term average frequency of the master, and the slave node sees PLL/ERM jitter as a short-term frequency offset.

Following the UART example, one can define the tolerable frequency offset:
Every bit starts with a rising edge and thus every bit has a re-synchronization point. The bit period (t_{Bit}) is divided into four equal length parts. Falling edges happen nominally after 1/4, 2/4 or 3/4 of the bit period. After 4/4 of the bit period a rising edge indicates the beginning of the next bit. The DIGITbus logic tolerates a jitter of these edges up to ±1/8 of the bit period. Thus, a transmitter frequency offset is tolerable up to $f_{Trans} = f_{Rec}(1 \pm 1/8) = f_{Rec} \pm 12.5\%$ and TOL = ±6.25%.

Again following the UART example, ERM/PLL jitter influences this tolerable offset:
With the Baud rate set to 31.25kBd, 1/8 of the bit period is 4µs. PLL/ERM jitter reduces the maximum tolerance TOL of ±6.25% by 2*20ns/4µs=1% to ±6.19%.

4.7.3.4. SPI and I2C

Modules like SPI and I2C synchronize with external devices by the serial clock. Thus, no frequency offset between transmitting and receiving station can develop, and no adverse effects of PLL/ERM operation are expected.

5. Memory and Boot System

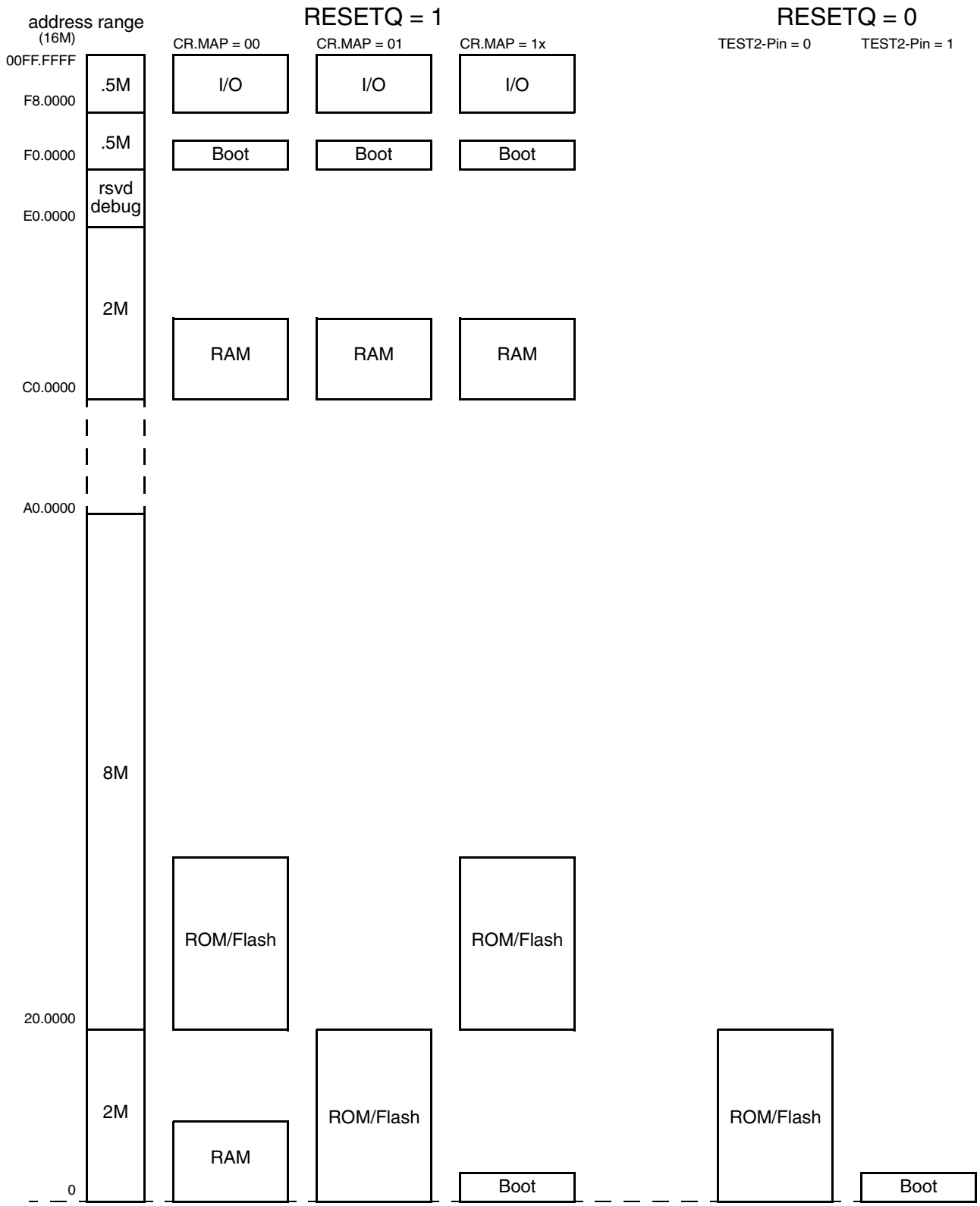


Fig. 5–1: Address Map. Most Common Settings

5.1. RAM and ROM

On-chip RAM is composed of static RAM cells. It is protected against disturbances during reset as long as the specified operating voltages are available.

The 128PQFP Multi Chip Module also contains a 512K byte Flash EEPROM of the AMD Am29LV400BT type (top boot configuration). This device exhibits electrical byte program and sector erase functions. Refer to the AMD data sheet for details.

Future mask ROM derivatives may be specified to contain less or more internal RAM and ROM than this IC:

– ROM will grow upward from 0x0200000 to 0x09FFFFF (8MByte) and can be remapped to physical address 0 (growing upward to 0x07FFFFF). It is 16bit wide and is asynchronously accessed with wait states.

– RAM will always grow upward from physical address 0x0C00000to 0x0DFFFFF (2MByte) and can be mirrored to physical address 0. It is 32bit wide and is asynchronously accessed without wait states.

– Boot ROM will grow upward from physical address 0x0F00000 to 0x0F7FFFF (0.5MByte) and can be mirrored to physical address 0. The I/O area will grow upward from physical address 0x0F80000 to 0x0FFFFFF (0.5MByte). It is 16bit wide and is asynchronously accessed with wait states.

Mirrored means the memory is accessible at both locations. Remapped means the memory is accessible at the new location only.

All parts (ROM, Flash and Emu) contain at least the I/O, the RAM and the Boot ROM.

5.1.1. Reserved Addresses

Reserved Addresses are memory locations which define the behavior of internal HW or external systems. In our system the memory locations at address 0 and following have dedicated functions. The function of these memory locations depend on which kind of physical memory is mapped to these locations. As you can see at table 5–1 ROM/Flash or Boot ROM has to be mapped to location 0 at reset. Otherwise Control Word can not define the HW behavior and no ingenious instruction is available at the reset start address. As long as RAM is mirrored to location 0 addresses 20 and following have no influence on the internal HW.

Table 5–1: Reserved Addresses

Addresses	Size [byte]	Usage if mapped/mirrored to 0		
		RAM	**ROM/Flash**	**Boot ROM**
030 - 5F	48	General purpose RAM. No HW defined action.	HW Options	
02C - 2F	4		Factory ID	
02A - 2B	2		reserved	
028 - 29	2		ROM ID	
024 - 27	4		Security Vector	ARM ID
020 - 23	4		Control word	
01C - 1F	4	FIQ (Fast Interrupt)		
018 - 1B	4	IRQ (Interrupt)		
014 - 17	4	Reserved		
010 - 13	4	Data Abort		
00C - 0F	4	Prefetch Abort		
008 - 0B	4	SWI (Software Interrupt)		
004 - 07	4	Undefined instruction		
000 - 03	4	Reset		

5.1.1.1. HW Options

Please refer to section “Hardware Options” for information about layout of the HW Options field and the corresponding Registers in the I/O area. To activate the HW Options related functions, the SW has to copy them to the corresponding locations in the I/O area.

But nevertheless this are HW Options. It is not intended to modify them by SW in ROM parts. In this case the result is unpredictable.

5.1.1.2. ROM ID

The ROM ID serves as identification of the corresponding application/boot program. It will be read by an external system (test, debug) and doesn't influence internal HW.

The ROM ID contains a half-word sized hexadecimal value. The range is 0x0000 to 0xFFFF.

5.1.1.3. Factory ID

The Factory ID contains a factory defined code. It contains information about the HW version, frequency, etc. It will be read by an external system (test, debug) and doesn't influence internal HW. The Boot system may use this information and adopt its behavior according to the Factory ID. The layout of the Factory ID is not yet defined **TBD**.

5.1.1.4. Security Vector

The main job of the Security Vector is to enable the JTAG interface via Boot ROM if the Flash ROM does not contain a correct application program (see Section 5.3. on page 50). The Boot ROM program can not enable the JTAG interface if the Security Vector contains the value 0x55AA55AA. This is the way the application program can disable JTAG access.

An empty (not programmed) Flash ROM contains all ones. Hence the Security Vector contains a non valid pattern and the Boot ROM enables the JTAG interface.

The following sequence of actions has to be done in order to reprogram a Flash ROM:

1. Clear the Security Vector (0x00000000).
2. Clear the Flash ROM (Security Vector = 0xFFFFFFFF).
3. Program all of the Flash ROM without the Security Vector.
4. Verify the Flash ROM.
5. If ok, write 0x55AA55AA to the Security Vector. Otherwise go to step 2 again.

This proceeding guarantees that the JTAG interface will be enabled after reset via Boot ROM, if something goes wrong during Flash ROM programming.

A correct application program should provide a different way and interface to enable JTAG and to modify the Security Vector.

During developing and debugging the Security Vector can be written to a non valid value to allow easy JTAG access.

5.1.1.5. ARM ID

The ARM core can contain a System Control Coprocessor (CP15) which contains among other things an ID Register. It allows the identification of the implemented processor. There is no CP15 implemented up to now, but the ARM ID field may contain the same information.

5.1.1.6. Control Word

The Control Word defines the behavior of the HW during reset. Refer to section "Core Logic" for information about Control Word definition.

5.2. I/O Map

The I/O region is divided into the lower part (addresses 00F80000 to 0x00FBFFFF) which is connected to the 8 bit wide bus and into the upper part (addresses 00FC0000 to 0x00FFFFFF) which is connected to the 32 bit wide bus. Please refer to section "Register Cross Reference Table" for detailed I/O register mapping.

Access to I/O modules which are connected to the 8 bit wide bus is restricted: If not otherwise mentioned those modules must be accessed by byte access only. This memory area is organized in little endian format. If the CPU operates in big endian format, only byte access is recommended.

Table 5–2: I/O Map

Address	Size	Access	What
00FFFFFF 00FFFF00	256	32bit, asynchronous, no wait states	IRQ and FIQ registers
00FFFEFF 00FFFE00	256		DMA registers
00FFFDFF 00FFFC00	512		Core registers
00FFFBFF 00FC0000	255k		Free

Table 5–2: I/O Map

Address	Size	Access	What
00FBFFFF 00F90800	190k	8bit, synchronous, wait states	Free
00F907FF 00F90000	2k		Registers
00F8FFFF 00F81200	59.5k		Free
00F811FF 00F81000	512		CAN registers
00F80FFF 00F80000	4k		CAN-RAM

5.3. Boot System

The job of the Boot System is to enable the JTAG interface if necessary. Further actions as there are download, Flash ROM programming or debugging and monitoring has to be done via JTAG interface.

If TEST2 pin is held high during reset, the Control Word from the Boot ROM is copied to the Control Register by HW. The Boot ROM Control Word is configured to start program execution from the Boot ROM, mirrored to location 0. The Boot ROM Control Word disables JTAG.

5.3.1. Principle of operation

The Boot ROM is accessible at two locations, originally at address 0xF00000 and mirrored at address 0x0. The first instruction of the Boot ROM (Reset Vector) loads the address of the next instruction in the original Boot ROM (0xF00100, above the Boot ROM HW Options) into the program counter. This causes a jump from the mirrored Boot ROM to the original Boot ROM. The remaining part of the program is running in the original Boot ROM and remapping of the memory does not influence correct operation of the boot program.

The program reads the TEST pin in order to distinguish between application and factory boot program. In case of the security vector is set in the application program, the application is started, otherwise the JTAG interface is enabled and program stays in an endless loop. In case of factory boot program a test program is started.

The watchdog is not triggered in the Boot ROM program. Especially when the program is in the endless loop this may cause problems. But this endless loop will not be reached in ROM parts, where the watchdog may be HW enabled (option), as long as the security vector is valid. In Flash ROM parts the watchdog should not be HW enabled.

```
boot()
{
   Jump to 0xF00100;
   if(TEST pin low)
   {     /* Custom boot */
      if(security vector)
      {  /* Application available */
         Load Control Registers with
         application Control Word;
         Jump to location 0x0;
      }
      else
      {  /* No application */
         Enable JTAG;
         Endless loop;
      }
   }
   else /* TEST pin high */
   {     /* Factory boot */
      Run test program;
   }
}
```

Fig. 5–2: Boot program

6. Core Logic

6.1. Control Word CW

Some system configuration items are freely selectable during device start-up by means of a unique Control Word (CW).

6.1.1. Reset Active

During Reset, the device fetches this CW from address locations 0x20 to 0x23 of a source that is determined by the state of pins TEST and TEST2, see Table 6–1 for MCM and ROM parts and Table 6–2 for EMU parts.

Table 6–1: CW fetch in MCM and ROM parts (QFP128)

Control Word Fetch desired from	Necessary Reset config. of pins	
	TEST2	TEST
Internal ROM/Flash	0	0
External via Multi Function port	0	1
Internal Boot ROM	1	x

Table 6–2: CW fetch in EMU parts (CPGA257)

Control Word Fetch desired from	Necessary Reset Config. of pins	
	TEST2	TEST
External via Emu port	0	0
External via Multi Function port	0	1
Internal Boot ROM	1	x

6.1.2. Reset Inactive

When exiting Reset, the CW is loaded into the Control Register (CR) and the system will start up according to the configuration defined therein.

Normally the CW is fetched from the same memory that the system will later start executing code from. Table 6–3 gives fix CWs for a list of the most commonly used configurations.

For special purposes, the CW source and the program source may differ. For these purposes, a detailed description of the CW and CR function is given in the chapter “Control Register and Memory Interface”.

Table 6–3: Some common system configurations and the corresponding CW setting

Part Type	Program Start desired from	Additional desired properties	Necessary CW	
			31:16	15:0
EMU	ext. 32-Bit sync SRAM (e.g. MT55L256L32F) on EMU port	Trace Bus ETM mode	0xFFBA	0x835F
		16-Bit ROM/Flash emulation, Trace Bus ETM mode	0xFFBB	0x835F
		16-Bit ROM/Flash emulation, Trace Bus Analyzer mode, Appl. JTAG released	0xFFBB	0xA3DF
	ext. 32-Bit async auto-power-down Flash (2x Am29LV400BT) on EMU port	-	0xFFBA	0x675F
	ext. 16-Bit async. auto-power-down Flash (Am29LV400BT) on EMU port	Trace Bus Analyzer mode	Don’t care	0x2F5F
		Trace Bus ETM mode	Don’t care	0x4F5F
MCM	int. 16-Bit Flash (Am29LV400BT)	-	Don’t care	0x7F5F
ROM	int. 16-Bit ROM	-	Don’t care	0x7F5F

6.2. Standby Registers

The Standby Registers SR0 to SR1 allow the user to switch on/off power or clock supply of single modules. With these flags it is possible to greatly influence power consumption and its related electromagnetic interference.

For details about enabling and disabling procedures and the standby state refer to the specific module descriptions.

SR0 Standby Register 0

	7	6	5	4	3	2	1	0	Offs
r/w	I2C1	I2C0	x	x	x	x	CAN2	CAN1	3
r/w	TIM2	TIM3	TIM4	UART1	x	DGB	CCC1	x	2
r/w	LCD	x	PSLW	UART0	ADC	x	TIM1	XTAL	1
r/w	SM	x	x	x	SPI1	CAN0	CCC0	SPI0	0
	0x00000100								Res

I2C1 **I2C Module 1**
r/w1: Enabled
r/w0: Disabled

I2C0 **I2C Module 0**
r/w1: Enabled
r/w0: Disabled

CAN2 **CAN Module 2**
r/w1: Module active.
r/w0: Module off.

CAN1 **CAN Module 1**
r/w1: Module active.
r/w0: Module off.

TIM2 **Timer 2**
r/w1: Module active.
r/w0: Module off.

TIM3 **Timer 3**
r/w1: Module active.
r/w0: Module off.

TIM4 **Timer 4**
r/w1: Module active.
r/w0: Module off.

UART1 **UART 1**
r/w1: Module active.
r/w0: Module off.

DGB **DIGITbus Master**
r/w1: Module active.
r/w0: Module off.

CCC1 **Capture Compare Counter 1**
r/w1: Module active.
r/w0: Module off.

LCD **LCD Module**
r/w1: Module active.
r/w0: Module off.

PSLW **Port Slow Mode**
r/w1: Slow mode.
r/w0: Fast mode.

UART0 **UART 0**
r/w1: Module active.
r/w0: Module off.

ADC **ADC Module**
r/w1: Module active.
r/w0: Module off.

TIM1 **Timer 1**
r/w1: Module active.
r/w0: Module off.

XTAL **Quartz Oscillator Mode**
r/w1: Start-Up Mode active (default after Reset).
r/w0: Run Mode active.

SM **Stepper Motor**
r/w1: Module active.
r/w0: Module off.

SPI1 **SPI 1**
r/w1: Module active.
r/w0: Module off.

CAN0 **CAN Module 0**
r/w1: Module active.
r/w0: Module off.

CCC0 **Capture Compare Counter 0**
r/w1: Module active.
r/w0: Module off.

SPI0 **SPI 0**
r/w1: Module active.
r/w0: Module off.

SR1 Standby Register 1

	7	6	5	4	3	2	1	0	Offs
r/w	x	x	x	x	x	x	x	x	3
r/w	x	x	x	x	x	x	x	x	2
r/w	x	PFM0	PWM11	PWM9	PWM7	PWM5	PWM3	PWM1	1
r/w	IRQ	FIQ	x	x	x	CPUM			0
	0x00000001								Res

PFM0 **Pulse Frequency Modulator 0**
r/w1: On
r/w0: Off

PWM11 **Pulse Width Modulator 11**
r/w1: On
r/w0: Off

PWM9 **Pulse Width Modulator 9**
r/w1: On
r/w0: Off

PWM7 **Pulse Width Modulator 7**
r/w1: On
r/w0: Off

PWM5 **Pulse Width Modulator 5**
r/w1: On
r/w0: Off

PWM3 **Pulse Width Modulator 3**
r/w1: On
r/w0: Off

PWM1 **Pulse Width Modulator 1**
r/w1: On
r/w0: Off

IRQ **IRQ Interrupt Controller**
r/w1: Enabled
r/w0: Disabled

FIQ **FIQ Interrupt Controller**
r/w1: Enabled
r/w0: Disabled

CPUM **CPU Mode**
Clock selection for CPU and peripheral modules (Section “CPU and Clock System”).

6.3. UVDD Analog Section

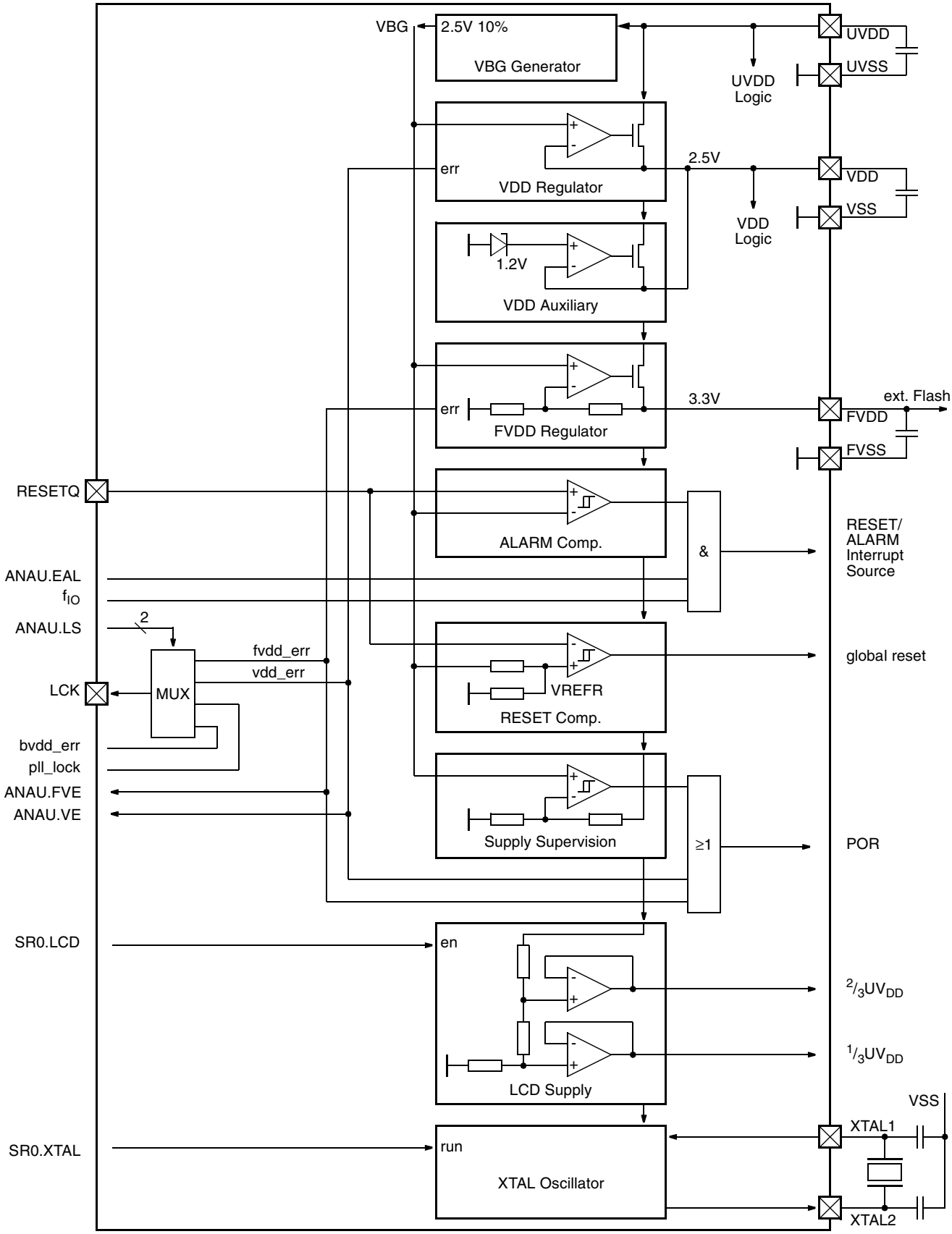


Fig. 6–1: UVDD Analog Section Block Diagram

6.3.1. VBG Generator

The low-power VBG Generator generates bias signals which are necessary for the operation of all UVDD Analog Section modules. Furthermore, it produces a reference voltage VBG, that is delivered to the VDD and FVDD Regulators, the RESET and ALARM Comparators and the UVDD Supply Supervision.

This module is permanently enabled.

6.3.2. VDD Regulator

The VDD Regulator generates the 2.5V VDD supply voltage for the internal core logic from the 5V UVDD. It derives its reference from the VBG Generator.

VDD must be buffered externally by a 220nF ceramic capacitor in parallel with a 10uF tantalum capacitor.

This module is permanently enabled. A certain set-up time has to elapse after power-up of UVDD for VDD to stabilize. During this time, the Supply Supervision (cf. 6.3.7.) generates a Power-On Reset.

An overload condition in the regulator (current or voltage drop-out) generates an immediate Reset and is stored in flag ANAU.VE. The immediate overload signal may be routed to the LCK special output by selection in field ANAU.LS.

6.3.3. VDD Auxiliary Regulator

The low-power VDD Auxiliary Regulator is designed to deliver a halt mode supply voltage to the core logic, where no clocked operation is required.

This module is permanently disabled and available only in Test modes.

6.3.4. FVDD Regulator

The FVDD Regulator generates the 3.3V FVDD supply voltage for the external Flash memory device from the 5V UVDD. It derives its reference from the VBG Generator.

FVDD must be buffered externally by a 470nF ceramic capacitor in parallel with a 3.3uF tantalum capacitor.

This module is permanently enabled. A certain set-up time has to elapse after power-up of UVDD for FVDD to stabilize. During this time, the Supply Supervision (cf. 6.3.7.) generates a Power-On Reset.

An overload condition in the regulator (current or voltage drop-out) generates an immediate Reset and is stored in flag ANAU.FVE. The immediate overload signal may be routed to the LCK special output by selection in field ANAU.LS.

6.3.5. ALARM Comparator

The Alarm Comparator on the pin RESETQ allows the detection of a threshold higher than the reset threshold. An alarm interrupt can be triggered with the output of this comparator.

To obtain a result that is independent from UVDD, the level of pin RESETQ is compared to the VBG reference voltage. The comparator features a small built-in hysteresis. The output constitutes the RESETQ/ALARM Interrupt Source and must be enabled by setting flag ANAU.EAL. Please refer to section 6.4.1. for functional details.

The interrupt source output is routed to the Interrupt Controller logic. But this does not necessarily select it as input to the Interrupt Controller. Check section “Interrupt Controller” for the actually selectable sources and how to select them.

The alarm interrupt is a level triggered interrupt. The interrupt is active as long as the voltage on pin RESETQ remains between the two thresholds of the ALARM and the RESET comparator.

6.3.6. RESET Comparator

As long as the Reset Comparator on the pin RESETQ detects the low level, the overall IC is reset.

To obtain a result that is independent from UVDD, the level of pin RESETQ is compared to the scaled down VBG reference voltage. The comparator features a built-in hysteresis.

Please refer to sections 6.4.2. and 6.4.4. for functional details.

6.3.7. Supply Supervision

When UVDD drops below a level VREFPOR of approx. 2.8V, or when the internal VDD or FVDD Regulators detect an overload condition, this module generates a Power-On reset signal POR that is routed to the Reset Logic.

Refer to section 6.4.2.1. for more details.

6.3.8. XTAL Oscillator

The XTAL Oscillator generates a 4 to 5 MHz reference signal from an external quartz resonator, cf. section “Electrical characteristics” for quartz data.

A reset sets the module to START-UP mode, where, at the expense of a higher current consumption, marginal quartzes receive more drive to ease start-up of oscillation.

After start-up of the CPU program, register SR0.XTAL may be cleared by SW to set the XTAL Oscillator to RUN mode, where current consumption is at its standard level.

For operation at UVDD levels between 3.5V and 4.5V, continuous operation of the module in START-UP mode may be necessary, to guarantee sufficient drive to the connected quartz.

Switching between START-UP and RUN modes must not be done in CPU modes PLL or PLL2, as this might lead to unpredictable behaviour of the clock system.

6.3.9. UVDD Analog Registers

ANAU **Analog UVDD Register**

	7	6	5	4	3	2	1	0
r/w	EAL	x	LS		x	x	FVE	VE
	0		0	0			0	0

EAL **Enable RESET/ALARM Interrupt Source output**
r/w1: Enabled.
r/w0: Disabled.

LS **LCK output Select**
w0: PLL Lock Signal.

w1: VDD Regulator Error.
w2: FVDD Regulator Error.
w3: BVDD Regulator Error.

FVE **FVDD Regulator Error Flag**
r1: Out of specification.
r0: Normal operation.
w1: Reset flag.
w0: No action.

VE **VDD Regulator Error Flag**
r1: Out of specification.
r0: Normal operation.
w1: Reset flag.
w0: No action.

6.4. Reset Logic

6.4.1. Alarm Function

The Alarm Comparator on the pin RESETQ allows the detection of a threshold higher than the reset threshold. An alarm interrupt can be triggered with the output of this comparator.

The intended use of this function is made, when a system uses a 5V regulator with an unregulated input. In this case, the unregulated input, scaled down by a resistive divider, is fed to the RESETQ pin. With falling regulator input voltage this alarm interrupt is triggered first. Then the reset threshold is reached and the IC is reset before the regulator drops out.

The time interval between the occurrence of the alarm interrupt and the reset may be used to save process data to non-volatile memory. In addition, power saving steps like turning off stepper motor drivers may be taken to increase the time interval until reset.

6.4.2. Internal Reset Sources

This IC contains four internal circuits that are able to generate a system reset: watchdog, supply supervision, clock supervision and FHR flag.

All internal resets are directed to the open drain output of pin RESETQ. Thus a “wired or” combination with external reset sources is possible. The RESETQ pin is current limited and therefore large external capacitances may be connected.

All internal reset sources initially set a reset request flag. This flag activates the pull-down transistor on the RESETQ pin. An internal reset timer starts, as soon as no internal reset source is active any more. It counts 2048 f_{XTAL} periods (for alternative settings refer to HW options register CR) and then resets the reset request flag, thus releasing the RESETQ pin.

As long as the Reset Comparator on the pin RESETQ detects the low level, the overall IC is reset.

The state of the flags CSW1.FHR, CSW1.CLM, CSW1.PIN, CSW1.POR and CSW1.WDRES, read directly after a system reset, allows to distinguish the cause of this last system reset (Table 6–5).

6.4.2.1. Supply Supervision

A UV_{DD} level below the Supply Supervision threshold VREFPOR, or an overload condition in the internal VDD or FVDD Regulators will permanently pull the pin RESETQ low and thus hold the IC in reset (see Fig. 6–2 on page 57). With HW Option CM.WCM = 0, this reset source can be enabled/disabled by flag CMA in register CSW0 (see Section 6.4.2.2. on page 56).

6.4.2.2. Clock Supervision

The Clock Supervision monitors the frequency at the oscillator input XTAL1 and also the frequency f_{SUP} that is present at the input of the central clock divider (see Fig. 4–1). Frequencies below the clock supervision threshold of approx. 200kHz will permanently pull the pin RESETQ low and thus hold the IC in reset (see Fig. 6–2 on page 57). With HW Option CM.WCM = 0, this reset source can be enabled/disabled by flag CMA in register CSW0.

Frequencies exceeding the specified IC frequency are not detected.

There are two general operation options which can be selected in the HW Options field CM:

1. Flag WCM = 1:
Clock and Supply Supervision are permanently active. They

can not be deactivated. The Watchdog must be serviced by SW. This mode is recommended for all stand-alone applications requiring high operational reliability.

2. Flag WCM = 0:
Clock and Supply Supervision are active after reset, but can be enabled/disabled by the clock monitor active flag CMA of register CSW0. The Watchdog must be serviced only after a first write access to register CSW1. This mode is recommended for test and evaluation purposes only.

6.4.2.3. Watchdog

The Watchdog module serves to monitor undisturbed program execution. A failure of the program to retrigger the Watchdog within a preselectable time will pull the pin RESETQ low and thus reset the IC (Fig. 6–2 and 6–3). With HW Option CM.WCM = 0, this reset source is only enabled after a write access to register CSW1 (see Section 6.4.2.2. on page 56).

The Watchdog (Fig. 6–3) contains a down-counter that generates a reset when it wraps from zero to 0xFF. It is reloaded with the content of the watchdog timer register, when, upon a write access to location CSW1, watchdog trigger registers 1 and 2 contain bit-complemented values. An IC reset resets the watchdog timer register to 0xFF, thus setting the Watchdog to the maximum reset interval.

The three Watchdog registers are programmed by writes to the same location CSW1. First write the desired watchdog timer value (only values between 1 and 255 are allowed):

$$\text{FAST and PLL modes: Value} = \frac{\text{Interval} \times f_{15}}{1} - 1$$

$$\text{SLOW modes: Value} = \frac{\text{Interval} \times f_{15}}{128} - 1$$

On further writes, to trigger a reload of the counter, alternatingly write a retrigger value (routed to trigger register 1) (not necessarily the former timer value) and its bit-complement (routed to trigger register 2) to CSW1. Failure to reload will result in a counter underflow and a Watchdog reset.

Never change the retrigger value. Writing a wrong value to CSW1 immediately prohibits further reloading of the watchdog counter.

The flag CSW1.WDRES is set as soon as the watchdog counter wraps to 0xFF. Thus, it is true after a Watchdog reset. Only a Supply Supervision reset or a write access to CSW1 clears it.

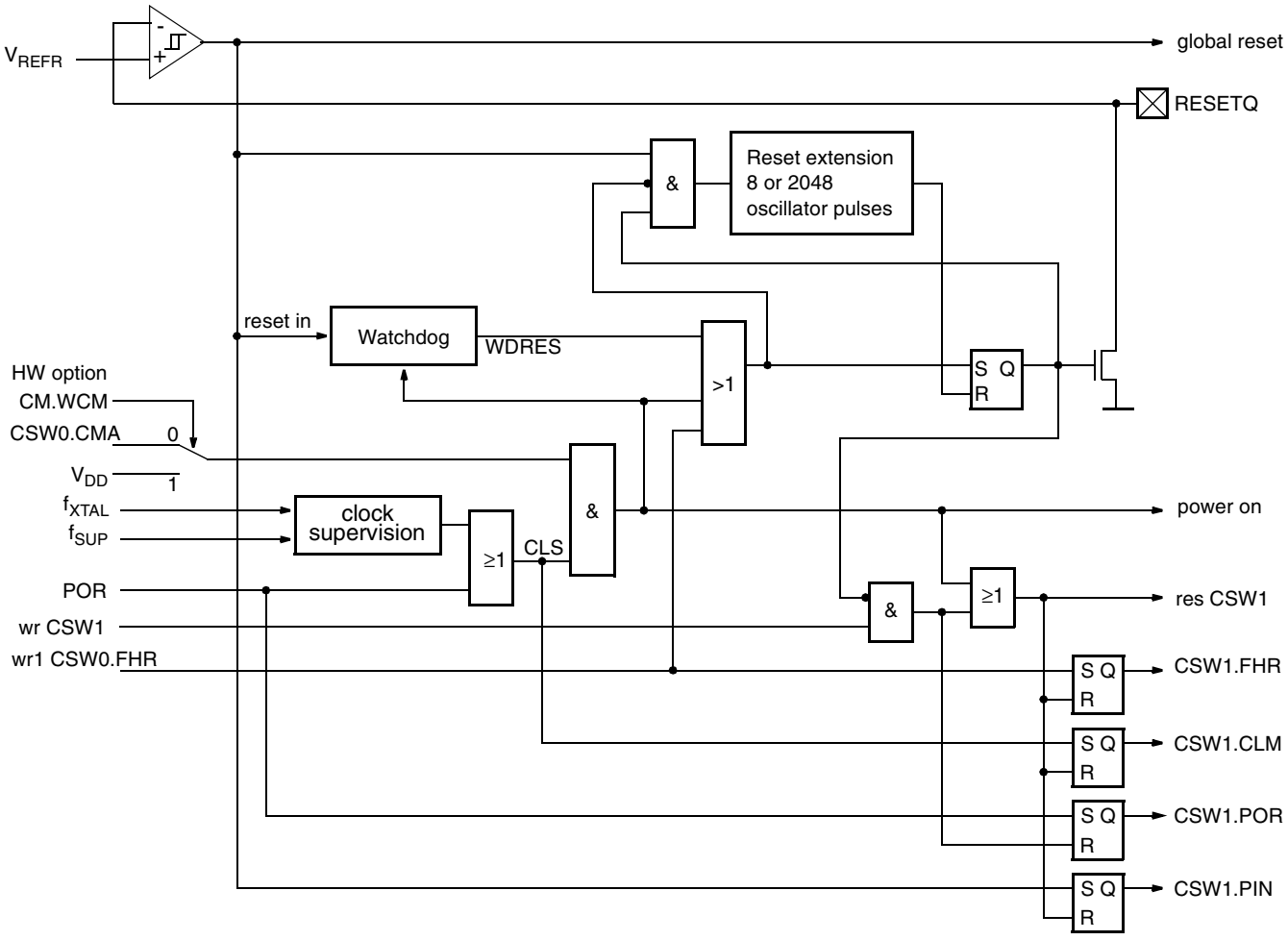


Fig. 6–2: Reset Logic Block Diagram

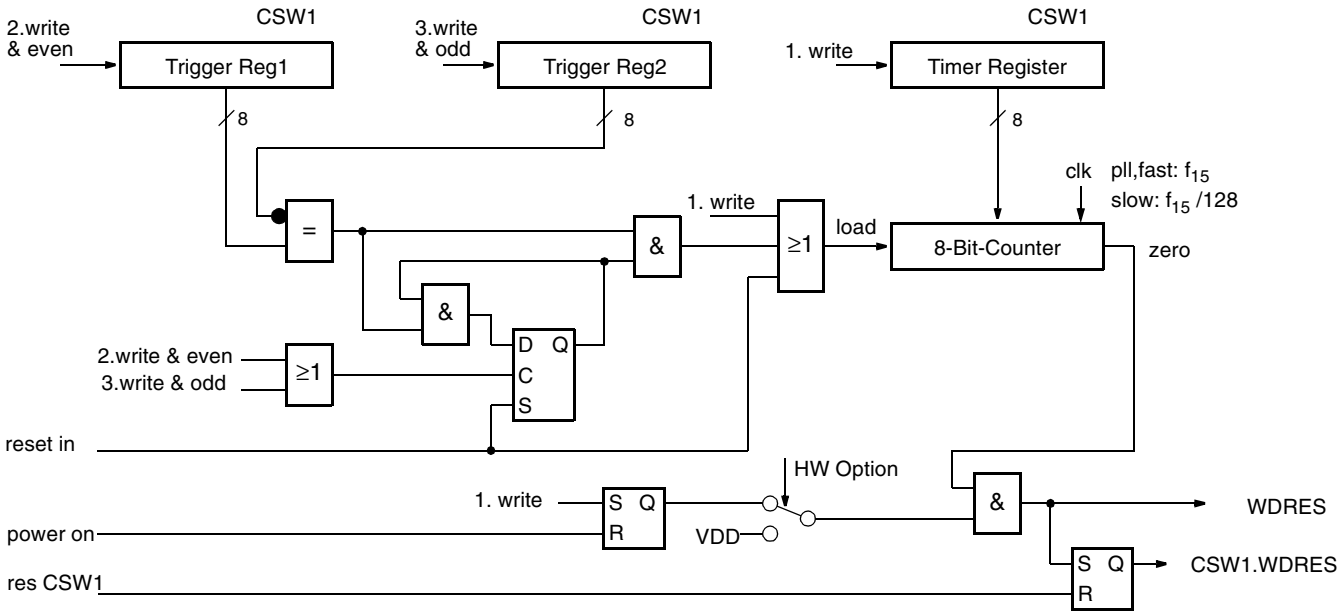


Fig. 6–3: Watchdog Block Diagram

6.4.3. Forced Hardware Reset

Setting flag CSW0.FHR immediately forces the RESETQ pin low. This allows the SW to restart the whole system by HW reset.

6.4.4. External Reset Sources

As long as the Reset Comparator on the pin RESETQ detects the low level, the overall IC is reset. On this pin, external reset sources may be wire-ored with the IC internal reset sources, leading to a system wide reset signal combining all system reset sources.

6.4.5. Summary of Module Reset States

After reset the IC modules are set to the reset state (Fig. 6–4)

Table 6–4: Status after Reset

Module	Status
CPU	CPU Fast mode (f_{OSC}).
Interrupt Controller	Interrupts are disabled. Priority registers, request flip flops and stack are cleared.
U-Ports	Normal mode. Output is tristate.
High current ports	Normal mode. Output is low.
LCD module	Registers are reset. No display.
Watchdog	Depends on mask option. EMU option: Switched off. SW activation is possible. Stand-alone option: Permanently active.
Clock monitor	Depends on mask option. EMU option: Active. SW may toggle. Stand-alone option: Permanently active.

6.4.6. Reset Registers

CSW0 Clock, Supply & Watchdog Register 0

	7	6	5	4	3	2	1	0	
w	FHR	x	x	x	x	x	x	CMA	
	0	x	x	x	x	x	x	1	Res

This register controls the Supply and Clock Supervision modules and allows to force a system reset.

FHR **Forced Hardware Reset**
w1: Reset forced
w0: no action

CMA **Clock and Supply Monitor Active**
w1: Both Enabled.
w0: Both Disabled.
Can be written to zero only after power on reset or clock supervision reset and before first write access to register CSW1 if allowed by HW option.

CSW1 Clock, Supply & Watchdog Register 1

	7	6	5	4	3	2	1	0	
r	TST	x	x	FHR	CLM	PIN	POR	WDRES	
	-	-	-	0	0	0	0	0	Res

The Reset state in the register frame above describes the state after a write to register CSW1.

TST **TEST Pin State**
r1: TEST is 1.
r0: TEST is 0.

FHR **Force Hardware Reset** (Table 6–5)

CLM **Clock Supervision Reset** (Table 6–5)

PIN **RESETQ Pin Reset** (Table 6–5)

POR **Supply Supervision Reset** (Table 6–5)

WDRES **Watchdog Reset** (Table 6–5)

Table 6–5: Source of last Hardware Reset

FHR	CLM	PIN	POR	WDRES	Source
0	0	1	0	0	external from RESETQ pin
0	0	1	0	1	internal Watchdog Reset
0	1	1	0	0	internal Clock Supervision Reset
0	1	1	1	0	internal Supply Supervision Reset
1	0	1	0	0	internal Forced Hardware Reset
The registers sum up the source of all HW resets that ocurred since the last write to register CSW1. Any write access to CSW1 resets all flags to 0.					

CSW1 Clock, Supply & Watchdog Register 1

	7	6	5	4	3	2	1	0	
w	Watchdog Time and Trigger Value								
	1	1	1	1	1	1	1	1	Res

This register controls the Watchdog module. Only values between 1 and 255 are allowed.

6.5. Test Registers

Test registers are for manufacturing test only. They must not be written by the user with values other than their reset values (00h). They are valid independent of the TEST input state.

In all applications where a hardware reset may not occur over long times, it is good practice to force a software reset on these registers within appropriate intervals.

TST1 Test Register 1

	7	6	5	4	3	2	1	0	
w	For testing purposes only								
	0	0	0	0	0	0	0	0	Res

TST2 Test Register 2

	7	6	5	4	3	2	1	0	
w	For testing purposes only								
	0	0	0	0	0	0	0	0	Res

TST3 Test Register 3

	7	6	5	4	3	2	1	0	
w	For testing purposes only								
	0	0	0	0	0	0	0	0	Res

TST4 Test Register 4

	7	6	5	4	3	2	1	0	
w	For testing purposes only								
	0	0	0	0	0	0	0	0	Res

TST5 Test Register 5

	7	6	5	4	3	2	1	0	
w	For testing purposes only								
	0	0	0	0	0	0	0	0	Res

TSTAD2 Test Register AD2

	7	6	5	4	3	2	1	0	
w	For testing purposes only								
	0	0	0	0	0	0	0	0	Res

TSTAD3 Test Register AD3

	7	6	5	4	3	2	1	0	
w	For testing purposes only								
	0	0	0	0	0	0	0	0	Res

7. JTAG Interface

This module provides JTAG style access to 5 internal scan chains. These allow testing, debugging, EmbeddedICE and ETM (Embedded Trace Module) programming. The scan chains are controlled by a JTAG style Test Access Port (TAP) controller. For further details on operating TAP controller, EmbeddedICE and ETM, please refer to ARM7TDMI Data Sheet (Document Number: ARM DDI 0029), Embedded Trace Macrocell Specification (Document Number: ARM IHI 0014) and ETM7 Technical Reference Manual (Document Number: ARM DDI 0158).

Features

- 2 Interfaces selectable
- Access to CPU periphery
- Access to EmbeddedICE
- Access to Embedded Trace Module

7.1. Functional Description

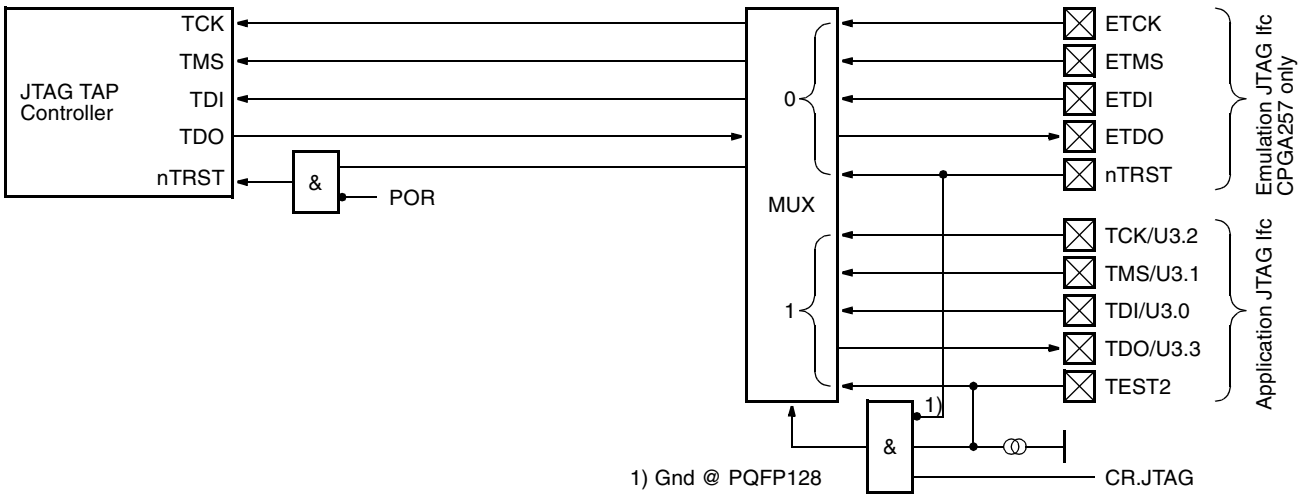


Fig. 7–1: JTAG Interface Block Diagram

The TAP controls the access to the scan chains. Scan chain 0 allows access to the entire periphery of the CPU. Scan chain 1 is a subset of the scan chain 0. Scan chain 2 allows programming of the EmbeddedICE debug module. Scan chain 3 is reserved for the boundary scan of the pads of the packaged device. Scan chain 6 allows programming of the ETM.

Table 7–1: Scan Chains

Number	Size [Bit]	Function
0	105	ARM7 Macrocell
1	33	Part of scan chain 0
2	38	EmbeddedICE
3	-	reserved for Boundary scan
6	40	ETM

Two interfaces can be selected to access the TAP controller. The selection has to be done by the control register flag CR.JTAG and the pins TEST2 and nTRST.

7.1.1. Application JTAG Interface

The application JTAG interface is connected to the special inputs and outputs of U-Ports. The U-Port for the signal TDO has to be configured as special out, those for the signals TCK, TMS and TDI as special in. The application JTAG interface is available if enabled and the external circuit layout allows it. It is enabled if the TEST2 pin is high, the nTRST pin is low and the flag CR.JTAG is set to one. The TEST2 pin is the nTRST input of the application JTAG interface.

If TEST2 pin is high during reset, U-Port U3.3 (= JTAG TDO) is forced to Port, Special, Output mode until programmed by SW. Otherwise the emulation JTAG interface couldn't be operated without internal SW support. To avoid conflicts between JTAG mode and SW control on this port bit, never mix these two modes in one application. The application SW must not initialize the involved U-Ports if flag CR.JTAG is set to one.

7.1.2. Emulation JTAG Interface

The emulation JTAG interface is connected to dedicated pins of the emulation parts (CPGA257 package). Series parts (PQFP128 package) do not provide this interface. It is enabled as long as the application JTAG interface is disabled.

7.1.3. Boundary Scan

The boundary scan is not implemented in this IC.

7.1.4. Pin TEST2

The pin TEST2 is weakly pulled down to UVSS by the current Ipd. Refer to section “Electrical Characteristics” for details. Besides JTAG, the pin TEST2 controls the behavior of the IC during reset. Refer to section “Core Logic” for further details.

7.2. External Circuit Layout

The emulation JTAG interface uses TTL level input comparators. The emulation JTAG inputs ETCK, ETMS, ETDI and nTRST need external pull-up resistors to EVDD. This has to be done in a way, that the TAP controller sees a logic one if the emulation JTAG interface is enabled but not driven.

The application JTAG interface shares its input and output pins with the I/O of U-Ports. The external circuit layout has to be done carefully in order to guarantee functionality of the JTAG interface. As long as the application JTAG interface is enabled and not driven, the TAP controller inputs TMS and TDI shall see logic one level. If it is enabled and driven, the external application circuit shall not influence proper operation of the JTAG interface. The external host must be able to drive the levels at the inputs TCK, TMS and TDI to CMOS logic one and logic zero levels and it must be the only source of these signals. The TAP controller must be able to drive the output TDO to both CMOS levels, logic one and zero, and must be the only source of this signal.

Common JTAG tools expect to see pull-up resistors at nTRST (TEST2), TCK,TMS and TDI.

7.3. JTAG ID

The JTAG ID is not implemented in this IC.

The JTAG TAP controller contains a HW coded JTAG ID which can be read serially via the JTAG interface. The CPU can’t access this ID.

Bits 1 to 19 are manufacturer defined. Bits 0 and 20 to 31 are ARM defined.

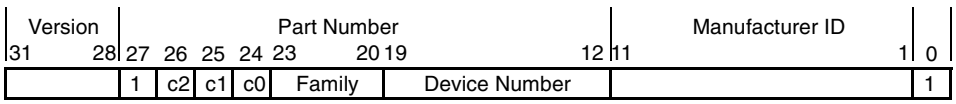


Fig. 7–2: JTAG ID Format

Bit 31 to 28 Version
0: ARM core revision 0.
1: ARM core revision 1.
2: etc.

Bit 27
0: ARM core ID.
1: Non ARM core ID.

Bit 26 Capability bit 2
0: Standard part.
1: ‘E’ part.

Bit 25 Capability bit 1 (Reserved)

Bit 24 Capability bit 0
0: Hard macro.
1: Synthesisable.

Bit 23 to 20 Family
7: ARM7.
9: ARM9.
A: ARM10.
etc.

Bit 19 to 12 Device Number
Manufacturer device number 0 to 255.

Bit 11 to 1 Manufacturer ID
Manufacturer ID is the compressed JEDEC code (0x06C).

Bit 0 Marker
Fixed value.

The necessity of using bits 19 to 12 as manufacturer device number forces us to use the Non ARM core ID format of the JTAG ID. This is the reason why some debug tools can’t use auto configuration, but must be configured by the user for the correct core and revision.
The part number shall be selected in a way that no two component types in the same package with TAP pins in the same location have the same part number.

8. Embedded Trace Module (ETM)

This module provides instruction and data trace capability. The ETM is controlled by a JTAG style Test Access Port (TAP) controller. For further details on the installed Rev1A please refer to Embedded Trace Macrocell Specification (Document Number: ARM IHI 0014) and ETM7 Technical Reference Manual (Document Number: ARM DDI 0158).

Features

- Instruction trace
- Data trace
- Trace before, about, after trigger
- Trigger and filter capabilities
- Access to Embedded Trace Module
- Normal trace data format
- Full-rate and half-rate clocking
- 4/8/16bit maximum port width

8.1. Functional Description

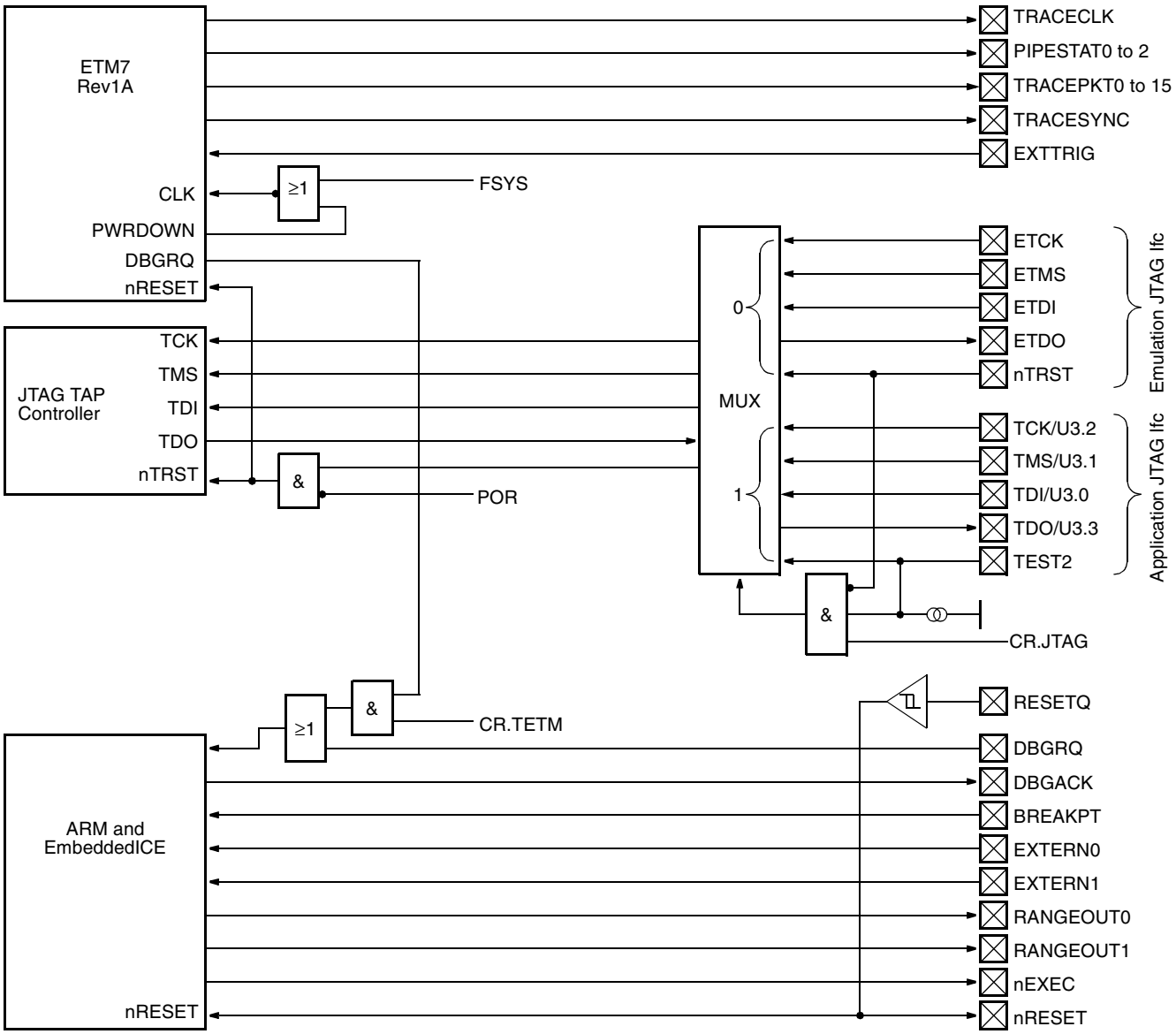


Fig. 8–1: ETM Interface Block Diagram

The ETM is controlled via scan chain 6 of the JTAG interface.

The process of remapping or loading code to RAM and execute it there is a problem for the ETM because one address can contain different code (overlay). The solution is based on the requirement that the memory map into which overlays are loaded exists in multiple places in the address space.

The memory controller of the IC decodes the 24 LSB address lines A0 to A23. This results in an memory map of 16 MByte. This memory map is repeated 256 times within the 32 bit ARM core address space of 4 GByte.

Thus it is possible to have one static image of the code being executed for the trace tool, with different possible overlays statically linked into the appropriate area of the address space.

Loading code into the RAM and execute it there means, copy the code into the RAM and then jump to its overlay. The ETM sees the full 32 bit address and reports this jump to the trace tool which has the static image with a memory map for each configuration at different places of its address space. The memory controller sees the 24 lower address lines only, therefor the jump is directed to the correct location.

The supported trace features are listed in Tabel 8–1.

Table 8–1: Trace Features

Features	Supported
Demultiplexed trace data format	-
Multiplexed trace data format	-
Normal trace data format	✔
Full-rate clocking	✔
Half-rate clocking	✔
Maximum port width	4/8/16-bit

9. IRQ Interrupt Controller Unit (ICU)

The Interrupt Controller Unit manages up to 63 interrupt sources. Each interrupt source has its own interrupt vector pointing to an interrupt service routine. One of 16 priorities can be assigned to each channel or it can be disabled. The Interrupt Controller Unit is connected to the nIRQ input of the CPU.

Features

- Expanding nIRQ input of ARM7TDMI
- Up to 63 interrupt sources (39 implemented)
- 16 priority levels
- HW vectoring
- HW prioritization
- HW stacking of priority levels
- 2 cycles maximum from input to CPU nIRQ

9.1. Functional Description

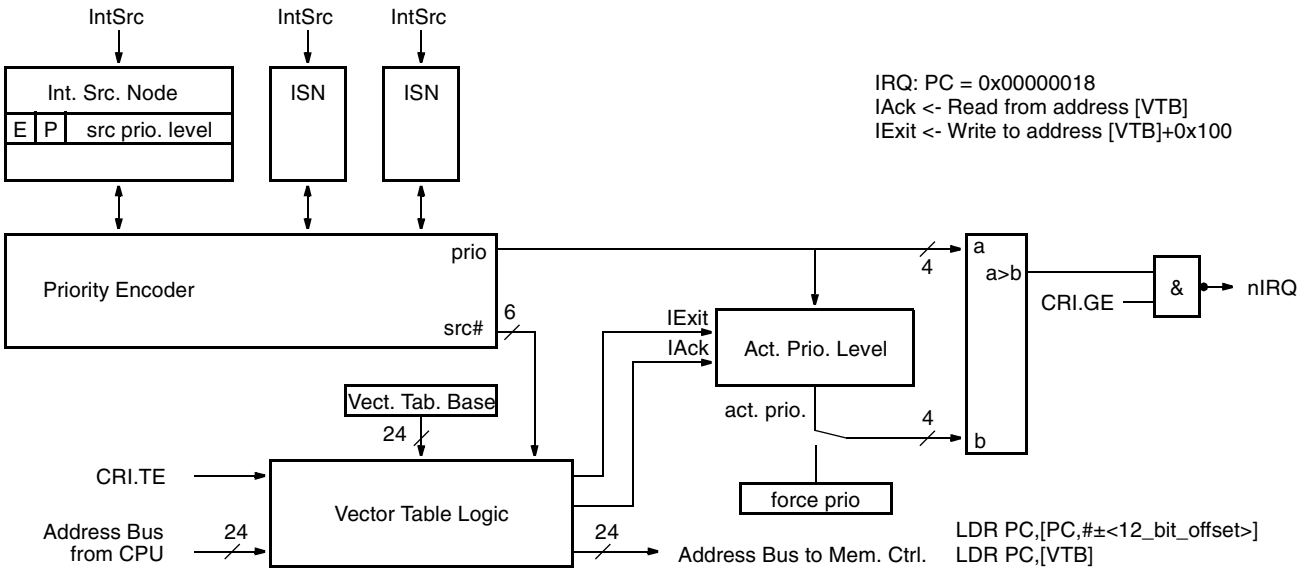


Fig. 9–1: Block Diagram

The Interrupt Controller Unit (ICU) is composed of an Interrupt Source Node (ISN) for each interrupt source, of a Priority Encoder, of a Vector Table Logic, of an Active Priority Level Logic and a comparator (Fig. 9–1).

Each falling edge of an interrupt source signals an interrupt request to its ISN and sets its Pending flag P (Fig. 9–2). Besides the P flag each ISN consists of an Enable flag (E) and a Source Priority register containing the priority of the corresponding interrupt source. As long as both flags (E and P) are true, the ISN outputs its priority. Otherwise it outputs the lowest priority (that is no priority).

The Priority Encoder outputs number and priority of the ISN with the highest active priority. If several ISNs with the same priority are active at the same time, the ISN with the lowest source number is selected, thus the ISNs are operated in a HW defined order. The interrupt vector table contains the start addresses of the interrupt service routines (ISR). The Vector Table Base register points to the first entry of the interrupt vector table. Thus the location of the interrupt vector table is programmable to any memory location. This allows easy switching between different tables.

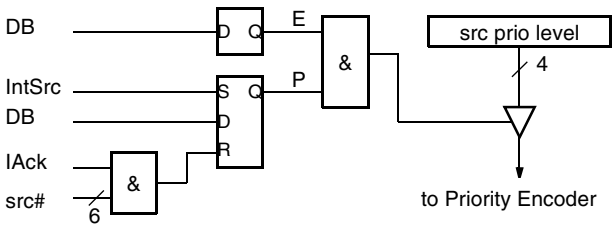


Fig. 9–2: ISN Flags

The Active Priority Level Logic outputs the priority of the currently running task (lowest priority is the background task). The comparator activates its output if this priority is lower than the priority output from the Priority Encoder.

If the ICU's output is enabled by the Global Enable flag (GE) the nIRQ input of the CPU is activated and held active until acknowledged. The IRQ is granted by the CPU as soon as the CPU internal IRQ flag (flag I in CPU register CPSR) is enabled by SW. In the meantime between interrupt activation in the ICU and granting by the CPU, higher priority interrupt requests may be signaled to the ICU, raising the priority output of the Priority Encoder.

The SW has to read the address where the Vector Table Base register points to ([VTB]) in order to get the start address of the ISR for the ISN with the currently highest active priority (Fig. 9–3). A data fetch from this location generates an internal interrupt acknowledge signal (IAck). With IAck the Active Priority Level Logic accepts the new priority and internally saves the priority of the interrupted task. IAck clears the P flag in the corresponding ISN and deactivates the nIRQ output. The ICU is ready for new interrupts now.

Before leaving the interrupt service routine, the SW has to write to the address where VTB points to plus 0x100 ([VTB]+0x100). A write to this location generates an internal interrupt exit signal (IExit). With IExit the Active Priority Level Logic internally deletes the priority of the current task and outputs the priority of the interrupted task where the immediately following return instruction jumps to.

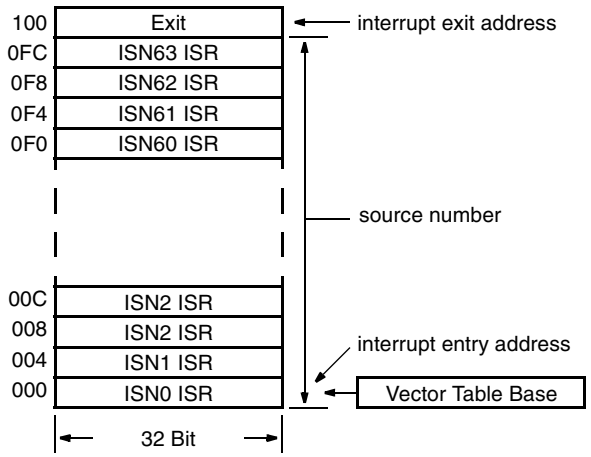


Fig. 9–3: Interrupt Vector Table

Each ISN has a dedicated source number. A maximum of 64 ISNs can be connected to the Priority Encoder. The Priority Encoder outputs source number 0 as long as all ISNs output priority 0 or no ISN is active or the comparator output is inactive. This is to guarantee a valid state of the Priority Encoder and return a valid start address even if no interrupt source is active. The corresponding vector is the first in the vector table (default vector). For this reason ISN0 can't be used for connecting an interrupt source, because ISN0 is not the only user of the corresponding interrupt vector. For example, reading the address location pointed to by the Vector Table Base register while nIRQ is inactive will return the ISR start address of ISN0.

Additional to the ISNs whose inputs are connected to a HW module, some ISNs are necessary whose inputs are not connected or unused. Those interrupts can be activated by SW solely (delayed interrupt).

The output of the Active Priority Level Logic may be forced by writing a higher priority to the Forced Priority register. This allows temporary raising of the priority of the currently running task. Writing the maximum priority to the Forced Priority register is another way to disable the ICU because no ISN can generate an IRQ. Raising of the priority in this way does not take effect as long as nIRQ is active.

The Global Enable (GE) signal at the output of the comparator disables the ICU output. It is impossible to inactivate an active nIRQ output by modifying an ISN, the GE flag or forcing the priority. Only IAck resets the nIRQ output.

The size of the ICU can be scaled in steps of 8 ISNs. This IC has 40 Interrupt Source Nodes implemented (ISN0 to ISN39). Derived parts can contain 40, 32 (ISN0 to ISN31), 24 (ISN0 to ISN23) or less ISNs.

The Pending flags P in the ISNs are operating even when the ICU is disabled (CRI.GE = 0). To be exact, only the ICU output is disabled. This avoids further interrupts. Interrupted ISRs will be finished and the Act. Prio. Level stack will be handled properly if those ISRs generate IExit before returning.

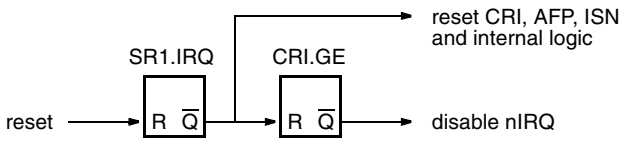


Fig. 9–4: Reset Structure

Figure 9–4 shows the reset structure. Registers can't be written until the IRQ flag in the standby register SR1 is set. The pending flags P in the ISNs are not reset by the standby register. It can be operated by HW even while SR1.IRQ is zero. Reading and writing of the P flags is impossible unless SR1.IRQ is set to one.

Table 9–1: Interrupt Assignment

ISN	Interrupt Source
0	Default vector, not connected
1	CC0OR
2	CC1OR
3	PINT0
4	PINT1
5	CAN0
6	SPI0
7	Timer 1
8	Timer 0
9	P06 COMP
10	RESET/ALARM
11	WAIT COMP
12	UART0
13	PINT2
14	reserved for WAPI
15	CC2OR
16	CC3OR
17	Timer 2
18	reserved for RTC
19	I2C0
20	Timer 3
21	SPI1
22	COMMRX
23	COMMTX
24	PINT3
25	DIGITbus
26	I2C1
27	CAN1
28	CC4OR
29	CC5OR
30	Timer 4
31	UART1

Table 9–1: Interrupt Assignment

ISN	Interrupt Source
32	PINT5
33	CAN2
34	CC0COMP
35	CC1COMP
36	CC2COMP
37	CC3COMP
38	PINT4
39	GBus

9.2. Timing

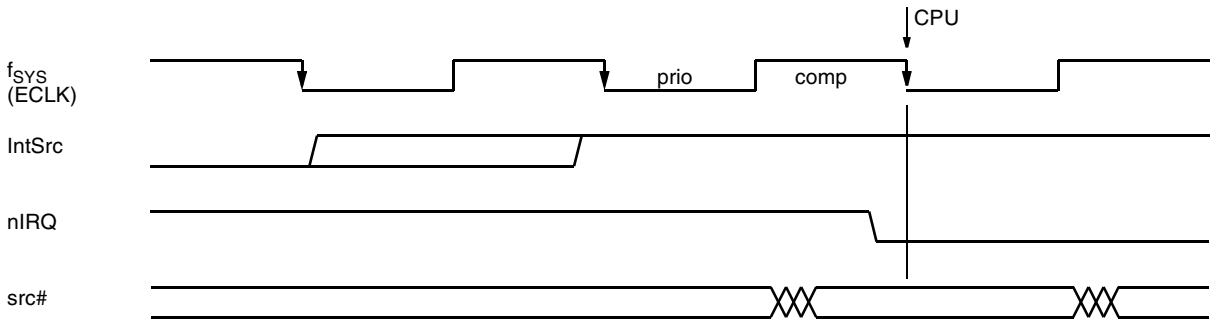


Fig. 9–5: Timing

The sample period of an incoming interrupt request lasts one cycle in the worst case. It is sampled by an ISN with the falling edge of f_{SYS}. Priority Encoder and comparator require another cycle. The CPU finally evaluates with the next falling edge of f_{SYS}.

This results in a maximum delay of 2 f_{SYS} cycles from request to CPU input.

9.3. Registers

CRI Control Register IRQ

	7	6	5	4	3	2	1	0	
r/w	GE	TE	x	x	x	x	x	x	
	0	0	x	x	x	x	x	x	Res

GE Global Enable
r/w1: Enable IRQ.
r/w0: Disable IRQ.
Disabling happens as soon as nIRQ is inactive. An active nIRQ will not be interrupted by writing a zero to GE.

TE Table Enable
r/w1: Enable.
r/w0: Disable.
The Vector Table Logic doesn't work if TE is disabled. Neither the correct ISR start address is returned nor the internal signals IAck and IExit are generated on accessing the dedicated memory location.

AFP Actual and Forced Priority Register

	7	6	5	4	3	2	1	0	
r/w	APRIO				FPRIO				
	0	0	0	0	0	0	0	0	Res

APRIO Actual Priority
r: (Table 9–3)
This field indicates the programmed priority of the actually running ISR. It is modified by HW only.

FPRIO Forced Priority
r/w: (Table 9–3)
Writing a value higher than the APRIO value to this location raises the priority of the actual running ISR. It doesn't change APRIO. Only ISRs with a priority higher than the forced priority are able to interrupt now.

It is necessary to first save the original FPRIO value before raising the own priority by overwriting FPRIO. The saved FPRIO value has to be restored before ISR exit.

PEPRIO Priority Encoder Priority output

	7	6	5	4	3	2	1	0	
r	x	x	x	x	Priority				
	x	x	x	x	0	0	0	0	Res

This register shows the priority of the highest pending and enabled interrupt source.

PESRC Priority Encoder Source output

	7	6	5	4	3	2	1	0	
r	x	x	Source						
	x	x	0	0	0	0	0	0	Res

This register shows the number of the highest pending and enabled interrupt source.

VTB Vector Table Base

	7	6	5	4	3	2	1	0	Offs
r/w	0	0	0	0	0	0	0	0	3
r/w	Address bit 23 to 16								2
r/w	Address bit 15 to 9							0	1
r/w	0	0	0	0	0	0	0	0	0
	0x00000000								Res

The register VTB has to be programmed with the memory base address of the interrupt vector table. The interrupt vector table has to start at an even page address (9 LSB are zero) and is not longer than one page (256 bytes). Besides the start address of the interrupt vector table VTB defines two addresses which perform HW actions when accessed and CRI.TE is set.

Every word read access to the location addressed by VTB deactivates the nIRQ output. If the comparator output is active, the internal signal IAck is activated, which returns the ISR start address of the ISN with the highest active priority, clears the corresponding P flag and saves the interrupted priority.

Every word write access to the location addressed by VTB plus 0x100 activates the internal signal IExit.

Accessing these locations ([VTB] and [VTB]+0x100) without generating IAck or IExit is possible when the Vector Table Logic is disabled (CRI.TE = 0).

ISNx Interrupt Source Node Register x

	7	6	5	4	3	2	1	0	
r/w	M	P	E	x	PRIO				
	0	x	0	x	0	0	0	0	Res

M **Modify Pending Flag** (Table 9–2)
w1: Modify Pending flag.
r/w0: Don’t modify Pending flag.
This flag is modified by SW only and always reads as 0. It allows modification of register ISNx without influence to flag P. Without this flag a HW modification of flag P could be corrupted by a simultaneous read-modify-write of register ISNx.

P **Pending** (Table 9–2)
r/w1: Interrupt is pending.
r/w0: No interrupt pending.
This flag can be modified by HW and SW. It is set by HW when the corresponding interrupt source input is activated. If this interrupt source node is enabled, this flag is cleared by HW as soon as the corresponding ISR is called.

Table 9–2: Pending Flag Access

M	P	Read	Write
0	0	Not pending	Don’t modify P
0	1	Pending	
1	0	Not possible	Clear P
1	1		Set P

E **Enable**
r/w1: Enable interrupt.
r/w0: Disable interrupt.
This flag is modified by SW only.

PRIO **Interrupt Source Node Priority**
This field is modified by SW only (Table 9–3).

Table 9–3: Priority Encoding

PRIO				Priority number
3	2	1	0	
0	0	0	0	0 (No priority)
0	0	0	1	1 (Lowest priority)
0	0	1	0	2
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15 (Highest priority)

9.4. Principle of Operation

9.4.1. Reset

Clearing standby register flag SR1.IRQ resets the ICU (see Fig. 9–4 on page 66). The registers are reset to their mentioned values (see Section 9.3. on page 68) and cannot be modified. The nIRQ output is inactive and the actual priority level logic is cleared.

9.4.2. Initialization

Proper configuration of the interrupt sources in the peripheral modules has to be made prior to initialization of the ICU.

Initialization is possible after the standby register flag SR1.IRQ has been written to one. Now the registers can be modified by SW. But no interrupt request is generated to the CPU.

Install the vector table beginning at an even page address (9 LSB are zero). Each entry has to be a 32 bit start address of an interrupt service routine. The vector table has to be located near (±4kB) the load PC instruction. Write the start address of the vector table to the Vector Table Base register VTB. Further access to register VTB is not necessary until you want to switch to another vector table at another location.

Set up the Interrupt Source Node registers ISNx with the necessary priority and enable them. The pending flags have to be cleared, because they are not cleared by SR1.IRQ and are operative all the time. Clearing an active pending flag and enabling the corresponding ISN must not be done with a single instruction. This might lead to an unwanted (spurious) interrupt which is directed to the default vector. First clear P and then set E in two instructions. Interrupt sources which shall not generate interrupts must not be enabled and need no priority (PRIO=0), but can be operated by polling and resetting the pending flag P by SW.

9.4.3. Operation

The ICU is operable in all CPU modes.

Setting both flags CRI.GE and CRI.TE enables the ICU at last. When an interrupt occurs, execution starts at address 0x18. For proper operation of the ICU the jump to the interrupt service routine has to be done by the PC relative load PC instruction
LDR PC,[PC,#<12_bit_offset>],
where the operand [PC,#<12_bit_offset>] must point to the first entry of the vector table. Due to the 12_bit_offset the vector table has to be located within ±4kB from the above instruction. Above instruction is called vectoring. There are two possibilities for the point of time, direct and delayed, when vectoring takes place.

9.4.3.1. Direct Vectoring

Above instruction is the first instruction which is executed when an interrupt occurs. The address 0x18 contains the PC relative load PC instruction.

9.4.3.2. Delayed Vectoring

Above instruction is delayed. The address 0x18 contains a jump to a short piece of code which does all what has to be done for every ISR (Save LR, SPSR and working registers). After this common prefix the jump to the appropriate ISR is launched by the PC relative load PC instruction.

9.4.4. Inactivation

An interrupt source can be disabled locally by clearing the enable flag E in the corresponding ISN register. Even a pending interrupt can be disabled this way. A disabled ISN does not participate in sending interrupt requests to the CPU.

All interrupt sources can be disabled globally by clearing the global enable flag CRI.GE. It is impossible to inactivate an active nIRQ output signal by clearing CRI.GE. An active nIRQ will be served and only further IRQs can be suppressed by setting the GE flag.

The pending flag P stays operative in both cases and may be polled by SW.

A zero in the standby register flag SR1.IRQ immediately resets registers and logic and forces the nIRQ output to inactive.

9.5. Application Hints

9.5.1. Hardware Triggered Interrupts

Normally the connected peripheral modules are setting the pending flag P. If the ISN is enabled (E=1) and the priority is not zero, an IRQ is generated. The P flag will be reset as soon as the corresponding interrupt service routine is called. It is not required and should be avoided to modify the P flag of those ISNs by SW.

9.5.2. Software Triggered Interrupts

Any ISN which is not used by the connected peripheral module can be used for generating IRQ interrupts by SW. It must be avoided that the interrupt source of this ISN is also generating interrupt requests. Either the corresponding peripheral module has to be switched off or its interrupt source output has to be disabled.

The ISN has to be enabled (E=1) and programmed to the desired priority (PRIO>0). Setting the pending flag P by SW generates an interrupt. This interrupt will be processed as soon as possible. When the CPU responds to the interrupt request and jumps to the corresponding ISR, the pending flag is cleared automatically.

9.5.2.1. Delayed Interrupt

Any ISN which is not used by the connected peripheral module can be used for implementing the delayed interrupt mechanism for an operating system. The ISN has to be

enabled (E=1) and programmed to priority 1 (the lowest priority which can generate an interrupt). Setting the pending flag P by OS-SW within a higher priority interrupt service routine generates a delayed interrupt, which is processed after all higher priority interrupts are finished.

9.5.3. Polling

Polling means that the pending flag P is observed by SW. Set by the corresponding interrupt source, the SW recognizes the P flag to be set, calls the corresponding routine and clears the P flag. The ISN should be disabled (E=0), otherwise unwanted IRQs would be generated.

9.5.4. Operating Nested Interrupts

Nested interrupt service routines use common data resources. Every routine, which may have interrupted a lower priority routine, has to save common data resources upon interrupt entry and restore them before returning to the interrupted routine. This is efficiently done by an entry and an exit sequence which are enclosing the interrupt service routine.

9.5.4.1. Interrupt Entry Sequence

The IRQ disable flag I in the core register CPSR is set after an IRQ, thus disabling further IRQs. Before the interrupt is enabled again, the user has to take the following steps:

1. For direct vectoring: Jump to the corresponding interrupt service routine by loading the first element from the vector table into the program counter by an LDR instruction.

2. Save Link Register (R14), SPSR and working registers to stack.

3. For delayed vectoring: Jump to the corresponding interrupt service routine by loading the first element from the vector table into the program counter an LDR instruction.

4. Clear CPSR.I to re-enable IRQs.

Now the actual application ISR can start.

9.5.4.2. Interrupt Exit Sequence

Before returning, it is necessary to clear the interrupt cause. Upon exit from an ISR some actions have to be taken without being interrupted:

1. Set CPSR.I to disable further IRQs.

2. Restore Link Register (R14), SPSR and working registers from stack.

3. Generate the signal IExit by performing a word write by an STR instruction to the interrupt exit address at [VTB]+0x100.

4. Returning to the interrupted routine has to be done by an instruction, which simultaneously writes the PC (R15) and CPSR with the values in R14 and SPSR (e.g. SUBS PC,R14_irq,#4).

9.5.5. Default Vector

Any read access to vector table address [VTB] will deliver the default vector, but will not generate IAck as long as the comparator output is inactive or the priority output of the priority encoder is zero. Due to this the default vector ISR runs with the priority of the interrupted routine. This is the only ISR which could be interrupted by itself. As long as this default vector ISR is not programmed reentrant, interrupts should not be re-enabled by clearing the I flag of the CPSR. No IExit shall be generated on interrupt exit by writing to [VTB]+0x100 because there was no IAck at interrupt entry.

Unintentional inactivation of an active comparator output signal can be caused by modifying the ISN which is the only source for the momentary active nIRQ output. This can be done by disabling (E=0), or clearing the P flag, or lowering the priority of this ISN. Those actions may lead to a default vector interrupt.

9.5.6. Debugger

Unintentional access to vector table addresses [VTB] and [VTB]+0x100 can result in malfunction of the interrupt system (HW and SW). If it is necessary, for instance, to dump the vector table, there are two ways to do this without generation of IAck or IExit:

The first way is to clear the flag CRI.TE which controls the vector table logic. Clearing it disables HW actions on accessing above addresses. But ensure that no interrupts are possible while TE is disabled.

The second way is to access above addresses by byte or half word operations only. The HW actions are only generated by word access. Disabling interrupts is not required in the latter case.

9.5.7. Critical Code

Critical code is a sequence of instructions which must not be interrupted, because it modifies common data resources. Protection from being interrupted can be achieved by disabling interrupts during critical code. There are several ways of doing this:

9.5.7.1. ARM core's Interrupt Disable Flag I and F

The ARM core itself provides the interrupt disable bits I and F in the program status register CPSR.

The control bits of the CPSR (I, F and others) can be SW altered only when the processor is in a privileged mode. ARM recommends to modify the CPSR by a read-modify-write instruction sequence in order to leave the reserved bits unchanged.

```
MRS     r0,cpsr
ORR     r0,r0,#I_Bit    ;disable interrupts
MSR     cpsr_c,r0
```

The interesting case is when an interrupt comes in during execution of the MSR instruction. The core commits to taking an interrupt before the instruction being executed completes. Therefore even though an MSR instruction may have written to the CPSR to disable interrupts, the interrupt will still be taken. A NOP between the MSR instruction and the first instruction of the critical code is not necessary. If an interrupt occurs during an MSR instruction, it will return to the instruction immediately following the MSR.

9.5.7.2. Global Enable Flag GE

Protection of critical code can be achieved by disabling the nIRQ output with the global enable flag CRI.GE. The GE flag changes its value in the cycle after the data transfer of the store instruction. In this cycle the next instruction is in the execution stage of the CPU and will be executed. Due to this one NOP is required between the store instruction, which clears CRI.GE, and the first instruction of the critical code.

9.5.7.3. Force Priority

To protect critical code, further IRQ interrupts can be disabled by writing the maximum priority to the forced priority register AFP. Modifying AFP works like clearing the GE flag. One NOP is required between the store instruction, which writes AFP, and the first instruction of the critical code.

9.5.7.4. Disabling via ISN

At last, critical code protection can be achieved by disabling all ISNs by clearing their enable flag E. The priority encoder is calculated at the beginning of a cycle. Due to this, changing an ISN register becomes effective only in the next cycle. Two NOPs are required between the store instruction, which clears the flag E, and the first instruction of the critical code.

9.5.8. Switching an Interrupt Vector

Interrupt service routines of an interrupt source can easily be changed by entering the start address of the new ISR at the corresponding entry of the interrupt vector table.

9.5.9. Switching the Vector Table

It can be switched between different vector tables if they have been installed. Changing the vector table is simply done by writing the base address of the new vector table to register VTB. All subsequent interrupt service routines must relate to this vector table. Due to this, it is necessary for an ISR in such an environment, to read the location of the current vector table from register VTB before accessing it.

Be careful when doing vector table switching within an ISR. Interrupted ISRs could try to do the IExit from an outdated table.

10. FIQ Interrupt Logic

The FIQ Interrupt Logic selects one out of eight interrupt sources as the CPU's nFIQ input. An interrupt request is latched in a pending flag until it is cleared by SW. The output can be disabled.

Features

- Expanding nFIQ input of ARM7TDMI
- 1 of 8 selection
- IRQ or FIQ selectable

10.1. Functional Description

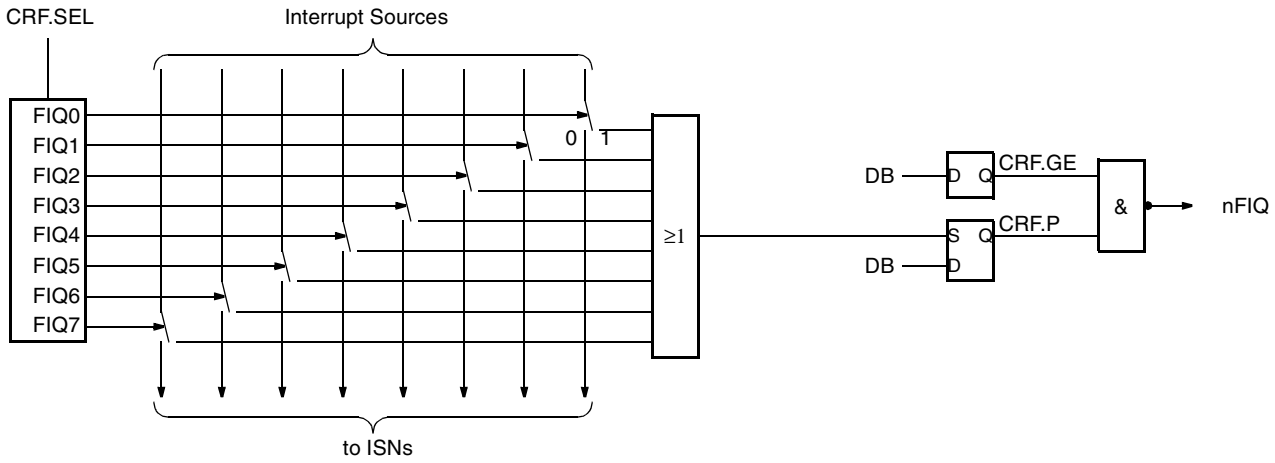


Fig. 10–1: Block Diagram FIQ

At one time, only one interrupt source can be connected to the nFIQ input of the CPU. The interrupt source which is connected to the nFIQ, is disconnected from the corresponding ISN. This ISN can then be used by SW.

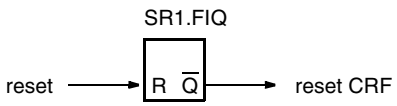


Fig. 10–2: Reset Structure

Figure 10–2 shows the reset structure. Registers can't be written until the FIQ flag in the standby register SR1 is set.

10.2. Registers

PRF	Pending Register FIQ							
	7	6	5	4	3	2	1	0
r/w	x	x	x	x	x	x	x	P
	x	x	x	x	x	x	x	0 Res

P **FIQ Pending**
r/w1: Pending FIQ.
r/w0: No pending FIQ.

This Flag is set by HW and SW. It must be cleared by SW before re-enabling FIQ by bit F in the core's CPSR register, or no further interrupt can occur.

CRF	Control Register FIQ							
	7	6	5	4	3	2	1	0
r/w	GE	x	x	x	SEL			
	0	x	x	x	0	0	0	0 Res

GE **Global Enable FIQ**
r/w1: Enable FIQ.
r/w0: Disable FIQ.
Disabling happens as soon as nFIQ is inactive. An active nFIQ will not be interrupted by clearing GE.

SEL **Select FIQ Source**
r/w: (Table 10–1)

Table 10–1: FIQ Source Selection

SEL				Switched to nFIQ		
3	2	1	0	Select	ISN	Interrupt Source
0	x	x	x	None		
1	0	0	0	FIQ0	6	SPI0
1	0	0	1	FIQ1	11	WAIT COMP
1	0	1	0	FIQ2	12	UART0
1	0	1	1	FIQ3	13	PINT2
1	1	0	0	FIQ4	15	CC2OR
1	1	0	1	FIQ5	17	Timer 2
1	1	1	0	FIQ6	19	I2C0
1	1	1	1	FIQ7	5	CAN0

10.3. Principle of Operation

10.3.1. Reset

Clearing standby register flag SR1.FIQ resets the FIQ Interrupt Logic (see Fig. 10–2 on page 73). The registers are reset to their mentioned values (see Section 10.2. on page 73) and cannot be modified. The nFIQ output is inactive.

10.3.2. Initialization

Proper configuration of the interrupt sources in the peripheral modules has to be made prior to initialization of the FIQ Interrupt Logic.

Initialization is possible after the standby register flag SR1.FIQ has been set. Now the registers can be modified by SW. But no interrupt request is generated to the CPU.

The FIQ Interrupt Logic is operable in all CPU speed modes.

10.3.3. Operation

Setting flag CRF.GE enables the FIQ Interrupt Logic. When an interrupt occurs, execution starts from address 0x1C.

10.3.4. Inactivation

The FIQ Interrupt Logic can be disabled by clearing the global enable flag CRF.GE. An active nFIQ will be served, however, and only future FIQs will be suppressed by clearing the GE flag.

Clearing the standby register flag SR1.FIQ immediately resets registers and logic and forces the nFIQ output to inactive.

11. Port Interrupts

Port interrupts are the interface of the Interrupt Controller to the external world. Six U-Port pins and alternatively six P-Port pins are connected to the module via their special input lines (Fig. 11–1). HW Option programmable multiplexers define which port signal is actually connected to the Trigger Mode Logic (Table 11–1). The P-Ports are actually analog input ports, thus Schmitt Triggers are enabled if the P-Ports are selected as port interrupts. The input sampling frequency is f_{0perm}, which is not disabled by CPU SLOW or DEEP SLOW modes.

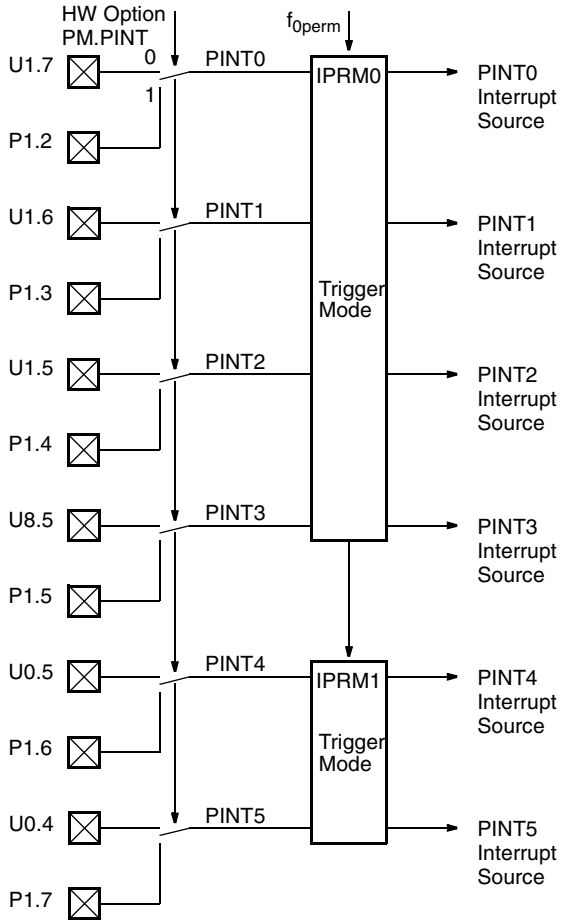


Fig. 11–1: Port Interrupts

The user can define the trigger mode for each port interrupt by the interrupt port mode register.

The Trigger Mode defines on which edge of the interrupt source signal the Interrupt Controller is triggered. The triggering of the Interrupt Controller is shown in figure 11–2.

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

Precautions

Parallel usage of a P-Port as analog and port interrupt input is possible but not recommended. In this case the Schmitt Trigger is enabled. This is the reason why input levels other than ground or digital supply may cause quiescent currents in the Schmitt Trigger circuit and thus lead to higher power consumption.

Table 11–1: Module specific settings

Module Name	HW Options		Initialization	
	Item	Address	Item	Setting
PINT0	Port Multiplexers	PM.PINT	PINT0	U1.7 special in
				P1.2
PINT1			PINT1	U1.6 special in
				P1.3
PINT2			PINT2	U1.5 special in
				P1.4
PINT3			PINT3	U8.5 special in
				P1.5
PINT4			PINT4	U0.5 special in
				P1.6
PINT5			PINT5	U0.4 special in
				P1.7

IRPM0 Interrupt Port Mode Register 0

	7	6	5	4	3	2	1	0	
r/w	PIT3		PIT2		PIT1		PIT0		
	0	0	0	0	0	0	0	0	Res

IRPM1 Interrupt Port Mode Register 1

	7	6	5	4	3	2	1	0	
r/w	x	x	x	x	PIT5		PIT4		
	x	x	x	x	0	0	0	0	Res

PITn Port interrupt trigger number n
This field defines the trigger behavior of the associated port interrupt (Table 11–2).

Table 11–2: PITn usage

PITn	Trigger Mode
0h	Interrupt source is disabled
1h	Rising edge
2h	Falling edge
3h	Rising and falling edges

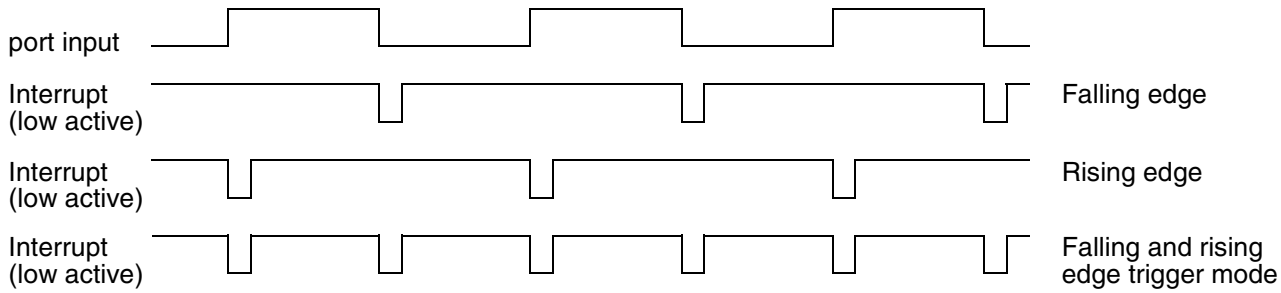


Fig. 11–2: Interrupt Timing

12. Ports

This chapter describes the P-, U- and H-Ports.

The analog input ports, P0 and P1, serve as input for the analog to digital converter and may be used as digital inputs.

P2 may be used as digital input, only.

The universal ports U0 to U8 serve as digital I/O and can be configured as LCD drivers.

The high current ports H0 to H7 serve as digital I/O and can be configured as stepper motor drivers.

12.1. Analog Input Port

The 16 pin analog input port is composed of ports P0 and P1. All port pins can be configured as digital input. P0.6 is connected to a comparator, which may be selected as interrupt source. P1.2 to P1.7 can be used as port interrupts. The 2-pin port P2 solely serves as digital input.

Features

- 16 pin analog input multiplexer.
- 18 pins configurable as digital input ports.
- Schmitt hysteresis digital input buffer, CMOS level (2.5V) or Automotive level (3.3V) selectable.
- 6 pins configurable as port interrupts.

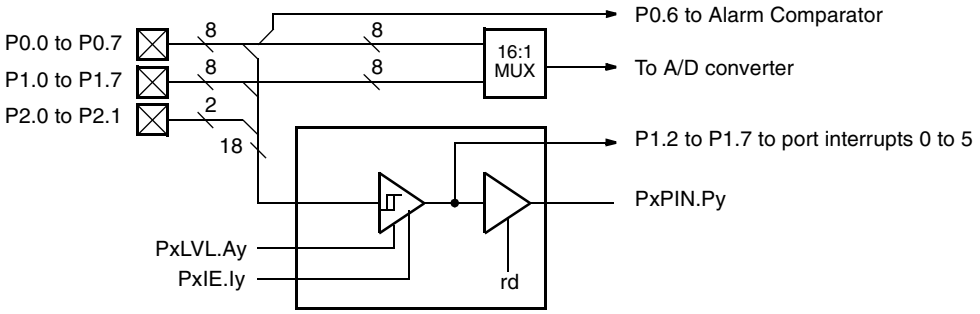


Fig. 12–1: P-Ports with Input Multiplexer and P0.6 Alarm Comparator

P0 and P1 analog input lines are connected to a multiplexer. The output of this multiplexer is connected to the 10-bit A/D converter.

Port P0.6 is, in addition, the input of the P0.6 Alarm Comparator, described in the chapter on the Analog Section.

P0 and P1 pins may alternatively, P2 may exclusively be used as digital input if enabled by setting the individual pin's enable flag PxIE.Iy. CMOS or Automotive Schmitt trigger input level may individually be selected by writing registers PxLVL. The digital value of the input pins is obtained by reading registers PxPIN. Disabled inputs read as 1. Pins should either be used as analog or digital inputs, not both at the same time.

Six of the analog input pins (P1.2 to P1.7) may be used as port interrupt input if selected by HW Option PM.PINT (see sections "Port Interrupts" and "HW Options" for more details). Configure as digital input for this operation.

PxPIN Port x Pin Register

	7	6	5	4	3	2	1	0	
r	P7	P6	P5	P4	P3	P2	P1	P0	
	1	1	1	1	1	1	1	1	Res

P0 to 7 **Pin Data 0 to 7**
r: Read Pin state

PxLVL Port x Input Level Register

	7	6	5	4	3	2	1	0	
r/w	A7	A6	A5	A4	A3	A2	A1	A0	
	0	0	0	0	0	0	0	0	Res

A0 to 7 **Automotive Flag 0 to 7**
r/w1: Schmitt trigger input level is Automotive
r/w0: Schmitt trigger input level is CMOS

PxIE Port x Input Enable Register

	7	6	5	4	3	2	1	0	
r/w	I7	I6	I5	I4	I3	I2	I1	I0	
	0	0	0	0	0	0	0	0	Res

I0 to 7 **Digital Input Enable 0 to 7**
r/w1: Enable input buffer
r/w0: Disable input buffer

12.2. Universal Ports U0 to U8

Universal Ports are pin-configurable as SW I/O port, Special Input/Output port (SI/SO) to special internal hardware modules or direct drive of 4:1 multiplexed LCD segment and backplane lines (LCD port).

The output drivers feature a current fold-back characteristic to allow shorting the output and to improve EMI performance.

Features

- Pin-configurable as I/O or Special Port or LCD driver.
- LCD mode: 1:4 multiplex, 5V supply.
- PORT mode: push-pull or open-drain output.
- Two output current fold-back characteristics selectable
- Schmitt hysteresis input buffer, CMOS level (2.5V) or Automotive level (3.3V) selectable.

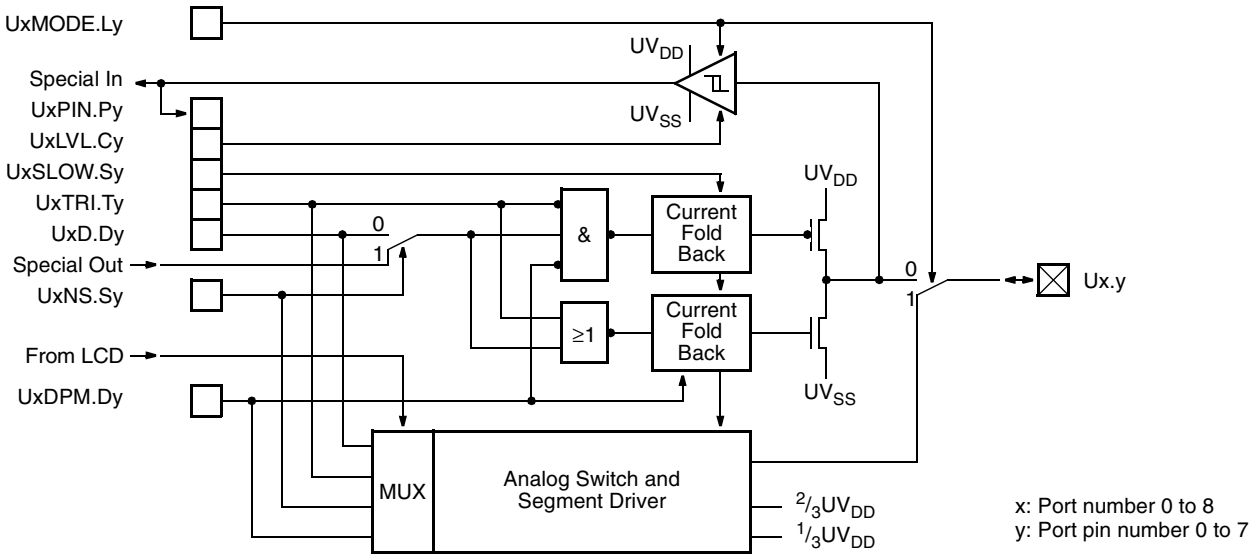


Fig. 12–2: Universal Port Pin Circuit Diagram

The Universal Port pins can be configured for several basic operating modes (Table 12–1)

Table 12–1: Universal Port basic Operating Modes

Modes		Function
Port Mode	Normal Input	The SW uses the port as digital input.
	Special Input	The port input is additionally connected to specific hardware modules.
	Normal Output	The SW uses the port as latched digital tristateable output.
	Special Output	The output signals of specific hardware modules are directly port output source.
LCD Mode		The port pin serves as backplane/segment driver for a 4:1 multiplexed LC display

See the chapter on Pinning for information about specific hardware module connections to individual port pins for Special Input and Special Output purposes.

Universal Port control is distributed among eight registers. Four of these registers have duplicate functions for Port and LCD mode. All register bits corresponding to one U-Port pin are controlled by the same bus bit.

In both LCD and Port modes, the SLOW mode may be defined for each individual U-Port pin. It reduces the current drive capability of the output stage. Set flag SR0.PSLW to enable this operation mode.

After reset, all Universal Ports are in Port, Normal, tristate, CMOS input level condition. SLOW mode is disabled.

12.2.1. Port Mode

For Port mode, the respective UxMODE register bit has to be cleared for mode selection.

The function of the seven remaining registers is given in Table 12–2.

Table 12–2: Register Functions in Port Mode

Register	Function
UxD	r/w Data register
UxTRI	enable/disable output
UxNS	select Data register or specific hardware module as output source
UxDPM	select push-pull or open-drain, double drive mode for output drivers
UxSLOW	enable/disable Port Slow mode for output drivers
UxLVL	select CMOS or Automotive Schmitt trigger input level
UxPIN	read pin state

In Port Mode, the Special Input path is always operative. This allows manipulating the input signal to the specific hardware module through Normal Output operations by software.

Because register UxPIN allows reading the pin level also in Special Output mode, the output state of the specific hardware module may be read by the CPU.

12.2.2. LCD Mode

For LCD Mode, the respective UxMODE register bit has to be set for mode selection.

The function of the seven remaining registers is given in Table 12–3.

Table 12–3: Register Functions in LCD Mode

Register	Function
UxD	r/w phase 0 segment line data
UxTRI	r/w phase 1 segment line data
UxNS	r/w phase 2 segment line data
UxDPM	r/w phase 3 segment line data
UxSLOW	enable/disable Port Slow mode for output drivers
UxLVL	no function
UxPIN	no function

By writing segment line data registers, only a master is changed. Any write to global register ULCDLD will transfer all master settings to the respective slaves and thereby change the LC display in one instant.

Registers UxD, UxTRI, UxNS and UxDPM compose a word-aligned 32bit register and may be accessed by one 32bit operation.

The output sequence timing on backplane and segment output ports in LCD Mode is controlled by the LCD module. Please refer to section LCD Module for information about operation of this module.

As generation of the backplane port output sequence is fully done by the LCD module, no segment line data setting is necessary for these ports.

12.2.3. Port Fast and Slow Modes

Once individual port pins have been enabled for Port Slow mode by setting registers UxSLOW, set flag SR0.PSLW to simultaneously enter this mode in all respective ports.

All U-Ports exhibit two operating regions in the DC output characteristic (see Fig. 12–3). Near zero output voltage the internal driver transistors operate non-limited, to offer a linear, low on-resistance. With larger output voltages, however, the output current folds back to a a limited value. This measure helps to fight supply current transients and related EMI noise during port switching.

In the fold-back region, Port Fast mode and Port Slow mode select two different current limits I_{shf} and I_{shs}. Port Slow mode sets a limit where the output may even be shorted continuously to either supply rail. Thus, wired-or configurations may be realized. The external load resistance should be greater than 5kOhms in Port Slow mode.

For actually switching to Port Slow mode, both registers UxSLOW and SR0.PSLW have to be set. In all other cases, Port Fast mode is selected.

It is recommended to place all LCD ports in Port Slow mode.

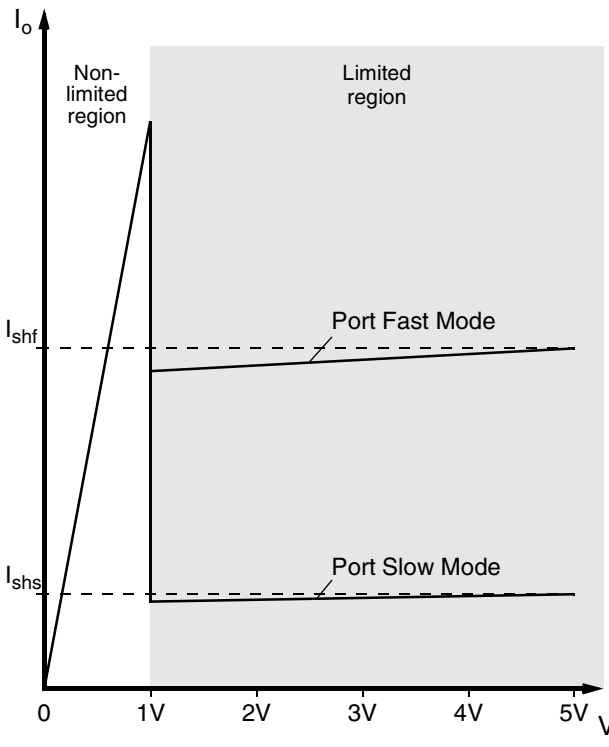


Fig. 12–3: Typical U-Port pull-down DC output characteristic (pull-up characteristic is complementary).

12.3. Universal Port Registers

Eight U-Port registers are basically available for 9 U-Ports U0 to U8, each. Because some U-Ports are less than 8 pins wide, not all of the described bits are available for every port. Furthermore, the respective device's pinning may require a reduction in available U-Ports. See the respective pinning table for details.

The general U-Port register model is given below.

UxMODE Universal Port Mode Register

	7	6	5	4	3	2	1	0	
r/w	L7	L6	L5	L4	L3	L2	L1	L0	
	0	0	0	0	0	0	0	0	Res

L0 to 7 Port Mode Flag
Select the mode of the corresponding port pins.
r/w1: Port pin is in LCD mode.
r/w0: Port pin is in Port mode.

UxD Universal Port x Data / Segment 0 Register

	7	6	5	4	3	2	1	0	
r/w	D7	D6	D5	D4	D3	D2	D1	D0	Port
r/w	SG7_0	SG6_0	SG5_0	SG4_0	SG3_0	SG2_0	SG1_0	SG0_0	LCD
	0	0	0	0	0	0	0	0	Res

D0 to 7 Data Latch
w: Write latch.
r: Read latch.

SG0_0 to 7_3 Segment Data Latch
w: Write latch.
r: Read latch.
In LCD mode, U-Port registers UxD, UxTRI, UxNS and UxDPM store LCD segment information. Segment register bits UxY.SGm_n contain the information for segment line m during phase n, which controls segment m_n. Thus, register bits UxD.SG0_0, UxTRI.SG0_1, UxNS.SG0_2 and UxPIN.SG0_3 contain the complete information for segment line 0 in U-Port x.

Please refer to Pin Assignment and Description for segment/ pin number assignment. Information about the usage of the LCD Segment field will be found at the functional description of the LCD Module.

UxTRI Universal Port x Tristate / Segment 1 Register

	7	6	5	4	3	2	1	0	
r/w	T7	T6	T5	T4	T3	T2	T1	T0	Port
r/w	SG7_1	SG6_1	SG5_1	SG4_1	SG3_1	SG2_1	SG1_1	SG0_1	LCD
	1	1	1	1	1	1	1	1	Res

T0 to 7 Output Tristate Flag 0 to 7
r/w1: Output driver is disabled (tristate)
r/w0: Output driver is enabled

UxNS Universal Port x Normal-Special / Segment 2 Register

	7	6	5	4	3	2	1	0	
r/w	S7	S6	S5	S4	S3	S2	S1	S0	Port
r/w	SG7_2	SG6_2	SG5_2	SG4_2	SG3_2	SG2_2	SG1_2	SG0_2	LCD
	0	0	0	0	0	0	0	0	Res

S0 to 7 Normal/Special Mode Flag 0 to 7
r/w1: Special Mode. Special hardware drives pin.
r/w0: Normal Mode. Data latch drives pin.

UxDPM Universal Port x Double Pull-Down Mode / Segment 3 Register

	7	6	5	4	3	2	1	0	
r/w	D7	D6	D5	D4	D3	D2	D1	D0	Port
r/w	SG7_3	SG6_3	SG5_3	SG4_3	SG3_3	SG2_3	SG1_3	SG0_3	LCD
	0	0	0	0	0	0	0	0	Res

D0 to 7 Double Pull-Down Mode
r/w1: Output driver is pull-down, I_{shs} (Port Slow mode) doubled.
r/w0: Standard.

All U-Port pins may be switched into a Double Pull-down Mode (DPM) by setting the appropriate DPMx flag, where

– the short circuit current I_{shs} is doubled (with Port Slow Mode enabled for these ports, and SR0.PSLW set to 1)

– the output configuration is pull-down, not the standard push-pull.

By these means these ports may be configured to operate as connection to a wired-or, single-wire bus (e.g. DIGITbus or I^2C) with external pull-up resistor.

UxSLOW Universal Port x Slow Mode Register

	7	6	5	4	3	2	1	0	
r/w	S7	S6	S5	S4	S3	S2	S1	S0	
	0	0	0	0	0	0	0	0	Res

S0 to 7 Slow Flag 0 to 7
r/w1: Output driver is in Port Slow mode
r/w0: Output driver is in Port Fast mode

UxLVL Universal Port x Input Level Register

	7	6	5	4	3	2	1	0	
r/w	A7	A6	A5	A4	A3	A2	A1	A0	
	0	0	0	0	0	0	0	0	Res

A0 to 7 Automotive Flag 0 to 7
r/w1: Schmitt trigger input level is Automotive
r/w0: Schmitt trigger input level is CMOS

UxPIN	Universal Port x Pin Register							
	7	6	5	4	3	2	1	0
r	P7	P6	P5	P4	P3	P2	P1	P0
	x	x	x	x	x	x	x	x Res

P0 to 7 **Pin Data 0 to 7**
r: Read Pin state.

ULCDLD	Universal Port LCD Load Register							
	7	6	5	4	3	2	1	0
w	LCDSLV	x	x	x	x	x	x	x
	0	0	0	0	0	0	0	0 Res

LCDSLV **LCD Module is Slave**
Select the mode of the LCD module.
w1: LCD module is slave.
w0: LCD module is master.

A write access to this memory location simultaneously loads all segment information of all U-Ports in LCD mode to the display. The flag LCDSLV is available only in LCD mode.

12.3.1. Special Register Layout of U-Port 4

U4.0 to U4.3 provide backplane signals in LCD Mode. To operate any ports as LCD segment driver it is necessary to switch all these ports to LCD mode. This has to be done by setting flags U4MODE.L0 through U4MODE.L3.

As backplane ports U4.0 to U4.3 require no segment data setting, SG0_0 through SG3_3 bits are not available in U4 registers.

12.4. High Current Ports H0 to H7

High Current Ports 0 to 7 are used to drive coils of stepper motors. All ports are 4 pins wide to facilitate control of individual stepper motors. The H-Ports are similar to universal ports but as the name says, they can drive higher currents. H-Ports can be operated by software like Universal Ports (Port Mode). Their Special Out inputs are connected to the stepper motor module or to PWM outputs.

Features

- Pin-configurable as I/O or Special Port driver
- 30mA output current
- Schmitt hysteresis input buffer, CMOS level (2.5V) or Automotive level (3.3V) selectable.
- Reduced slew rate of current and voltage for driving resistive, capacitive or inductive loads.

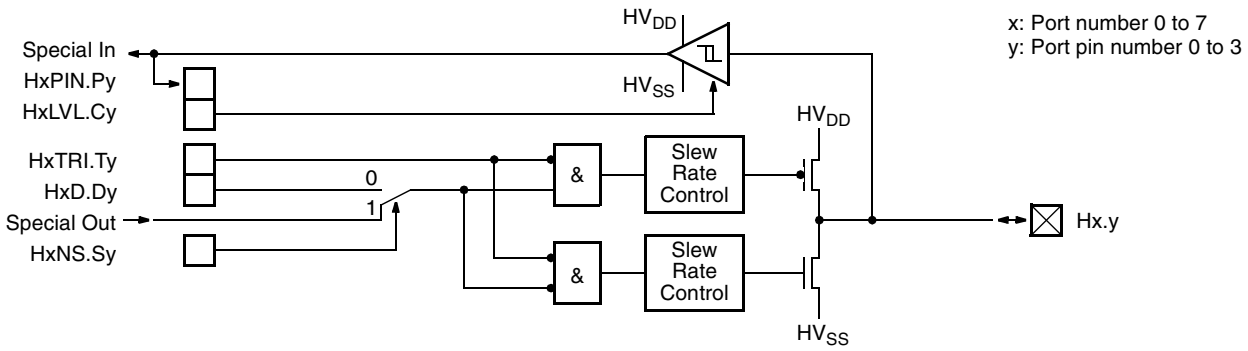


Fig. 12–4: High Current Port Pin Circuit Diagram

The H-Port pins can be configured for several basic operating modes (Table 12–4)

Table 12–4: High Current Port basic Operating Modes

Mode	Function
Normal Input	The SW uses the port as digital input.
Special Input	The port input is additionally connected to specific hardware modules.
Normal Output	The SW uses the port as latched digital tristateable output.
Special Output	The output signals of specific hardware modules are directly port output source.

See the chapter on Pinning for information about specific hardware module connections to individual port pins for Special Input and Special Output purposes.

H-Port control is distributed among five registers. All register bits corresponding to one H-Port pin are controlled by the same bus bit.

After reset, all H-Ports are in Normal, Output, Low, CMOS input level condition.

The function of the five registers is given in Table 12–5.

Table 12–5: Register Functions

Register	Function
HxD	r/w Data register
HxTRI	enable/disable output
HxNS	select Data register or specific hardware module as output source
HxLVL	select CMOS or Automotive Schmitt trigger input level
HxPIN	read pin state

The Special Input path is always operative. This allows manipulating the input signal to the specific hardware module through Normal Output operations by software.

Because register HxPIN allows reading the pin level also in Special Output mode, the output state of the specific hardware module may be read by the CPU.

Two high current ports together with a coil build a H-bridge. Two H-bridges are necessary to operate a stepper motor.

The n-channel and the p-channel transistor of the output driver are controlled separately, to eliminate crossover currents.

The reset output levels of the ports are low to avoid floating coils.

12.5. High Current Port Registers

Five H-Port registers are basically available for 8 H-Ports H0 to H7, each. But the respective device's pinning may require a reduction in available H-Ports. See the respective pinning table for details.

The general H-Port register model is given below.

HxD High Current Port x Data Register

	7	6	5	4	3	2	1	0	
r/w	x	x	x	x	D3	D2	D1	D0	
	x	x	x	x	0	0	0	0	Res

D0 to 3 Data Latch
w: Write latch.
r: Read latch.

HxTRI High Current Port x Tristate Register

	7	6	5	4	3	2	1	0	
r/w	x	x	x	x	T3	T2	T1	T0	
	x	x	x	x	0	0	0	0	Res

T0 to 3 Output Tristate Flag 0 to 3
r/w1: Output driver is disabled (tristate)
r/w0: Output driver is enabled

HxNS High Current Port x Normal/Special Register

	7	6	5	4	3	2	1	0	
r/w	x	x	x	x	S3	S2	S1	S0	
	x	x	x	x	0	0	0	0	Res

S0 to 3 Normal/Special Mode Flag 0 to 3
r/w1: Special Mode. Special hardware drives pin.
r/w0: Normal Mode. Data latch drives pin.

HxLVL High Current Port x Input Level Register

	7	6	5	4	3	2	1	0	
r/w	x	x	x	x	A3	A2	A1	A0	
	x	x	x	x	0	0	0	0	Res

A0 to 3 Automotive Flag 0 to 3
r/w1: Schmitt trigger input level is Automotive
r/w0: Schmitt trigger input level is CMOS

HxPIN High Current Port x Pin Register

	7	6	5	4	3	2	1	0	
r	x	x	x	x	P3	P2	P1	P0	
	x	x	x	x	0	0	0	0	Res

P0 to 3 Pin Data 0 to 3
r: Read Pin state.

13. AVDD Analog Section

The Analog Section operates from the AVDD supply pin and comprises the PLL/ERM module, the ADC, the P06 and the WAIT Comparators. In addition it contains support circuits like the VREFINT Generator, the BVDD Regulator and the necessary biasing circuits. Fig. 13–1 gives an overview.

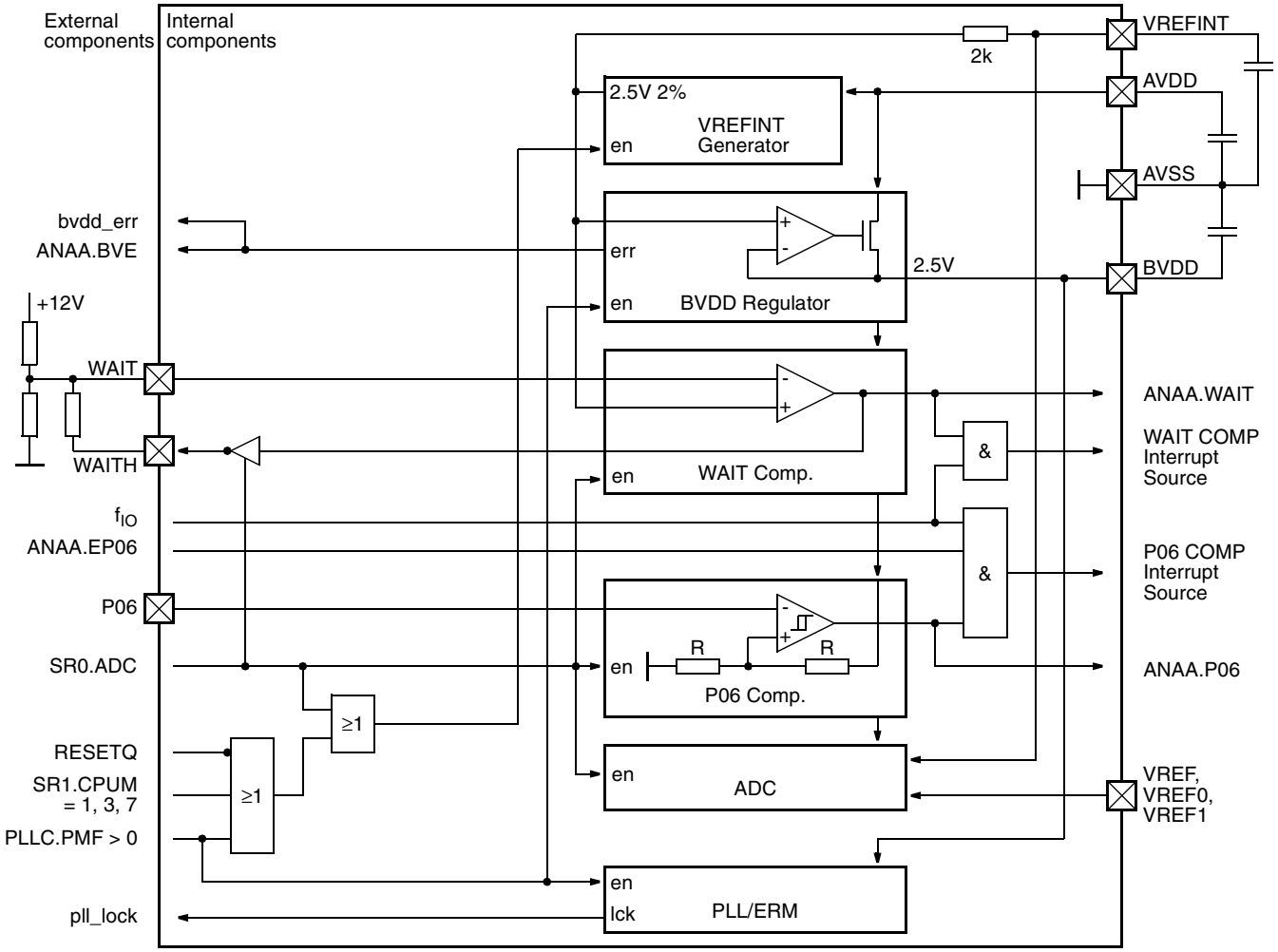


Fig. 13–1: AVDD Section

Table 13–1: Activation of AVDD Analog Section modules

CPU Mode	VREFINT Gen.	PLL/ERM and BVDD Regulator	ADC, P06, WAIT
RESET	on	off	off
FAST, PLL and PLL2 modes	on	on if PLLC.PMF > 0	on if SR0.ADC=1
SLOW and DEEP SLOW modes	on if PLLC.PMF > 0 or SR0.ADC=1		

13.1. VREFINT Generator

The VREFINT Generator generates bias signals which are necessary for the operation of all Analog-Section modules. Furthermore, it produces a tightly controlled reference voltage VREFINT, that is delivered to the BVDD Regulator and the WAIT Comparator. Via a decoupling resistor it also is routed to the VREFINT pin.

The VREFINT-pin voltage, which has to be buffered externally by a 10-nF ceramic capacitor, is input to the ADC as alternative, internally generated, reference voltage.

This module is permanently enabled during reset, in the CPU modes FAST, PLL and PLL2, and whenever SR0.ADC or PLLC.PMF is not 0. A certain set-up time has to elapse after enabling the module for VREFINT to stabilize.

No resistive load must be connected to the VREFINT pin.

13.2. BVDD Regulator

The BVDD Regulator generates the 2.5-V BVDD supply voltage for the internal PLL/ERM module from the 5-V AVDD. It derives its reference from the VREFINT Generator.

BVDD must be buffered externally by a 150-nF ceramic capacitor.

This module is permanently enabled whenever PLLC.PMF is not 0. A certain set-up time has to elapse after enable for BVDD to stabilize.

An overload condition in the regulator (current or voltage drop-out) is stored in flag ANAA.BVE. The immediate overload signal may be routed to the LCK special output by selection in field ANAU.LS (UVDD Analog Section).

13.3. Wait Comparator

The level on pin WAIT is compared to the internal reference VREFINT. The state of the comparator output is available as flag ANAA.WAIT and as WAIT Comparator interrupt source.

Furthermore, the output is available on pin WAITH, so that the hysteresis of this comparator can be set with an external positive-feedback resistor (100kOhms min.).

After reset, the module is off (zero standby current). The module is enabled by setting flag SR0.ADC, together with the P0.6 Comparator and the ADC. If the VREFINT Generator is powered up as well (cf. Table 13–1), the user has to assure that the necessary VREFINT set-up time has elapsed, before using comparator results (flag and interrupt).

The interrupt source output is routed to the Interrupt Controller logic. But this does not necessarily select it as input to the Interrupt Controller. Check section “Interrupt Controller” for the actually selectable sources and how to select them.

The WAIT Comparator interrupt source toggles with f_{IO}, to generate interrupts as long as the level on pin WAIT is lower than the internal reference.

13.4. P0.6 Comparator

The level on port P0.6 is compared to AVDD/2. The comparator features a small built-in hysteresis. The state of the comparator output is available as flag ANAA.P06 and as P0.6 Comparator interrupt source.

After reset, the module is off (zero standby current). The module is enabled by setting flag SR0.ADC, together with the WAIT Comparator and the ADC. If the VREFINT Generator is powered up as well (cf. Table 13–1), the user has to assure that the necessary VREFINT set-up time has elapsed, before using comparator results (flag and interrupt).

The interrupt source output, which must be enabled by setting flag ANAA.EP06, is routed to the Interrupt Controller logic. But this does not necessarily select it as input to the Interrupt Controller. Check section “Interrupt Controller” for the actually selectable sources and how to select them.

The P0.6 Comparator interrupt source toggles with f_{IO}, to generate interrupts as long as the level on pin P0.6 is lower than the internal reference.

13.5. PLL/ERM

The PLL and ERM modules are operated on the internally generated 2.5V BVDD supply voltage.

For details on operating this module please refer to section “CPU and Clock System”.

13.6. A/D Converter (ADC)

The Analog to Digital Converter allows the conversion of an analog voltage ranging from AVSS to either one of three external references VREF, VREF0, VREF1 (2.5 to 5V) or the internal reference VREFINT (~2.5V), to a 10-bit digital value. A multiplexer connects one of 16 analog input ports to the ADC. A sample and hold circuit holds the analog voltage during conversion. The duration of the sampling time is programmable.

Features

– 10-bit resolution.
– Successive approximation, charge balance type.
– 16 channel input multiplexer.
– Input buffering for high ohmic sources selectable.
– Sample and hold circuit.
– 4/8/16/32µs conversion selectable for optimum throughput/accuracy balance.
– 2.5V internal reference (VREFINT) or 2.5 to 5V external references (VREF, VREF0, VREF1) selectable
– Zero standby current

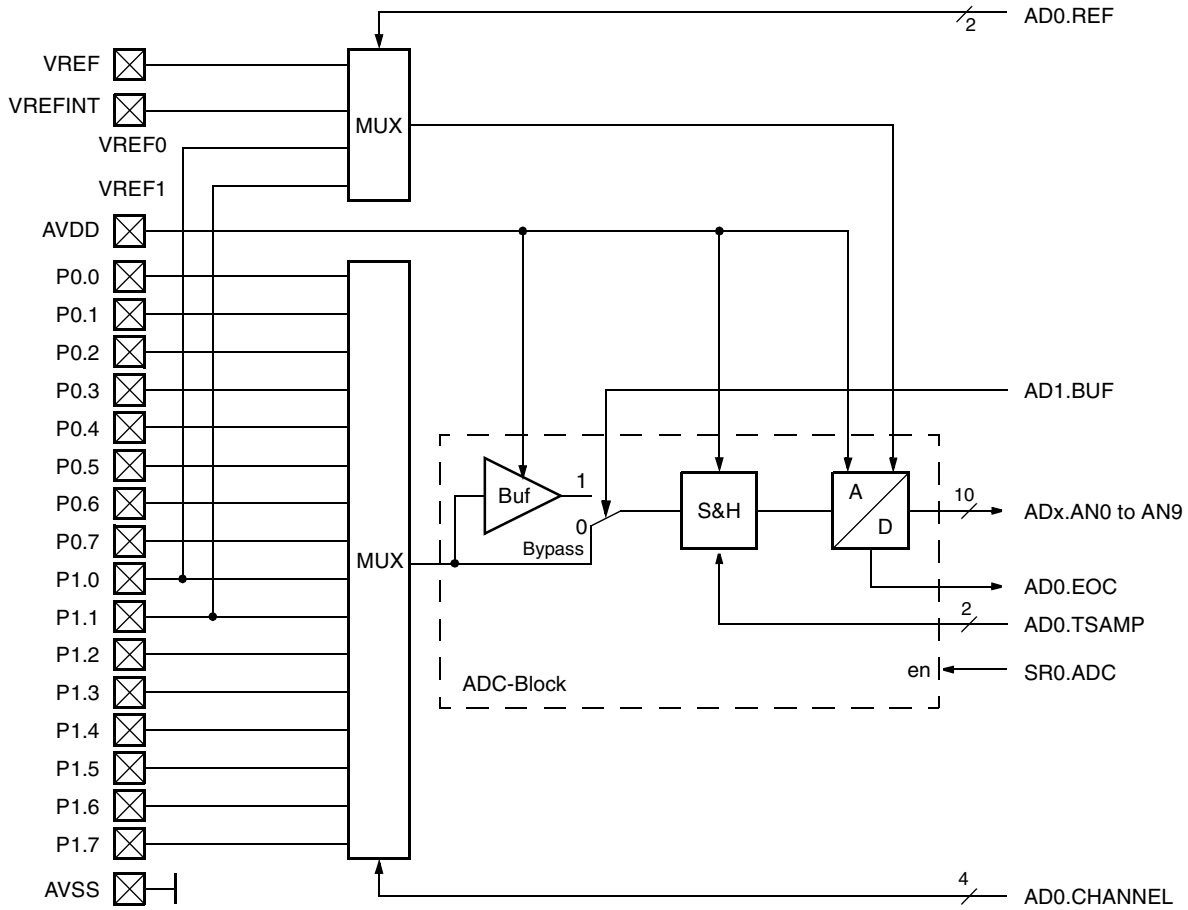


Fig. 13–2: ADC Block Diagram

13.6.1. Principle of Operation

After reset, the module is off (zero standby current). The module is enabled by setting flag SR0.ADC. The user has to assure that the necessary VREFINT-set-up time has elapsed.

Before starting a conversion, select input-buffer usage or bypass with flag AD1.BUF. Note that the input buffer requires

a 1us setup time before usage. When the buffer is never used, leave flag AD1.BUF cleared. When the buffer is always used, leave this flag set. When toggling buffer usage, set this flag at least 1us before starting a conversion.

Before starting a conversion, check flag AD0.EOC to be set.

A conversion is started by a write access to register AD0, selecting sample time (AD0.TSAM), reference source (AD0.REF) and input channel (AD0.CHANNEL).

Sampling starts one f_0 clock cycle after completion of the write access to AD0. Flag AD0.EOC signals the end of conversion. The 10-bit result is stored in the registers AD1 (8 MSB) and AD0.

The conversion time depends on f_0 and the programmed sample time (Table 13–2).

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

13.6.1.1. Conversion Law

The result of A/D conversion is described by the following formula:

$$DV = INT\left(\frac{U_{In}}{1LSB}\right) \quad \text{where} \quad 1LSB = \frac{U_{Ref}}{1024}$$

DV = Digital Value; INT = Integer part of the result

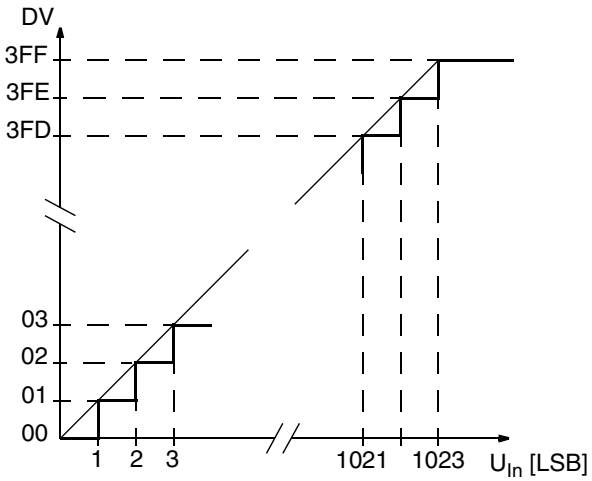


Fig. 13–3: Characteristic Curve

The voltage on the reference-input pins VREF, VREF0 and VREF1 may be set to any level in the range from AV_{SS} to AV_{DD}. However, accuracy is only specified in the range from 2.56V (1 LSB = 0.25mV) to 5.12V (1 LSB = 0.5mV).

13.6.1.2. Measurement Errors

The result of the conversion mirrors the voltage potential of the sampling capacitance (typically 8pF) at the end of the sampling time. This capacitance has to be charged by the source through the source impedance within the sampling-time period. To avoid measurement errors, system design has to make sure that at the end of this sampling period, the voltage on the sampling capacitance is within ±0.1 LSB from the source voltage.

Measurement errors may occur, when the voltage of high-impedance sources has to be measured:

– To reduce these errors, the sampling time may be increased by programming the field AD0.TSAMP.

– In cases where high-impedance sources are only rarely sampled, a 100nF capacitor from the input to AVSS is a sufficient measure to ensure that the voltage on the sampling capacitance reaches the full source voltage, even with the shortest sampling time.

– In some high-impedance applications a charge-pumping effect may noticeably influence the measurement result: Charge pumping from a high-potential to a low-potential source will occur when such two sources are measured alternatingly. This results in a current that appears as flowing from the high-potential source through the IC into the low-potential source. This current explains from the fact that during the respective sampling period the high-potential source always charges the sampling capacitance, while the low-potential source always discharges it. Usage of the input buffer (AD1.BUF) substantially reduces this effect.

13.7. Registers

AD0 ADC Register 0

	7	6	5	4	3	2	1	0	
r	EOC	x	x	x	x	TEST	AN1	AN0	
w	TSAMP		REF		CHANNEL				
	0	0	0	0	0	0	0	0	Res

AD1 ADC Register 1

	7	6	5	4	3	2	1	0	
r	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	
w	x	x	x	x	x	x	x	BUF	
								0	Res

EOC End of Conversion
r1: End of conversion
r0: Busy
EOC is reset by a write access to the register AD0. EOC must be true before starting the first conversion after enabling the module by setting SR0.ADC.

TSAMP Sampling Time
TSAMP adjusts the sample conversion times.

Table 13–2: TSAMP Usage: Sample and Conversion Time

TSAMP	t_{Sample}	$t_{Conversion}$
0H	$20/f_0$	$40/f_0$
1H	$60/f_0$	$80/f_0$
2H	$140/f_0$	$160/f_0$
3H	$300/f_0$	$320/f_0$

REF Conversion Reference
w0: External reference from VREF pin used
w1: Internal reference on VREFINT pin used
w2: External reference from VREF0 pin used
w3: External reference from VREF1 pin used

CHANNEL Channel of Input Multiplexer
CHANNEL selects from which pin of port P0 or P1 the conversion is done. The MSB of CHANNEL is bit 3.

Table 13–3: CHANNEL Usage: ADC Input Selection

CHANNEL	Port Pin
0 to 7	P0.0 to P0.7
8 to 15	P1.0 to P1.7

AN 9 to 0 Analog Value Bit 9 to 0
The 10-bit data format is positive integer, i.e. 000H for lowest and 3FFH for highest possible input signal. The 8 MSB can be read from register AD1. The two LSB can be read from register AD0. The result is available until a new conversion is started.

BUF Input Buffer Usage
w1: Buffer used
w0: Buffer bypassed

TEST for factory use only

ANAA Analog AVDD Register

	7	6	5	4	3	2	1	0	
r/w	EP06	P06	WAIT	x	x	x	x	BVE	
	0							0	Res

EP06 Enable P06 Comparator Interrupt Source output
r/w1: Enabled.
r/w0: Disabled.

P06 P06 Comparator Output
r1: P0.6 is lower than AVDD/2.
r0: P0.6 is higher than AVDD/2.

WAIT WAIT Comparator Output
r1: WAIT is lower than VREFINT.
r0: WAIT is higher than VREFINT.

BVE BVDD Regulator Error Flag
r1: Out of specification.
r0: Normal operation.
w1: Reset flag.
w0: No action.

14. Timers (TIMER)

Five general purpose timers are implemented. T0 is a 16 bit timer, T1 to T4 are 8 bit timers.

14.1. Timer T0

Timer T0 is a 16bit auto reload down counter. It serves to deliver a timing reference signal to the ICU, to output a frequency signal or to produce time stamps.

Features

- 16bit auto reload counter
- Time value readable
- Interrupt source output
- Frequency output

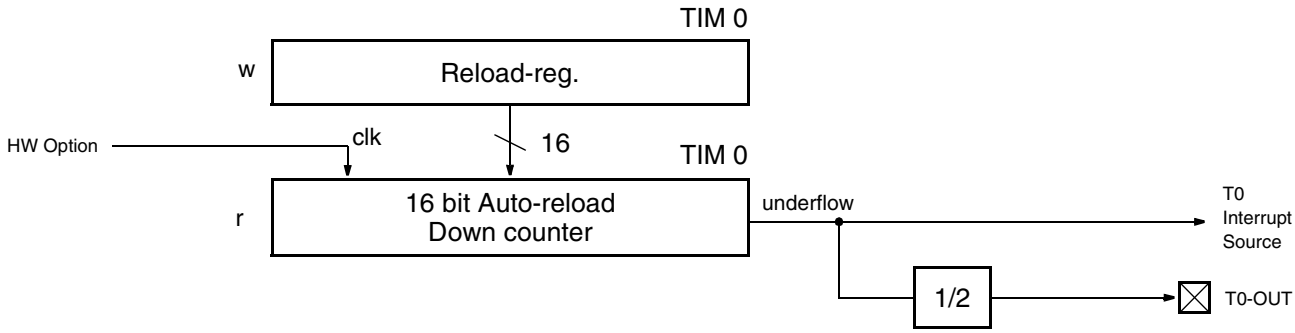


Fig. 14–1: Timer T0 Block Diagram

14.1.1. Principle of Operation

14.1.1.1. General

The timer's 16bit down-counter is clocked by the input clock and counts down to zero. One clock count after reaching zero, it generates an output pulse, reloads with the content of the TIM0 reload register and restarts its travel.

For the effect of CPU clock modes on the operation of this module refer to section "CPU and Clock System" (see Table 4–1 on page 36).

14.1.1.2. Operation

The clock input frequency is settable by HW option (see Table 14–1 on page 92).

Prior to entering active mode, proper SW initialization of the U-Ports assigned to function as T0-OUT outputs has to be made (Table 14–1). The ports have to be configured Special Out. Refer to "Ports" for details.

T0 is always active (no standby mode). After reset the timer starts counting with reload value 0xFFFF generating a maximum period output signal.

A new time value is loaded by writing to the 16bit register TIM0, high byte first. Upon writing the low byte, the reload register is set to the new 16bit value, the counter is reset, and immediately starts down-counting with the new value.

On reaching zero, the counter generates a reload signal, which can be used to trigger an interrupt. The same signal is connected to a divide by two scaler to generate the output signal T0-OUT with a pulse duty factor of 50%.

The interrupt source output of this module is routed to the Interrupt Controller logic. But this does not necessarily select it as input to the Interrupt Controller. Check section "Interrupt Controller" for the actually selectable sources and how to select them.

The state of the down-counter is readable by reading the 16bit register TIM0, low byte first. Upon reading the low byte, the high byte is saved to a temporary latch, which is then accessed during the subsequent high byte read. Thus, for time stamp applications, read consistency between low and high byte is guaranteed.

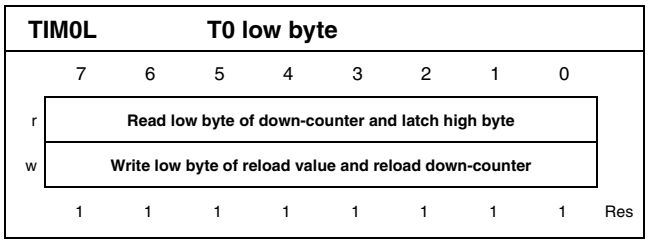
14.1.1.3. Precautions

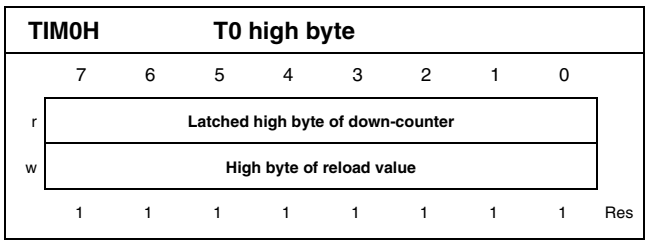
Use 8bit load/store operations to access Timer 0 register rather than 16bit access.

Table 14–1: Module specific settings

Module Name	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
T0	Input clock	T0C	T0-OUT output	U1.2 special out	

14.1.2. Registers





TIM0 has to be read low byte first and written high byte first.

Table 14–2: Reload Register Programming

Reload value	Output interrupt source frequency is divided by	Output T0-OUT is divided by
0x0000	1	2
0x0001	2	4
0x0002	3	6
:	:	:
0xFFFF	65536	131072

14.2. Timer T1 to T4

Timer T1 to T4 are 8bit auto reload down counters. They serve to deliver timing reference signals to the ICU or to output frequency signals.

Table 14–3 describes implementation specific HW Option addresses and enable flags of T1 to T4.

Features

- 8bit auto reload counter
- Interrupt source output
- Frequency output

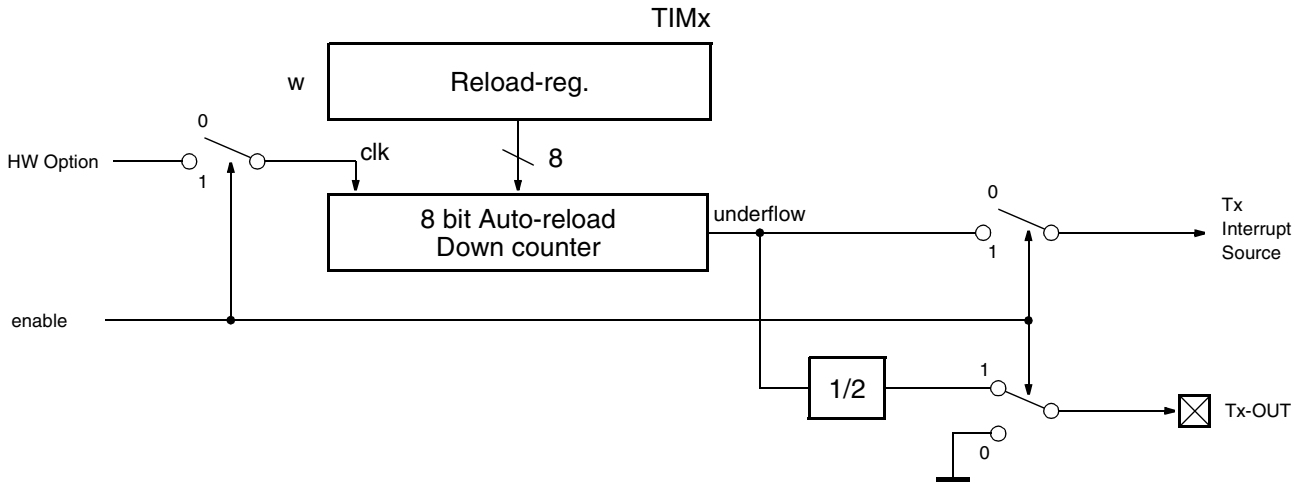


Fig. 14–2: Timer T1 to T4 Block Diagram

14.2.1. Principle of Operation

14.2.1.1. General

The timer's 8bit down-counter is clocked by the input clock and counts down to zero. One clock count after reaching zero, it generates an output pulse, reloads with the content of the TIMx reload register and restarts its travel.

For the effect of CPU clock modes on the operation of this module refer to section "CPU and Clock System" (see Table 4–1 on page 36).

14.2.1.2. Operation

The clock input frequencies are settable by HW options (see Table 14–3 on page 94). After reset, the 8bit timer is in standby (inactive).

Prior to entering active mode, proper SW initialization of the U-Ports assigned to function as Tx-OUT outputs has to be made (Table 14–3). The ports have to be configured Special Out. Refer to "Ports" for details.

To initialize a timer, reload register TIMx has to be set to the desired time value, still in standby mode.

For entering active mode, set the corresponding enable bit in the standby registers (see Table 14–3 on page 94). The timer will immediately start counting down from the time value present in register TIMx.

During active mode, a new time value is loaded by simply writing to register TIMx. Upon writing, the counter is reset, and immediately starts counting down from the new time value.

On reaching zero, the counter generates a reload signal, which can be used to trigger an interrupt. The same signal is connected to a divide by two scaler to generate the output signal Tx-OUT with a pulse duty factor of 50%.

The interrupt source output of this module may be but must not be connected to the interrupt controller. Please refer to section Interrupt Controller.

Returning Tx to standby mode by resetting its respective enable bit will halt its counter and will set its outputs LOW. The register TIMx remains unchanged.

The state of the down-counter is not readable.

Table 14–3: Module specific settings

Module Name	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
T1	Input clock	T1C	T1-OUT output	U1.1 special out	SR0.TIM1
T2	Input clock	T2C	T2-OUT output	U1.0 special out	SR0.TIM2
T3	Input clock	T3C	T3-OUT output	U0.7 special out	SR0.TIM3
T4	Input clock	T4C	T4-OUT output	U0.6 special out, PM.U06 = 0	SR0.TIM4

14.2.2. Registers

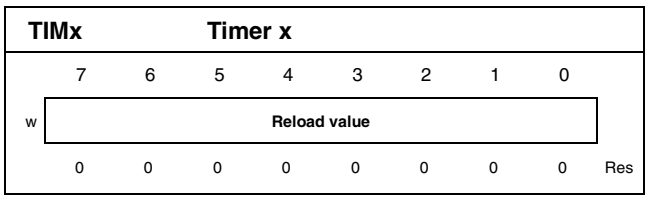


Table 14–4: Reload Register Programming

Reload value	Output interrupt source frequency is divided by	Output Tn-OUT is divided by
0x00	1	2
0x01	2	4
0x02	3	6
:	:	:
0xFF	256	512

15. Pulse Width Modulator (PWM)

A PWM is an auto reload down-counter with fixed reload interval. It serves to generate a frequency signal with variable pulse width or, with an external low pass filter, as a digital to analog converter.

This module is combined of two independently operatable 8bit PWMs which can be combined to a single 16bit PWM.

The number of PWMs implemented is given in table 15–1. The “x” in register names distinguishes the module number and can be 1, 3, 5, 7, 9, 11.

Features

– Two 8bit or one 16bit pulse width modulator

– Wide range of HW option selectable cycle frequencies

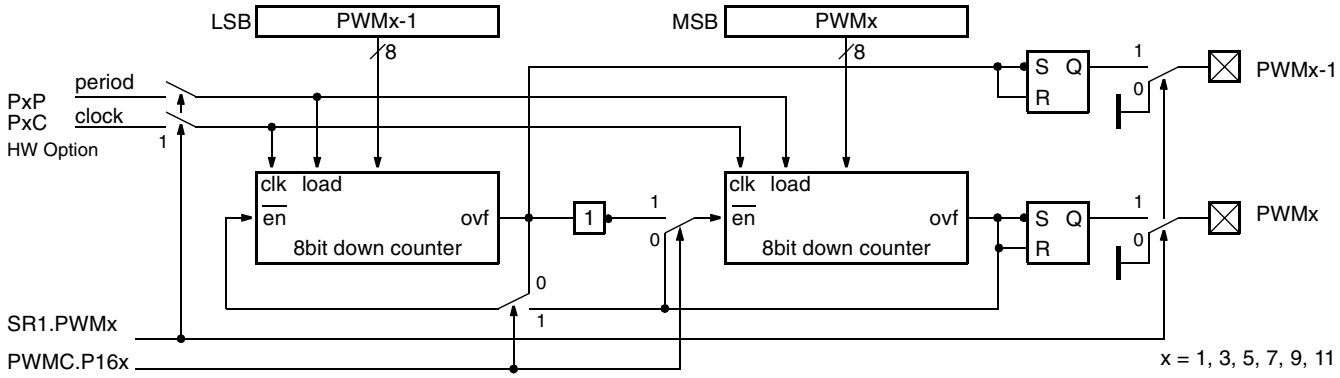


Fig. 15–1: PWM Block Diagram

15.1. Principle of Operation

15.1.1. General

A PWM’s down-counter is clocked by its input clock and counts down to zero. Reaching zero, it stops and sets the output to LOW. A period input pulse reloads the counter with the content of the PWM register, restarts it and sets the output to HIGH.

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

15.1.2. Hardware settings

The clock and period input frequencies are settable by HW option (Table 15–1). There is one common source for both 8bit PWMs, one for clock and one for period, thus clock and period are not independently selectable for the two 8bit PWMs. For full resolution a clock to period frequency ratio of 256 (65536 in 16bit mode) is recommended. Should other ratios be used, make sure that the combination of clock, period and pulse width setting allow the PWM to generate an output signal with a LOW transition.

Some of the PWM outputs share pins with outputs of other modules. The output multiplexer is controlled by HW option (Table 15–1).

15.1.3. Initialization

Prior to entering active mode, proper SW initialization of the H-Ports and U-Ports assigned to function as PWMx outputs has to be made (Table 15–1). The ports have to be configured Special Out. Refer to “Ports” for details.

It has to be decided which PWM module shall work as one 16bit or as two 8bit PWMs. Selection has to be done via the PWM control register PWMC as long as the PWM module is disabled.

15.1.4. Operation

After reset, a PWM is in standby mode (inactive) and the output signal PWMx is LOW.

For entering active mode, select the desired mode (8-/16bit mode) and then set the respective enable bit (Table 15–1). Then write the desired pulse width value to register PWMx (write low byte first in 16bit mode). Each PWM will start producing its output signal immediately after the next subsequent input pulse on its period input.

During active mode, a new pulse width value is set by simply writing to the register PWMx. Upon the next subsequent input pulse on its period input the PWM will start producing an output signal with the new pulse width value, starting with a HIGH level.

Table 15–1: Module specific settings

Module Name	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
PWM1	Clock and period	P1C, P1P	PWM0	U0.3 special out	SR1.PWM1
	H0.3 SMG/PWM1 output multiplexer	PM.H0	PWM1	U0.2 and/or H0.3 special out	
PWM3	Clock and period	P3C, P3P	PWM2	U0.1special out	SR1.PWM3
	H0.2 SMG/PWM3 output multiplexer	PM.H0	PWM3	U0.0 and/or H0.2 special out	
PWM5	Clock and period	P5C, P5P			SR1.PWM5
	H7.3 SME/PWM4 output multiplexer	PM.H7	PWM4	H7.3 special out	
	H0.1 SMG/PWM5 output multiplexer	PM.H0	PWM5	H0.1 special out	
PWM7	Clock and period	P7C, P7P			SR1.PWM7
	H7.2 SME/PWM6 output multiplexer	PM.H7	PWM6	H7.2 special out	
	H0.0 SMG/PWM7 output multiplexer	PM.H0	PWM7	H0.0 special out	
PWM9	Clock and period	P9C, P9P			SR1.PWM9
	H7.1 SME/PWM8 output multiplexer	PM.H7	PWM8	H7.1 and/or H6.3 special out	
	H7.0 SME/PWM9 output multiplexer	PM.H7	PWM9	H7.0 and/or H6.2 special out	
PWM11	Clock and period	P11C, P11P	PWM10	H6.1 special out	SR1.PWM11
			PWM11	H6.0 special out	

Returning a PWM to standby mode by resetting its respective enable flag will immediately set its output LOW.

The 8bit PWM output PWMx-1 is not usable in 16bit mode.

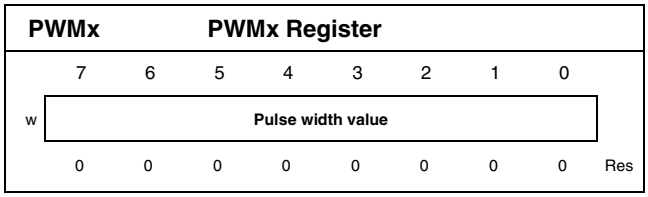
The state of the down-counters and the PWM registers is not readable.

Due to EMI reduction the start of a period is delayed for different PWMs (Table 15–2).

Table 15–2: Module Delay

Module Number	Delay
PWM 0, 4, 8	0
PWM 1, 5, 9	$1/f_0$
PWM 2, 6, 10	$2/f_0$
PWM 3, 7, 11	$3/f_0$

15.2. Registers



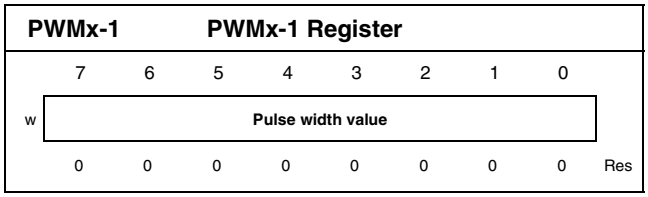


Table 15–3: 8bit Mode Pulse Width Programming

Pulse width value	Pulse duty factor
0x00	0% (Output is permanently low)
0x01	1/256
0x02	2/256
:	:
0xFE	254/256
0xFF	100% (Output is permanently high) [1])
[1]) Pulse duty factor 255/256 is not selectable.	

Table 15–4: 16bit Mode Pulse Width Programming

Pulse width value	Pulse duty factor
0x0000	0% (Output is permanently low)
0x0001	1/65536
0x0002	2/65536
:	:
0xFFFE	65534/65536
0xFFFF	100% (Output is permanently high) [1])
[1]) Pulse duty factor 65535/65536 is not selectable.	

PWMC PWM Control Register

	7	6	5	4	3	2	1	0	
w	x	x	P1611	P169	P167	P165	P163	P161	
	x	x	0	0	0	0	0	0	Res

P16x PWM 16 Mode of Module x
w1: 16bit mode.
w0: 8bit mode.

16. Pulse Frequency Modulator (PFM)

The PFM generates a signal with variable frequency and variable pulse width. Together with external elements it may serve to generate a negative voltage for LCD elements.

Features

- Pulse width and period separately controllable
- Pulse width and period counters operate with HW option selectable clock
- Output polarity selectable
- Standby mode

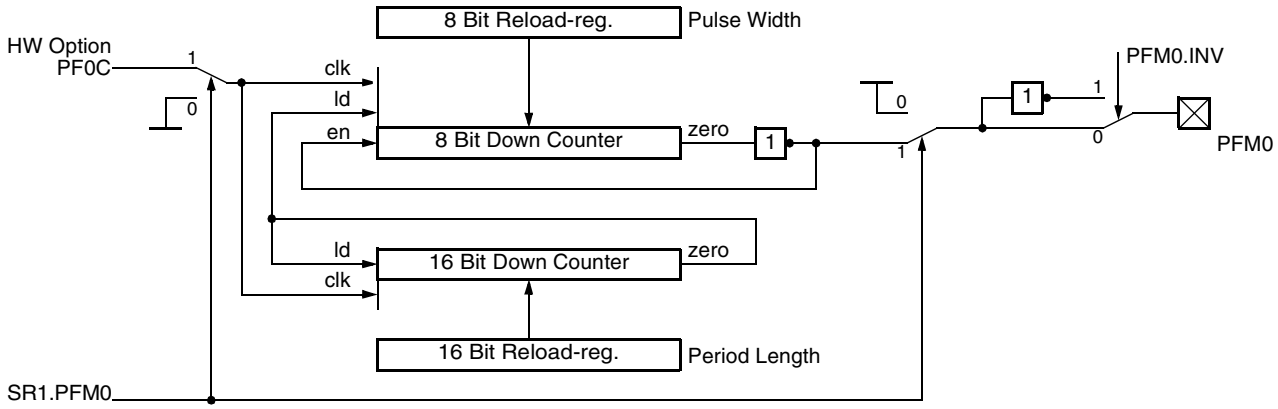


Fig. 16–1: PFM Block Diagram

16.1. Principle of Operation

16.1.1. General

The pulse width and the period counter start synchronously with down-counting. As long as the pulse width counter is running, it's zero output is LOW. When this counter reaches zero it stops counting and sets the zero output to HIGH. When the period counter reaches zero, it reloads both counters, which starts a new count cycle. The zero output of the pulse width counter can be driven out directly or inverted via pin PFM0.

The module is operable in PLL, FAST and SLOW mode. As long as PF0C is available it is also operable in DEEP SLOW mode. See also chapter "CPU and Clock System" for further details.

16.1.2. Hardware Settings

The clock input frequency PF0C is settable by HW option (see Table 16–1).

Table 16–1: Module specific settings

HW Options		Initialization		Enable Bit
Item	**Address**	**Item**	**Setting**	
Input clock	PF0C	PFM0	U5.0 and/or U1.7 special out	SR1.PFM0

16.1.3. Initialization

Prior to entering active mode, proper SW initialization of the U-Ports assigned to function as PFM0 output has to be made (Table 16–1). The ports have to be configured Special Out. Refer to "Ports" for details.

16.1.4. Operation

After reset the PFM is in standby mode (inactive) and the output signal is LOW.

To prepare for active mode, write new values, if needed, for the pulse width and the period length to the respective PFM0 register and select output inversion, if necessary, with flag INV. For entering active mode set the enable bit SR1.PFM0.

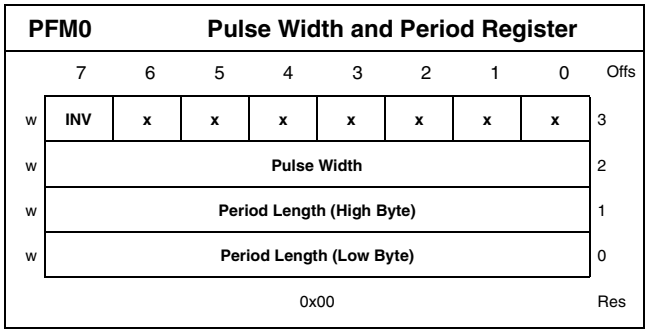
Changing the PFM0 register setting during active mode, is simply done by writing a 32bit word to this register. After the register has been updated, the PFM will produce an output signal with the new pulse width and period length starting with the next subsequent load signal of the period counter.

For data consistency, when using 8bit and 16bit writes, new values will only become valid after a write to the pulse width register (byte 2 in the PFM0 register).

Returning the PFM to standby mode by clearing its Enable Bit SR1.PFM0 will immediately set its output to INV and disable the clock input. The content of the PFM0 register is not affected by standby mode.

The state of the counters and the reload registers is not readable.

16.2. Registers



INV **Invert Output Signal**
r/w1: inverted
r/w0: direct

The pulse width counter zero output HIGH time is calculated by

$$t_{HIGH} = \frac{\text{Pulse Width}}{\text{F}_{\text{PF0C}}}$$

and the duration of the period time by

$$t_{Period} = \frac{\text{Period Length}}{\text{F}_{\text{PF0C}}}$$

Therefore, the pulse width counter zero output LOW time is

$$t_{LOW} = t_{Period} - t_{HIGH}$$

Table 16–2 shows the relation of the Pulse Width and the Period Length and its effect on the PFM0 output.

Table 16–2: Pulse Width to Period Length Relation

Pulse Width	Period Length	INV	PFM0 output
0	x	0	Always low
> 0	≤ Pulse Width		Always high
> 0	> Pulse Width		High pulses
0	x	1	Always high
> 0	≤ Pulse Width		Always low
> 0	> Pulse Width		Low pulses

17. Capture Compare Module (CAPCOM)

The IC contains two Capture Compare Modules (CAPCOM).

A CAPCOM is a complex relative timer. It comprises a free running 16bit Capture Compare Counter (CCC) and a number of Subunits (SU). The timer value can be read by SW.

A SU is able to capture the relative time of an external event input and to generate an output signal when the CCC passes a predefined timer value. Three types of interrupts enable interaction with SW. Special functionality provides an interface to the asynchronous external world.

- 16bit free running counter with read out.
- 16bit capture register.
- 16bit compare register.
- Input trigger on rising, falling or both edges.
- Output action: toggle, low or high level.
- Three different interrupt sources: overflow, input, compare
- Designed for interface to asynchronous external events

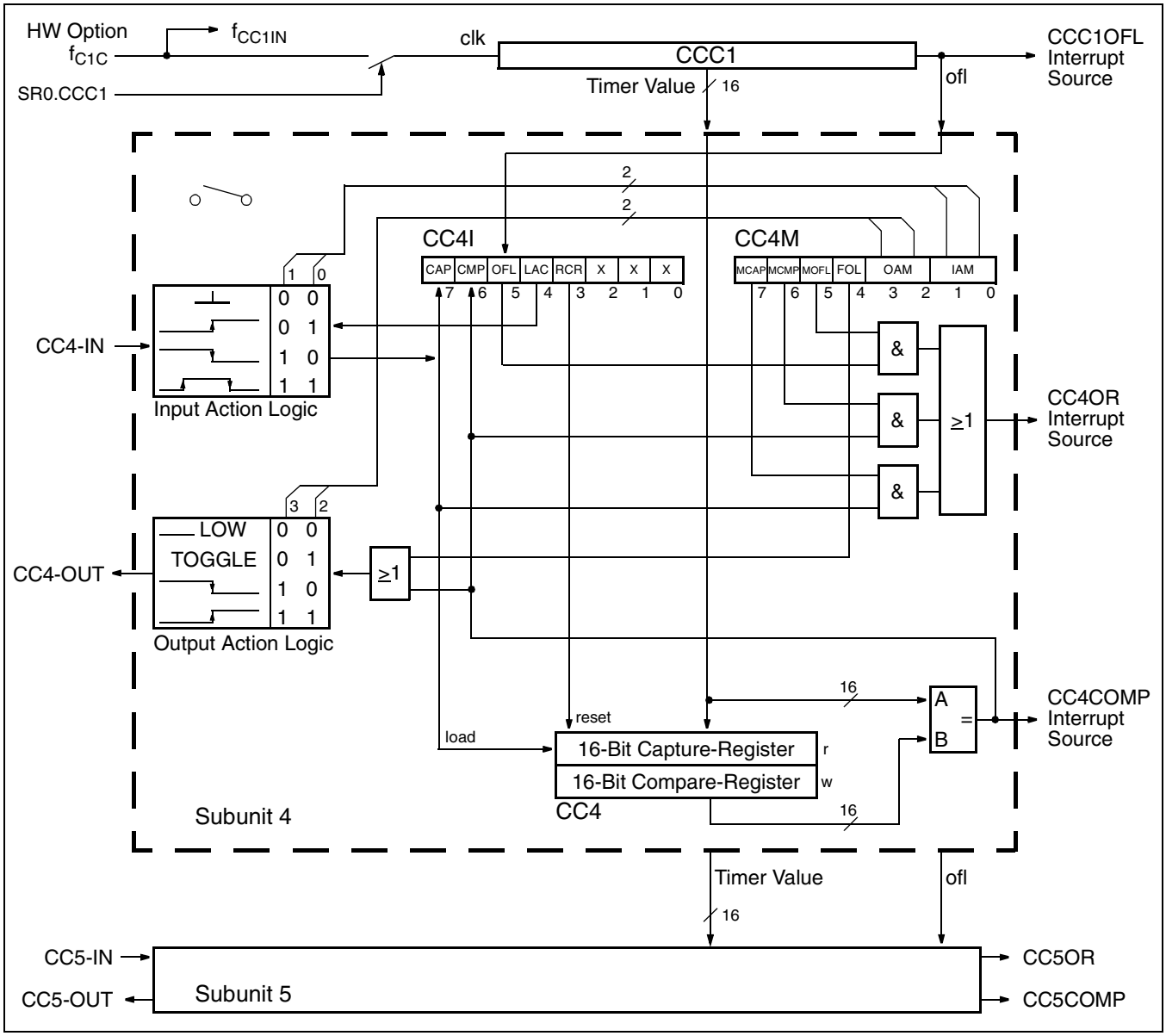


Fig. 17–1: CAPCOM Module 1 Block Diagram

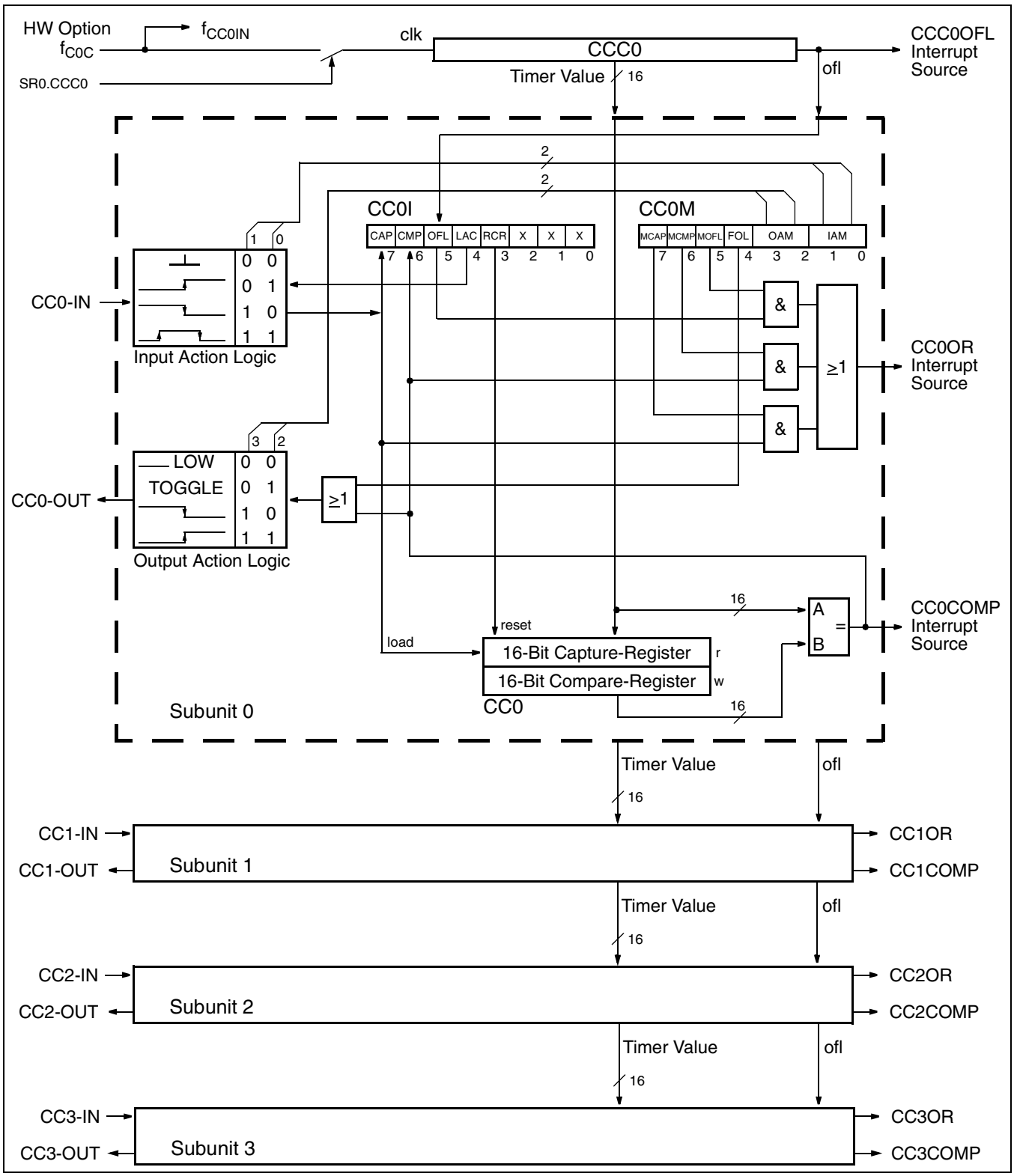


Fig. 17–2: CAPCOM Module 0 Block Diagram

17.1. Principle of Operation

17.1.1. General

The Capture Compare Module (CAPCOM, Fig. 17–1, 17–2) contains one common free running 16bit counter (CCC) and a number of capture and compare subunits (SU). More details are given in Tables 17–1 and 17–2. The timer value can be read by SW from 16bit register CCC. The CCC provides an interrupt on overflow.

Each SU is able to capture the CCC value at a point of time given by an external input event processed by an Input Action Logic.

A SU can also change an output line level via an Output Action Logic at a point of time given by the CCC value.

Thus, a SU contains a 16bit capture register CCx to store the input event CCC value, a 16bit compare register CCx to program the Output Action CCC value, an 8bit interrupt register CCxI and an 8bit mode register CCxM. Two types of interrupts per SU enable interaction with SW.

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

17.1.2. Hardware Settings

The CCC0 and CCC1 clock frequency must be set via HW option (Table 17–1 and 17–2). Some SUs use several ports. They can be selected via HW Option Port Multiplexer (PM). Refer to “HW Options” for setting them.

17.1.3. Initialization

After system reset the CCC and all SUs are in standby mode (inactive).

In standby mode, the CCC is reset to value 0x0000. Capture and compare registers CCx are reset. No information processing will take place, e.g. update of interrupt flags. However, the values of registers CCxI and CCxM are only reset by system reset, not by standby mode. Thus it is possible to program all mode bits in standby mode and a predetermined start-up out of standby mode is guaranteed.

Prior to entering active mode, proper SW configuration of the U-Ports assigned to function as Input Capture inputs and Output Action outputs has to be made (Table 17–1, 17–2). The Output Action ports have to be configured as special out and the Input Capture ports as special in. Refer to “Ports” for details.

17.1.3.1. Subunit

For a proper setup the SW has to program the following SU control bits in registers CCxI and CCxM: Interrupt Mask (MSK), Force Output Logic (FOL, 0 recommended), Output Action Mode (OAM), Input Action Mode (IAM), Reset Capture Register (RCR, 0 recommended), and Lock After Capture (LAC). Refer to section 17.2. for details.

Please note that the compare register CCx is reset in standby mode. It can only be programmed in active mode.

Table 17–1: Unit 0 specific settings

Subunit	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
SU0			CC0-OUT	U3.2, U4.0 special out	SR0. CCC0
	Input	PM. CACO	CC0-IN	U3.2, U4.1 special in	
SU1			CC1-OUT	U3.1, U2.5 special out	
	Input	PM. CACO	CC1-IN	U3.1, U2.4 special in	
SU2			CC2-OUT	U3.0, U2.3 special out	
	Input	PM. CACO	CC2-IN	U3.0, U2.2 special in	
SU3	Output	PM. U06	CC3-OUT	U0.5, U0.6, U8.1 special out	
			CC3-IN	U0.6 special in	
SU0, SU1, SU2, SU3	Clock	C0C			

Table 17–2: Unit 1 specific settings

Subunit	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
SU4			CC4-OUT	U5.3, U8.0 special out	SR0. CCC1
	Input	PM. CC4I	CC4-IN	U5.3, P0.0 special in	
SU5			CC5-OUT	U7.4 special out	
			CC5-IN	U7.4 special in	
SU4, SU5	Clock	C1C			

17.1.4. Operation of CCC

For entering active mode of the entire CAPCOM module set the enable bit (Table 17–1 and 17–2).

The CCC will immediately start up-counting with the selected clock frequency and will deliver this 16bit value to the SUs.

The state of the counter is readable by reading the 16bit register CCC, low byte first. Upon reading the low byte, the high byte is saved to a temporary latch, which is then accessed during the subsequent high byte read. Thus, for time stamp applications, read consistency between low and high byte is guaranteed.

The CCC is free running and will overflow from time to time. This will cause generation of an overflow interrupt event. The interrupt (CCCxOFL) is directly fed to the Interrupt Controller and also to all SUs where further processing takes place.

17.1.5. Operation of Subunit

17.1.5.1. Compare and Output Action

To activate a SUs compare logic the respective 16bit compare register CCx has to be programmed, low byte first. The compare action will be locked until the high byte write is completed. As soon as CCx setting and CCC value match, the following actions are triggered:

– The flag CMP in the CCxI register is set.

– The CCxCOMP interrupt source is triggered.

– The CCxOR interrupt source is triggered if activated.

– The Output Action logic is triggered.
Four different reactions are selectable for the Output Action signal: according to field CCxM.OAM (Table 17–3) the equal state will lead to a high or low level, toggling or inactivity on this output.
Another way to control the Output Action is bit CCxM.FOL. E.g. rise-mode and force will set the output pin to high level, fall-mode and force to low level. This forcing is static, i.e. it will be permanently active and may override compare events. Thus it is recommended to set and reset shortly after that, i.e. to pulse the bit with SW. Toggle mode of the Output Action logic and forcing leads to a burst with clock-frequency and is not recommended.

17.1.5.2. Capture and Input Action

The Input Action logic operates independently of the Output Action logic and is triggered by an external input in a way defined by field CCxM.IAM. Following Table 17–4 it can completely ignore events, trigger on rising or falling edge or on both edges. When triggered, the following actions take place:

– Flag CCxI.CAP is set.

– The CCxOR interrupt source is triggered if activated.

– The 16bit capture register CCx stores the current CCC value, i.e. the “time” of the external event. Read CCx low byte first. Further capture and input action will be locked until the subsequent high byte read is completed. Thus a coherent result is ensured, no matter how much time has elapsed between the two reads.

Some applications suffer from fast input bursts and a lot of capture events and interrupts in consequence. If the SW cannot handle such a rate of interrupts, this could evoke stack overflow and system crash. To prevent such fatal situations the Lock After Capture (LAC) mode is implemented. If bit CCxI.LAC is set, only one capture event will pass. After this event has triggered a capture, the Input Action logic will lock until it is unlocked again by writing an arbitrary value to register CCxM. Make sure that this write only restores the desired setting of this register.

Programming the Input Action logic while an input transition occurs may result in an unexpected triggering. This may overwrite the capture register, lock the Input Action logic if in LAC mode and generate an interrupt. Make sure that SW is prepared to handle such a situation.

For testing purposes, a permanent reset (0xFFFF) may be forced on capture register CCx by setting bit CCxI.RCR. Make sure that the reset is only temporary.

17.1.5.3. Interrupts

Each SU supplies two internal interrupt events:

1. Input Capture event and

2. Comparator equal state.

In addition to the above mentioned two, the CCC Overflow interrupt event sets flag CCxI.OFL in each SU. Thus, three interrupt events are available in each SU. As previously explained, interrupt events will set the corresponding flags in register CCxI. The corresponding flags are masked with their mask bits in register CCxM and passed to a logical or. The result (CCxOR) is fed to the interrupt controller as a first interrupt source. In addition, the Comparator equal (CCxCOMP) interrupt is directly passed to the interrupt controller as second interrupt source. Thus a SU offers four types of interrupts: CCC overflow (maskable ored), input capture event (maskable ored) and comparator equal state (maskable ored and non-maskable direct).

All interrupt sources act independently, parallel interrupts are possible. The interrupt flags enable SW to determine the interrupt source and to take the appropriate action. Before returning from the interrupt routine the corresponding interrupt flag should thus be cleared by writing a 1 to the corresponding bit location in register CCxI.

The interrupts generated by internal logic (CCC Overflow and Comparator equal) will trigger in a predetermined and known way. But as explained in 17.1.5.2. erroneous input signals may cause some difficulties concerning the Input Capture input as well as interrupt handling. To overcome possible problems the Input Capture Interrupt flag CCxI.CAP is double buffered. If a second or even more input capture interrupt events occur before the interrupt flag is cleared (i.e. SW was not able to keep track), the flag goes to a third state. Two consecutive writes to this bit in register CCxI are then necessary to clear the flag. This enables SW to detect such a multiple interrupt situation and eventually to discard the capture register value, which always relates to the latest input capture event and interrupt.

The internal CAPCOM module control logic always runs on the clock divider chain f_0 frequency, regardless of CPU clock mode. Avoid write accesses to the CCxI register in CPU Slow mode since the logic would interpret one CPU access as many consecutive accesses. This may yield to unexpected results concerning the functionality of the interrupt flags. The following procedure should be followed to handle the capture interrupt flag CAP:

1. SW responds to a CAPCOM interrupt, switching to CPU Fast or PLL mode if necessary and determining that the source is a capture interrupt (CAP flag =1).

2. The interrupt service routine is processed.

3. Just before returning to main program, the service routine acknowledges the interrupt by writing a 1 to flag CAP.

4. The service routine reads CAP again. If it is reset, the routine can return to main program as usual. If it is still set an external capture event overrun has happened. Appropriate actions may be taken (i.e. discarding the capture register value etc.).

5. go to 3.

17.1.6. Inactivation

The CAPCOM module is inactivated and returned to standby mode (power down mode) by setting the enable bit to 0. Section 17.1.3. applies.

CCxI and CCxM are only reset by system reset, not by standby mode.

17.1.7. Precautions

The CCxI register must not be written in CPU Slow mode (see Section 17.1.5.3. on page 104). Read-Modify-Write operations on single flags of register CCxI must be avoided. Unwanted clearing of other flags of this register may be the result otherwise.

17.2. Registers

The CAPCOM counter and the Capture/Compare registers have to be read/written low byte first to avoid inconsistencies. The memory controller accesses multiple byte quantities low byte first. Thus the 16 bit CAPCOM counter and the 16 bit Capture/Compare registers can be accessed 16 bit wide.

CCCyL CAPCOM Counter low byte

	7	6	5	4	3	2	1	0	
r	Read low byte and lock CCC								
	0	0	0	0	0	0	0	0	Res

CCCyH CAPCOM Counter high byte

	7	6	5	4	3	2	1	0	
r	Read high byte and unlock CCC								
	0	0	0	0	0	0	0	0	Res

CCxM CAPCOM x Mode Register

	7	6	5	4	3	2	1	0	
r/w	MCAP	MCMP	MOFL	FOL	OAM		IAM		
	0	0	0	0	0	0	0	0	Res

MCAP Mask CAP Flag
r/w1: Enable.
r/w0: Disable.

MCMP Mask CMP Flag
r/w1: Enable.
r/w0: Disable.

MOVL Mask OVL Flag
r/w1: Enable.
r/w0: Disable.

FOL Force Output Action Logic
r/w1: Force Output Action logic.
r/w0: Release Output Action logic.
This flag is static. As long as FOL is true neither comparator can trigger nor SW can force, by writing another “one”, the Output Action logic. After forcing it is recommended to clear FOL unless Output Action logic should not be locked.

OAM Output Action Mode
r/w: Defines behavior of Output Action logic.

Table 17–3: OAM usage

Bit 3 2	Output Action Logic Modes
0 0	Disabled, ignore trigger, output low level.
0 1	Toggle output.
1 0	Output low level.
1 1	Output high level.

IAM Input Action Mode
r/w: Defines behavior of Input Action logic.

Table 17–4: IAM usage

Bit 1 0	Input Action Logic Modes
0 0	Disabled, don’t trigger.
0 1	Trigger on rising edge.
1 0	Trigger on falling edge.
1 1	Trigger on rising and falling edge.

CCxI CAPCOM x Interrupt Register

	7	6	5	4	3	2	1	0	
r/w	CAP	CMP	OFL	LAC	RCR	x	x	x	
	0	0	0	0	0	0	0	0	Res

CAP Capture Event
r1: Event.
r0: No Event.
w1: Clear flag.
w0: No change.

CMP Compare Event
r1: Event.
r0: No Event.

w1: Clear flag.
w0: No change.

OFL **Overflow Event**
r1: Event.
r0: No Event.
w1: Clear flag.
w0: No change.

LAC **Lock After Capture**
r/w1: Enable.
r/w0: Disable.
Refer to section 7.1.5.2

RCR **Reset Capture Register**
r/w1: Reset capture register permanently to 0xFFFF.
r/w0: Release capture register.

CCxL **CAPCOM x Capture/Compare Register low byte**

	7	6	5	4	3	2	1	0	
r	Read low byte of capture register and lock it.								
w	Write low byte of compare register and lock it.								
	1	1	1	1	1	1	1	1	Res

CCxH **CAPCOM x Capture/Compare Register high byte**

	7	6	5	4	3	2	1	0	
r	Read high byte of capture register and unlock it.								
w	Write high byte of compare register and unlock it.								
	1	1	1	1	1	1	1	1	Res

18. Stepper Motor Module VDO (SMV)

The SMV module serves to control air cored movements or stepper motors that are directly coupled in H-bridge formation to H-Ports. Upon CPU programming it creates all waveforms necessary to position the drive pointer as desired. In addition it supports the Rotor Zero Position Detection by supplying motor blockage information.

The Rotor Zero Position Detection capability is protected by a patent from Mannesmann VDO and may only be used with VDO's prior approval.

The number of motors that are controllable by subunits (control units) of the module is given in Table 18–1.

Features

- Multi channel pulse width modulated output
- Outputs offset for improved EMC properties
- Four quadrant operation
- 8bit resolution
- Analog voltage sampling for Rotor Zero Position Detection support
- HW Option selectable output cycle frequency

18.1. Principle of Operation

18.1.1. General

An 8bit, free-running counter FRC (Fig. 18–1) operates on the f_{SM} input clock (generally 4MHz) and creates an 8bit counter word that is fed to a number of control units SMx.

A control unit (Fig. 18–1) contains 8bit sine and cosine compare registers. One comparator each is associated with these registers and creates a compare signal when register content and FRC word are equal. An output flip-flop associated with each comparator is set when the FRC word is zero and reset by the respective compare signal. A delay stage associated with each control unit delays the flip-flop output signals by a fixed number of f_{SM} cycles to achieve non-synchronism between the output signals of the various control units, thus achieving an improved EMC behavior of the SMV (cf. Fig. 18–3). According to the setting of a quadrant register associated with each control unit, each of a unit's two output signals is multiplexed to signals SMxn+ and SMxn- so as to properly control 2 individual H-Ports that form an H-bridge together with the connected motor coil. By these means, a control unit supplies two H-bridges with signals SMx1+, SMx1-, SMx2+ and SMx2- to function as variable pulse width modulator outputs with selectable polarity.

Summing up: when the compare registers are set to the sine and cosine value of a desired rotor angle and the quadrant register is set to the desired quadrant, an air cored movement or a stepper motor connected to the unit's 4 H-Ports will carry the proper average coil currents of proper polarity so that its rotor will assume the desired rotary angle.

Three registers control readjustment of a rotor to a new angle. Sine, cosine and unit/quadrant registers serve as temporary storage of new sine, cosine, related quadrant and unit selection values. A scheduler logic times the synchronous downloading of the three buffered words to the respective unit's sine, cosine and quadrant registers, so as to avoid inconsistencies among them. A Busy bit may be read out signaling completion of the downloading.

Each control unit contains circuitry to detect an induced voltage resulting from the rotation of the connected motor's rotor (Fig. 18–2). A comparator compares the input voltage from one of the unit's H-Ports to 1/9th of the supply voltage. A capture logic opens a capture window and samples the comparator output. The capture result signal supplies a rotor blockage information necessary for the Rotor Zero Position Detection in all cases where the CPU has lost track of the display angle of a pointer that is driven by the motor via a mechanical transmission.

For the effect of CPU clock modes on the operation of this module refer to section "CPU and Clock System" (see Table 4–1 on page 36).

18.1.2. Hardware settings

Prior to entering active mode, the f_{SM} input clock has to be set by HW Option (see Table 18–1 on page 108). A frequency value of 4MHz is recommended resulting in a pulse width modulator cycle frequency of 4MHz/256.

Some H-Ports may receive the output signals either of the SMV module or of PWM modules as an alternative. Refer to Table 18–1 for the necessary settings.

Refer to section "HW Options" for details.

18.1.3. Initialization

Prior to entering active mode, proper SW initialization of the H-Ports assigned to function as H-bridge outputs SMxn+ and SMxn- has to be made (Table 18–1). The H-Ports have to be configured Special Out. Refer to "Ports" for details.

18.1.4. Operation

After reset, the SMV is in standby mode (inactive). The output lines to the H-Ports are low.

For entering active mode, set bit SR0.SM. The FRC will immediately start counting but the control units' output lines will still be low.

18.1.4.1. Generating Output

After entering active mode, the SMV's control units are ready to receive sine, cosine and quadrant values.

First load the unit/quadrant information to register SMVC, then the cosine value to register SMVCOS and last the sine value to register SMVSIN. Upon writing SMVSIN, the scheduler logic will set flag SMVSIN.BUSY and load the buffered values to the respective unit's sine, cosine and quadrant registers on the next zero transition of the FRC, after a maxi-

Table 18–1: Unit specific settings

Contr. Unit	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
SMA			SMAn+/- outputs	H4.0 to H4.3 special out	SR0.SM
			SMA-COMP input	H4.0 special in	
SMB			SMBn+/- outputs	H3.0 to H3.3 special out	
			SMB-COMP input	H3.0 special in	
SMC			SMCn+/- outputs	H2.0 to H2.3 special out	
			SMC-COMP input	H2.0 special in	
SMD			SMDn+/- outputs	H5.0 to H5.3 special out	
			SMD-COMP input	H5.0 special in	
SME	SME/PWM selection	PM.H7	SMEn+/- outputs	H7.0 to H7.3 special out	
			SME-COMP input	H7.0 special in	
SMF			SMFn+/- outputs	H1.0 to H1.3 special out	
			SMF-COMP input	H1.0 special in	
SMG	SMG/PWM selection	PM.H0	SMGn+/- outputs	H0.0 to H0.3 special out	
			SMG-COMP input	H0.0 special in	
All	Input clock selection	SM			

mum of 256 f_{SM} input clock cycles. After completing the download, flag BUSY is reset and the respective unit will immediately start producing the output signals with the desired timing (see Table 18–4) on the proper pins (see Table 18–3).

The above procedure for loading values to a first unit is repeated for all others. Make sure that the BUSY flag is 0 before rewriting registers SMVC, SMVCOS and SMVSIN.

18.1.4.2. Rotor Zero Position Detection

During Rotor Zero Position Detection one of a unit's H-Ports (Table 18–1) has temporarily to be operated as input to an internal analog comparator. Reconfigure this port as Special Input. Refer to "Ports" for details.

Reading of the induced voltage at the measured motor winding is started by setting the questioned unit's control bit SMVCMP.ACRx to 1. The respective analog comparator's output will now be sampled. Once three consecutive "1" samples (spaced $1/f_{CPU}$) - indicating a sufficient analog comparator input voltage - are received, a 1 may be read from the questioned unit's result flag SMVCMP.ACRx, indicating that the Rotor Zero Position Detection is under way.

Resetting the questioned unit's control bit SMVCMP.ACRx to 0 stops the sampling and resets the result flag. When after a restart of the above sampling procedure and after a sufficiently long capture period still no 1 was read from the questioned unit's result flag SMVCMP.ACRx, this indicates that Rotor Zero Position Detection is complete.

Parallel Rotor Zero Position Detection on all control units is permitted.

After completion of Rotor Zero Position Detection, reconfigure the comparator input port as Special Out.

18.1.5. Inactivation

Returning the SMV module to standby mode by resetting bit SR0.SM will immediately halt the FRC, return all output signals to 0, reset all internal registers and disconnect the comparators from supply.

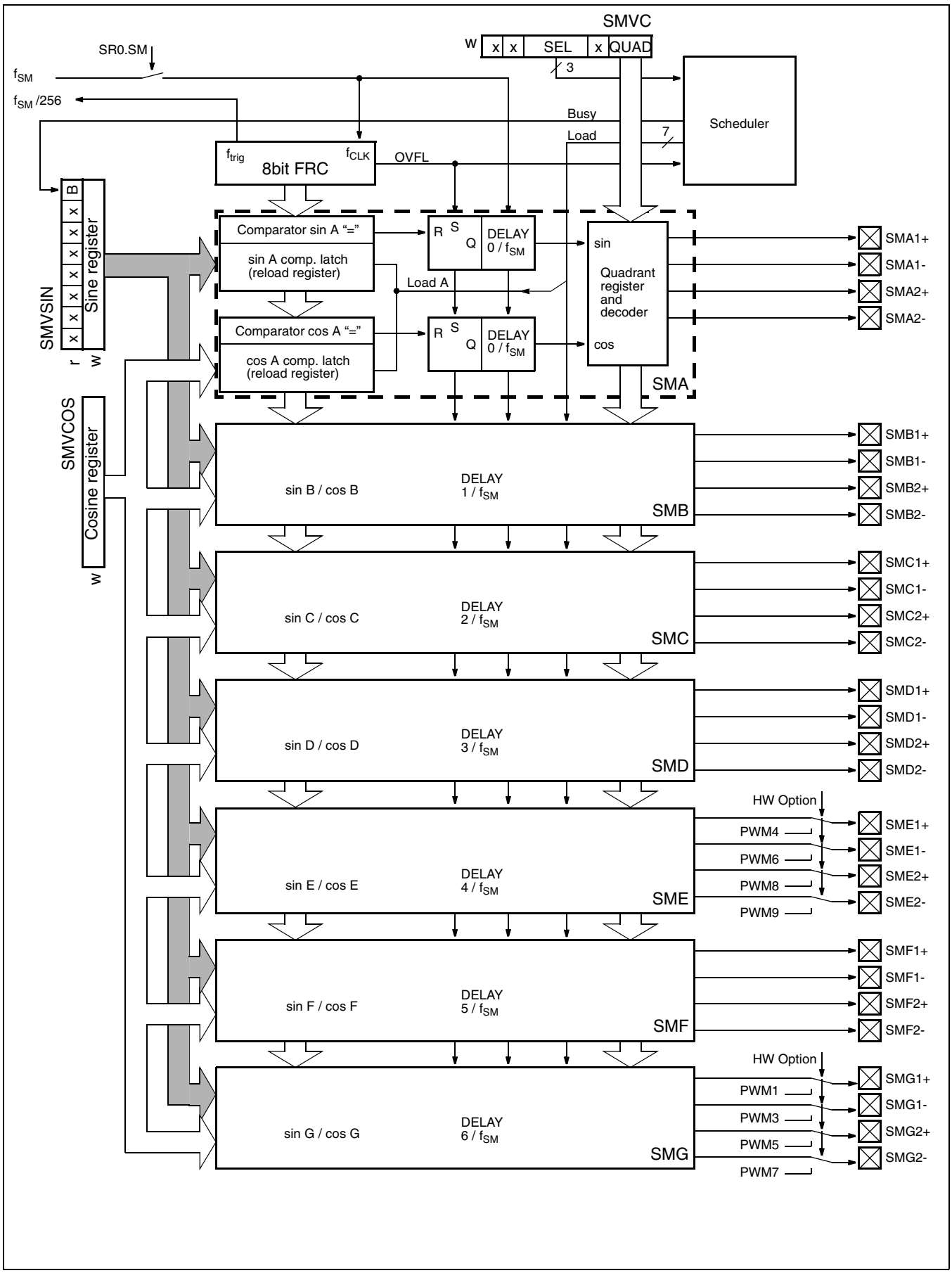


Fig. 18–1: Block Diagram of Output Generation Circuit

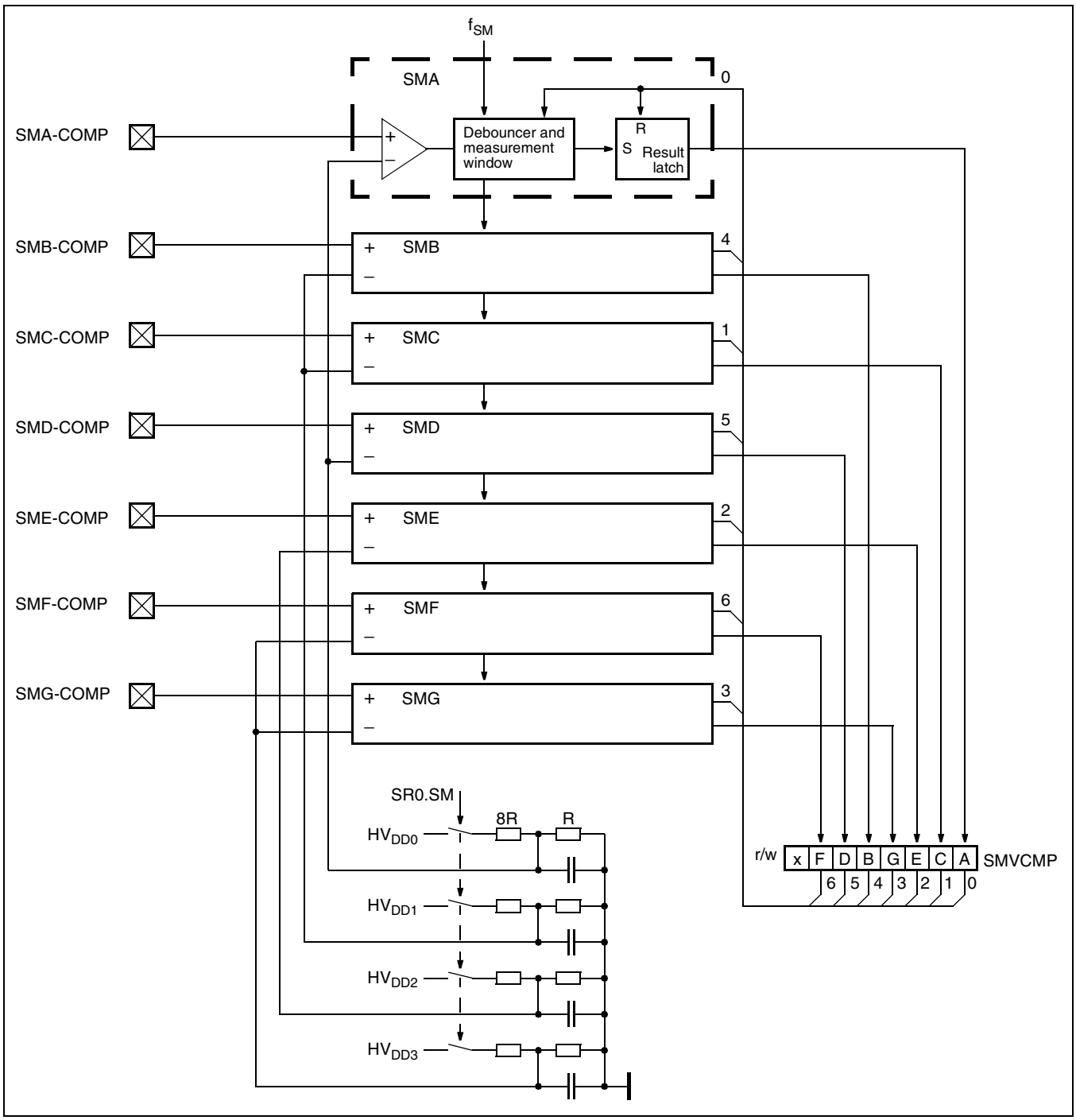


Fig. 18–2: Block Diagram of Rotor Zero Position Detection Circuit

18.2. Registers

SMVC								Stepper Motor VDO, Control Register
	7	6	5	4	3	2	1	0
w	x	x	SEL			x	QUAD	
	x	x	0	0	0	x	0	0 Res

SEL **Control unit Selection field (Table 18–2)**

QUAD **Quadrant selection field (Table 18–3)**

Table 18–2: SEL usage

SEL	selected control unit
000	SMA
001	SMB
010	SMC
011	SMD
100	SME
101	SMF
110	SMG
111	Not permitted

Table 18–3: QUAD setting and resulting control unit output signal function

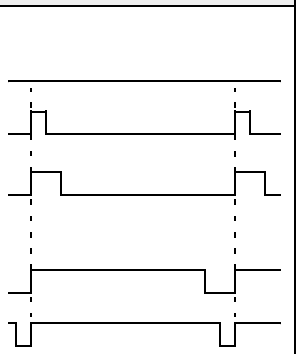
QUAD	Control unit output signal function			
	SMx1+	SMx1-	SMx2+	SMx2-
00	sine	VSS	cosine	VSS
01	sine	VSS	VSS	cosine
10	VSS	sine	VSS	cosine
11	VSS	sine	cosine	VSS

SMVSIN								Stepper Motor VDO, Sine Register
	7	6	5	4	3	2	1	0
r	x	x	x	x	x	x	x	BUSY
w	8bit Sine Value							
	0	0	0	0	0	0	0	0 Res

SMVCOS								Stepper Motor VDO, Cosine Register
	7	6	5	4	3	2	1	0
w	8bit Cosine Value							
	0	0	0	0	0	0	0	0 Res

BUSY **Scheduler Busy Flag**
r0: Scheduler not busy
r1: Scheduler busy, do not write registers SMVC, SMVCOS, SMVSIN

Table 18–4: Usage of SMVSIN and SMVCOS registers

Value	Duty factor	Pulse Diagram
00h	0/256 (continuously low)	
01h	1/256	
02h	2/256	
:	:	
FEh	254/256	
FFh	255/256 [1])	

[1]) 256/256 (continuously high) is not available.

SMVCMP								Stepper Motor VDO, Comparator Register
	7	6	5	4	3	2	1	0
r/w	x	ACRF	ACRD	ACRB	ACRG	ACRE	ACRC	ACRA
	x	0	0	0	0	0	0	0 Res

ACRA to G **Analog Comparator Control and Result for SMA to SMG**
r0: Capture result: no induced voltage detected
r1: Capture result: induced voltage detected
w0: Stop capture and clear result flag
w1: Start capture

18.3. Timing

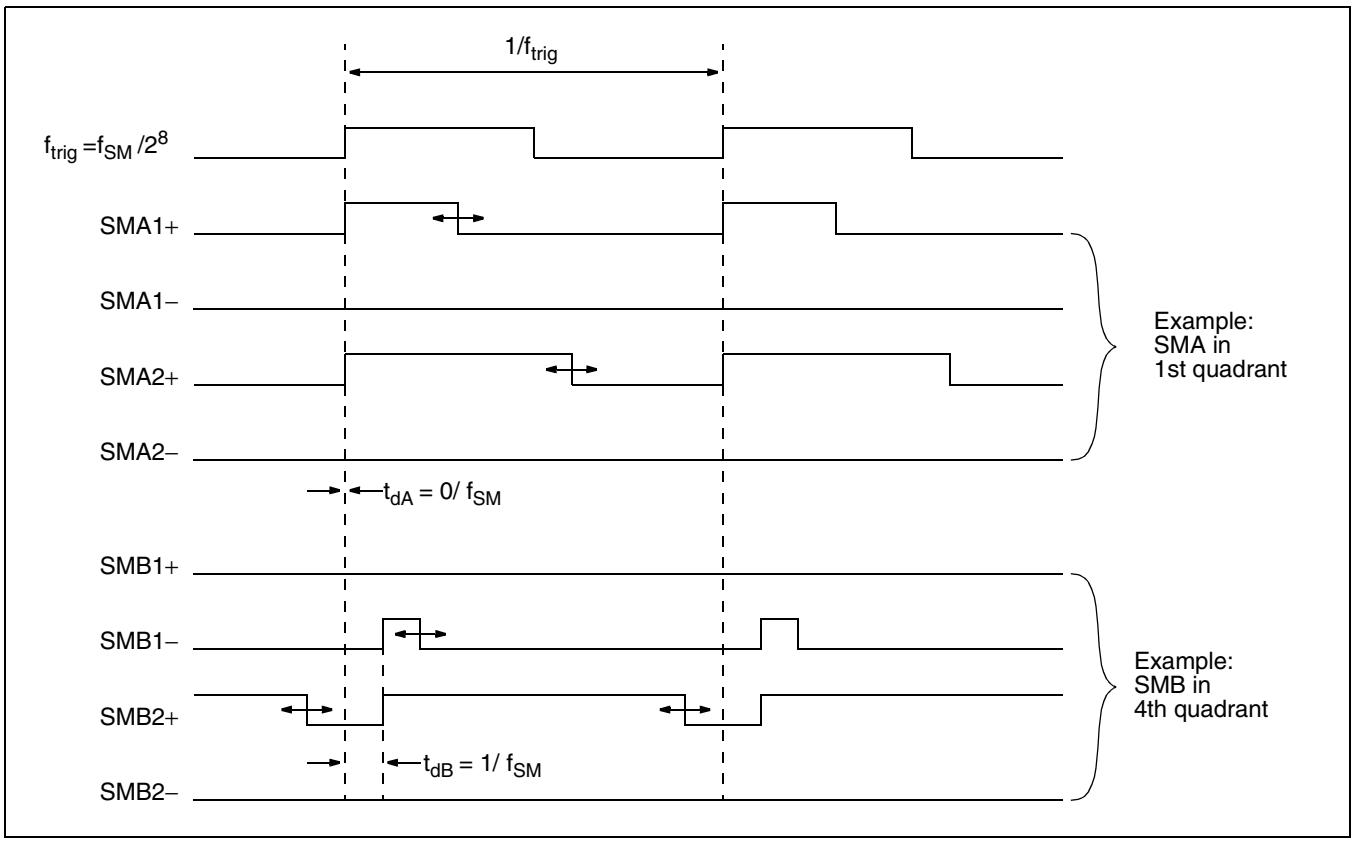


Fig. 18–3: Timing Diagram of Output Signals

19. LCD Module

The Liquid Crystal Display (LCD) Module is designed to directly drive a 1:4 multiplexed liquid crystal display. It generates all signals necessary to drive 4 backplane and 48 segment lines which are output via U-Ports in LCD mode. Up to 192 segments or pixels can be controlled if all U-Ports are designated as segment outputs.

In addition, the module provides functions that enable the user to cascade it with external expansion ICs providing more segment lines. It can be operated as master or slave in such an extended system.

Features

- 1:4 multiplex
- 5V supply
- Maximum of 192 segments
- Cascadable with external expansion ICs
- 0.3mA buffered 1/3 and 2/3 voltage divider
- Zero standby current
- 200µA no load active current
- Frame frequency HW Option selectable

19.1. Principle of Operation

19.1.1. General

Each LCD pixel or segment which is controlled by the LCD module is located at the crossing point of a segment line and a backplane line. The LCD module co-ordinates the output sequences of backplane and segment lines (see Fig. 19–3 on page 115).

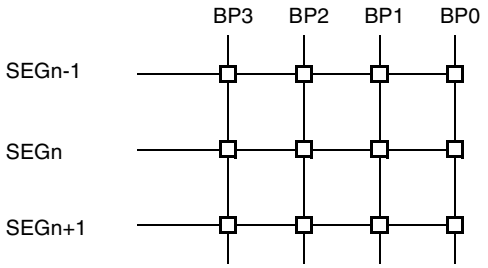


Fig. 19–1: Segments and Backplanes

A segment pin can drive 4 different voltage levels (UVSS, 1/3 UVDD, 2/3 UVDD, UVDD) in LCD mode. The output of each segment pin is controlled by the corresponding segment bits of the registers UxD, UxTRI, UxNS and UxDPM (further called segment registers). Each such register contains one bit (of a 4 bit segment field) for each of its port pins. Each segment bit (0 to 3) of a segment field corresponds to a backplane line (BP0 to BP3). If the segment bit, corresponding with the backplane line BPx is true, then the segment at the crossing of the two lines is on (black).

The LCD module does not contain a display ROM translating character information into segment code. The advantage is that arbitrary characters or displays can be generated just by changing the program code. Segment information is directly entered by writing to the corresponding segment bit. It is validated (loaded to all corresponding slave registers) for all segment U-Ports simultaneously by a write access to register ULCDLD.

Two internal voltage sources provide the U-Port circuits and the backplane generator with the voltage levels 1/3 UVDD and 2/3 UVDD. These levels are generated by a buffered resistor divider.

19.1.2. Hardware settings

The LCD frame frequency is settable by HW option LC. The resulting frame frequency is the selected input frequency, divided by 120. It should be in the range from 50 to 200Hz.

For best electromagnetic interference results it is recommended to operate all segment and backplane U-Ports in Port Slow mode. Refer to “Ports” for more details and to “HW-Options” for setting the corresponding HW options. Set flag PSLW in register SR0 to HIGH to enable Port Slow mode.

19.1.3. Initialization

After reset, the LCD module is in standby mode (inactive) and all U-Ports are in Port mode, non-conducting.

All U-Ports designated to function as backplane or segment outputs are to be set to LCD mode. Refer to “Ports” for more details. This will set these U-Ports to output LOW state.

After reset the content of the segment registers is undefined. It must be set by writing the desired segment information to the segment registers and by validating it by a write access to register ULCDLD (write 0x00 for master mode, 0xFF for slave mode), before the LCD module is enabled.

19.1.4. Operation

For entering active mode, set flag LCD in register SR0. Each segment and backplane U-Port will immediately start producing its LCD output signal according to the segment information provided during initialization.

During active mode, a new segment information is entered by simply writing the desired segment information to the segment registers and by validating it by a write access to register ULCDLD (write 0x00 while in master mode, 0xFF while in slave mode). Each segment and backplane U-Port will immediately start producing an LCD output signal according to the new segment information.

Returning the LCD module to standby mode by resetting flag LCD in register SR0 will immediately return all segment and backplane U-Ports to the output LOW state.

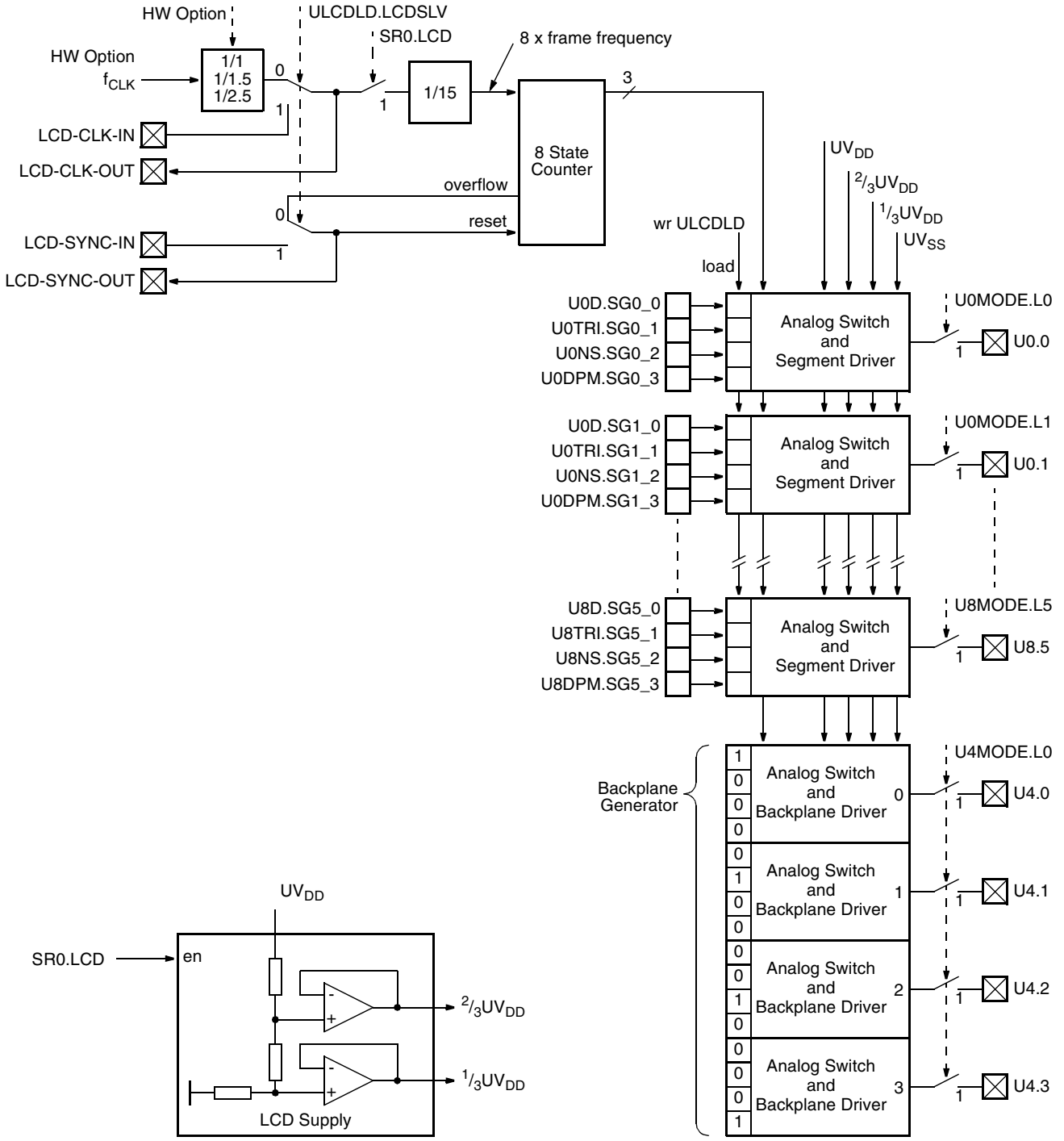


Fig. 19–2: Block Diagram

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

19.1.5. Cascading of LCD Driver Modules

For expansion purposes, the LCD module may be cascaded with external LCD driver ICs. Master or slave mode is selectable for the LCD module while in standby. Special signals provide phase and frequency synchronism for the LCD frame among the cascaded ICs.

For master mode, set flag LCDSLV in register ULCDLD LOW. The module always directs signal LCD-SYNC-OUT to pins U8.5 and LCD-CLK-OUT to pins U8.3. They connect to external slave ICs’ SYNC-IN and CLK-IN inputs for synchronization.

For slave mode, set flag LCDSLV in register ULCDLD HIGH. Configure pins U8.4 and U8.2 to receive signals LCD-SYNC-IN and LCD-CLK-IN from an external master IC’s SYNC-OUT and CLK-OUT outputs. These signals will then substitute the LCD module’s own HW option frame frequency settings.

Starting up and shutting down such an expanded system is described in section 19.3.

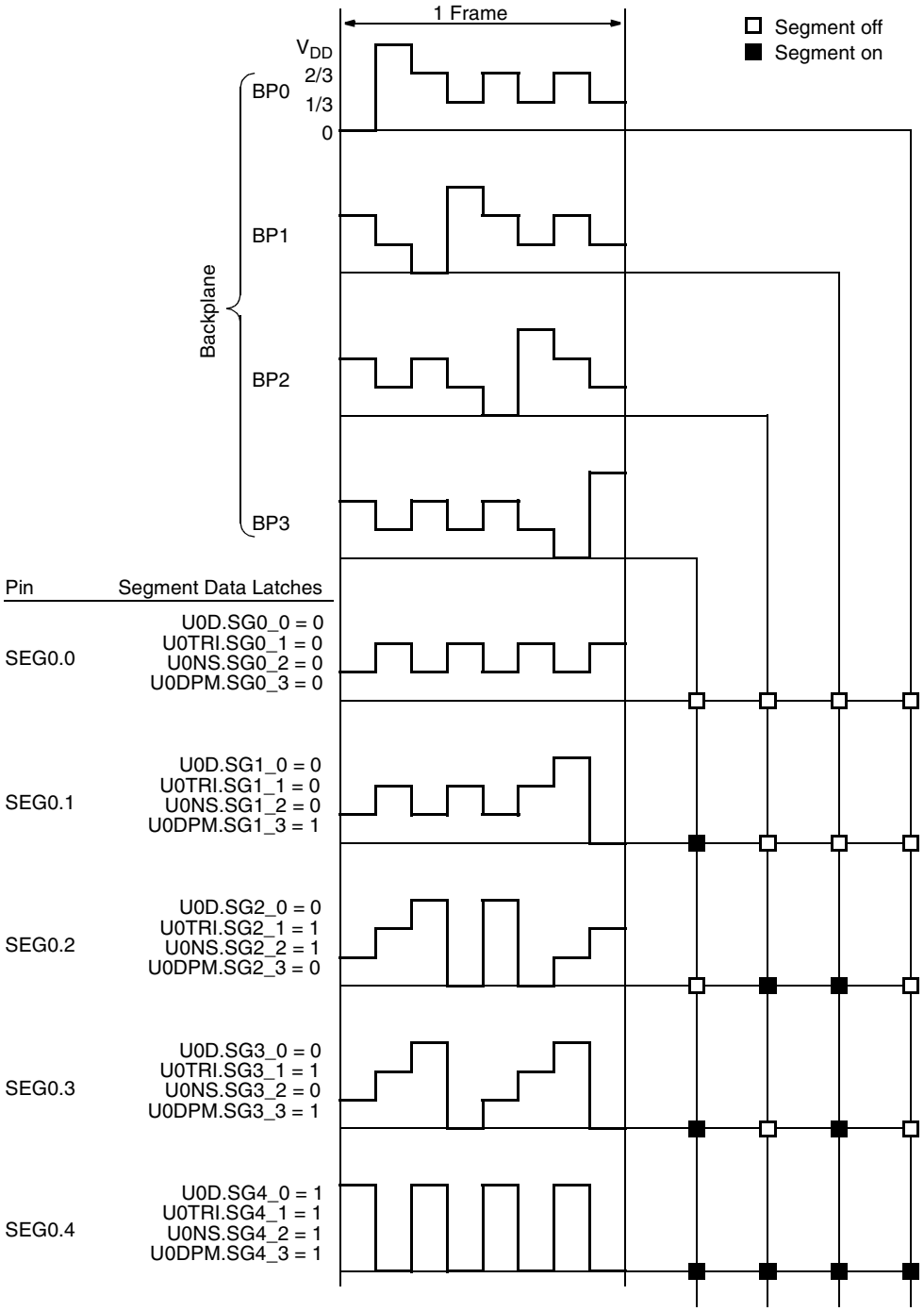


Fig. 19–3: Frame Timing Diagram

A segment at a crossing of backplane and segment lines is turned black when at the same time the backplane driver outputs a full swing and the segment driver outputs a full swing of opposite polarity.

19.2. Registers

Please refer to section “Universal Port Registers” for details on segment register layout.

ULCDLD				Universal Port LCD Load Register				
	7	6	5	4	3	2	1	0
w	LCDSLV	x	x	x	x	x	x	x
	0	0	0	0	0	0	0	0 Res

LCDSLV LCD Module is Slave
Select the mode of the LCD module.
w1: LCD module is slave.
w0: LCD module is master.

A write access to this memory location simultaneously loads all segment information of all U-Ports in LCD mode to the display.

19.2.1. Special Register Layout of U-Port 4

U4.0 to U4.3 provide backplane signals in LCD Mode. To operate any ports as LCD segment driver it is necessary to switch all these ports to LCD mode. This has to be done by setting flags U4MODE.L0 through U4MODE.L3.

As backplane ports U4.0 to U4.3 require no segment data setting, SG0_0 through SG3_3 bits are not available in U4 registers.

19.3. Application Hints for Cascading LCD Modules

19.3.1. Power On and Start Up Procedure

1. The SW in master and slave configures the corresponding IC.

Table 19–1: Suggested sequence

Master	Slave
Load LCD display register.	Load LCD display register.
Clear flag LCDSLV.	Set flag LCDSLV.
LCD-CLK-OUT, and LCD-SYNC-OUT: Configure universal ports as Special Out Ports.	LCD-CLK-IN, and LCD-SYNC-IN: Configure universal ports as Special In Ports.

2. Optionally the slave signals to the master via handshake link or an inter processor interface (IPI) that it is ready to display.

3. The slave continuously scans the inputs LCD-CLK-IN and LCD-SYNC-IN for the bit combination “01” (SW debouncing required).

4. The master LCD module is switched on. LCD-CLK-OUT and LCD-SYNC-OUT switch to “01”.

5. The slave CPU detects the bit combination “01” and immediately switches on the slave LCD module. The slave LCD now generates a display.

Note: During the time that the slave needs to detect the bit combination “01”, master and slave operate asynchronously. Suggestion: limit time to approximately 100 to 200ms.

6. The LCD modules now operate in controlled synchronization.

19.3.2. Operation

In order to obtain optimum synchronization of LCD switchover, a change of display must be coordinated between master and slave (preferably via IPI) in such a way, that the time lag between write accesses to ULCDLD of the master and of the slave is kept as small as possible. Suggestion: Lower ms range or customer specification.

19.3.3. Power Off Procedure

1. (Optional) The processor which decides that the display is to be switched off signals this to the other via IPI.

2. The slave continuously scans the inputs LCD-CLK-IN and LCD-SYNC-IN for the bit combination “11” (SW debouncing required).

3. The master LCD module is switched off. LCD-CLK-OUT and LCD-SYNC-OUT switch to “11”.

4. The slave CPU detects the bit combination “11” and immediately switches off the slave LCD module.

Note: Keep time delay as short as when switching on.

5. All LCD ports output a low signal now. The LCD display is now inactive.

20. DMA Controller

The DMA controller allows transferring data fields between internal memory and either an external IC via U-Ports (G-Bus), or an SPI module, with minimum CPU interaction.

DMA transfers can be triggered by the interrupt source output of the corresponding module (self timed), a dedicated DMA Timer output or a port interrupt.

The G-Bus is intended to support the operation of external LCD driver ICs (e.g. SED1560 by Epson):
The DMA module copies 8bit pixel data bytes by direct memory access (DMA) to the external IC's graphic RAM with help of that IC's internal autoincrement address counter, and without CPU interaction. Other off-chip registers, allowing control of the display behavior (blinking, scrolling, etc.), have to be addressed by CPU operations.

In SPI mode, the DMA module copies data bytes by direct memory access (DMA) to the SPIxD data register, self timed or under timing of the DMA timer and without CPU interaction, to construct long serial data transfer sequences. It frees the CPU of repeatedly reloading data, e.g. under interrupt control.

Features

- 3 DMA channels:
  direct 8bit data read or write between memory and U-Ports U5 and U7 (G-Bus),
  direct 8bit data read or write between memory and SPI0,
  direct 8bit data read or write between memory and SPI1
- 256 byte maximum DMA block size
- one byte DMA block alignment
- CPU cycle steal
- Interrupt on DMA sequence finished

20.1. Functions

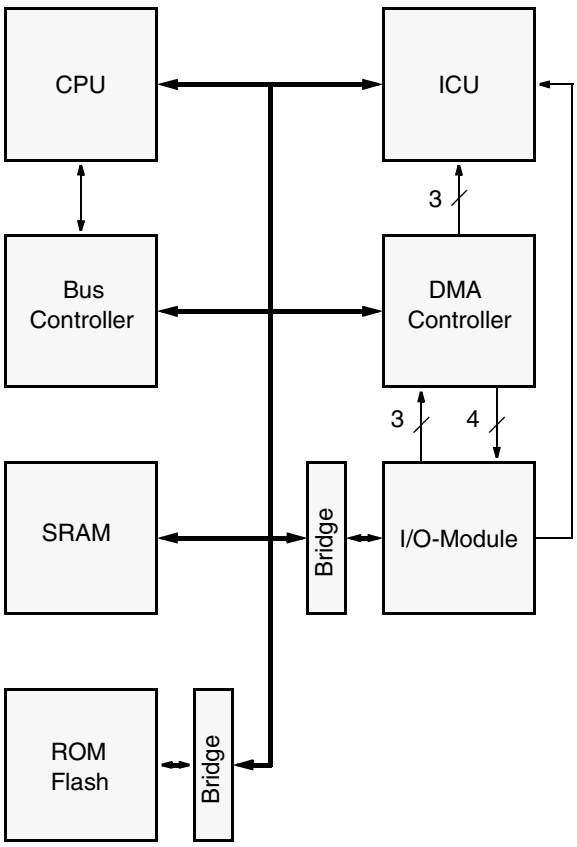


Fig. 20–1: System Block Diagram

The DMA Controller transfers bytes (8 bit) between I/O modules and memory. One transfer is called a DMA cycle. The transfer of a block of bytes is called a DMA sequence.

The DMA Controller contains one DMA channel logic for each DMA channel, the priority encoder, the control logic, the DMA vector base register, address and cycle count buffer, and the bus interface (see Fig. 20–2 on page 118).

The DMA vector base register points to the beginning of the DMA table which is filled with a DMA vector for each DMA channel. Location zero contains the default vector and is not assigned to any DMA channel. Each DMA vector is composed of a 24 bit source/destination address and a 8 bit cycle counter value (see Fig. 20–5 on page 119).

A DMA cycle is divided in a sequence of three steps:

1. Output Address of the DMA vector and read source/destination address and cycle counter.

2. Output Address of the DMA vector and write back incremented source/destination address and decremented cycle counter.

3. Output source/destination address and write/read data to/from I/O module.

Each step is one bus access which holds the CPU (cycle stealing). The DMA Controller generates the necessary control signals for above bus accesses.

An I/O module requests a DMA cycle via its interrupt source output which is connected to the DMA request input (DREQ) of the corresponding DMA channel logic. The DMA interrupt output (DINT) is connected to the ICU instead where it indicates the end of a DMA sequence (see Fig. 20–3 on page 119). The signal DINT is connected to the G-Bus logic too, where it sets a flag indicating the end of the DMA sequence (see Fig. 20–4 on page 119).

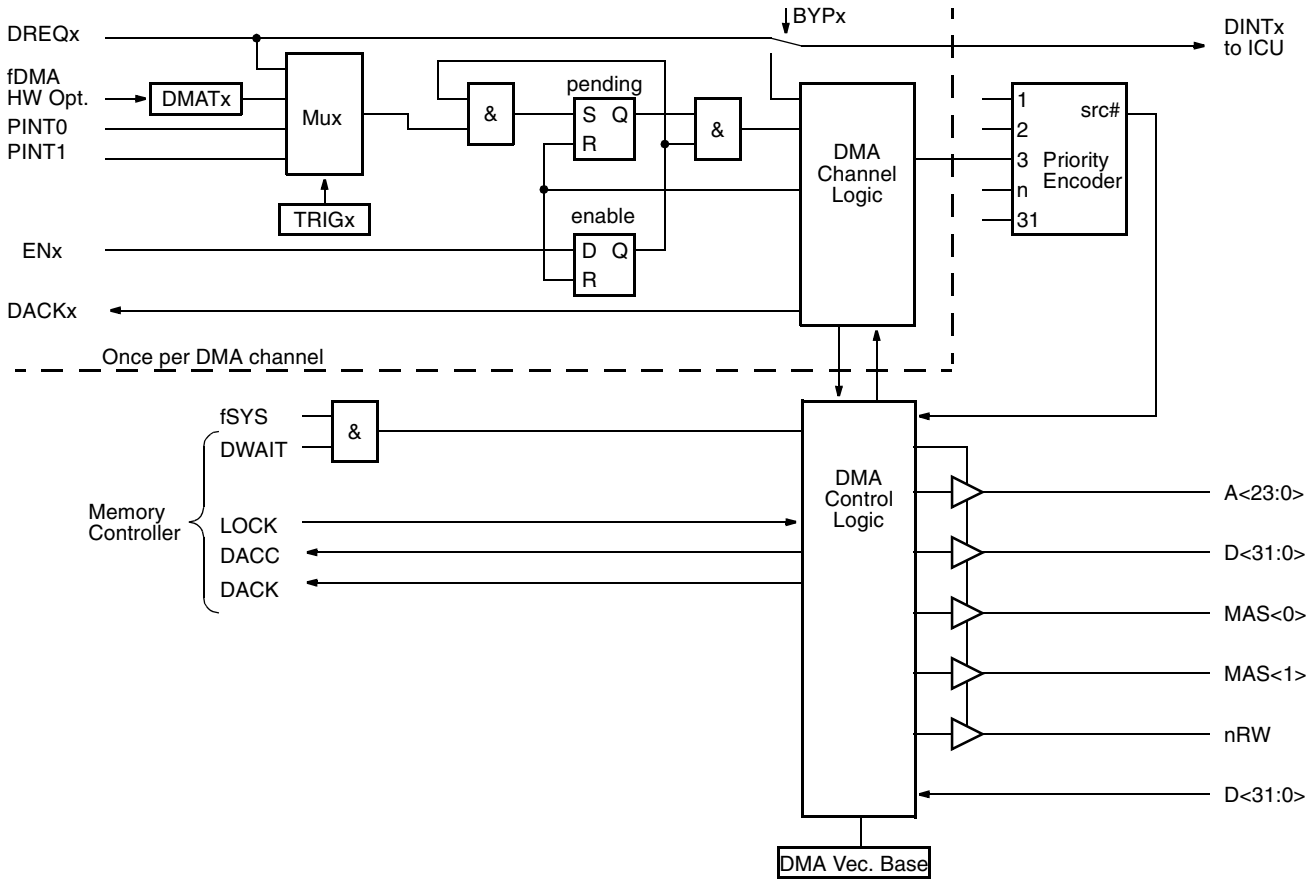


Fig. 20–2: DMA Controller

The DMA channel logic contains an input multiplexer which selects one of four possible DMA request sources (see Table 20–2 on page 120). The output of this multiplexer sets a pending flag which is automatically reset when the DMA cycle is finished. An enable flag (EN) masks the pending flag output to the priority encoder. A bypass flag (BYP) allows to redirect DREQ to DINT and thus generate no DMA request but an interrupt.

The priority encoder assigns each DMA channel a fixed unique priority (Table 20–1). This is necessary when more than one DMA channel signals a DMA request at the same time. The priority encoder outputs the source number with the highest priority.

The control logic controls the above described three steps of bus accesses and generates the DMA acknowledge signal (DACKx) which indicates to the requesting module that the DMA transfer has finished.

Table 20–1: DMA Channels

Priority	I/O-Module	Register Name
0	Default	
1	U-Port	GD
2	SPI 0	SPI0D
3	SPI 1	SPI1D

There are two fundamentally different modes to operate DMA sequences.

– Self timed describes the situation where the corresponding I/O module requests a DMA transfer when it's ready. In this case the I/O module starts the DMA module when there is something to transfer and the DMA controller starts the I/O module after the transfer is finished. This is the fastest possible way to transfer information via DMA. Trying to get it faster enforces the danger that one of the communication partners is not ready.

– External triggered describes the situation where a third party requests a DMA transfer. This can be a DMA timer or a port interrupt. The SW design has to guarantee that the I/O module as well as DMA controller can do their work between two consecutive DMA requests.

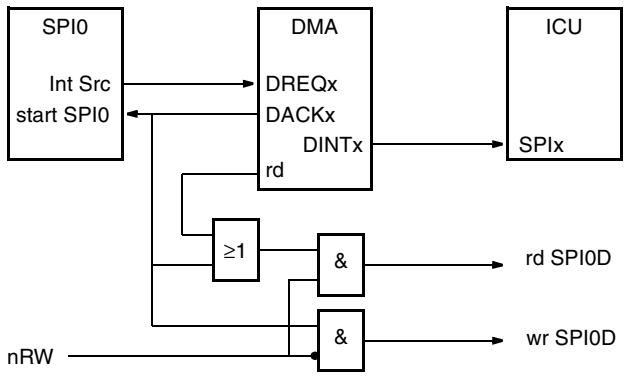


Fig. 20–3: DMA SPI Interaction

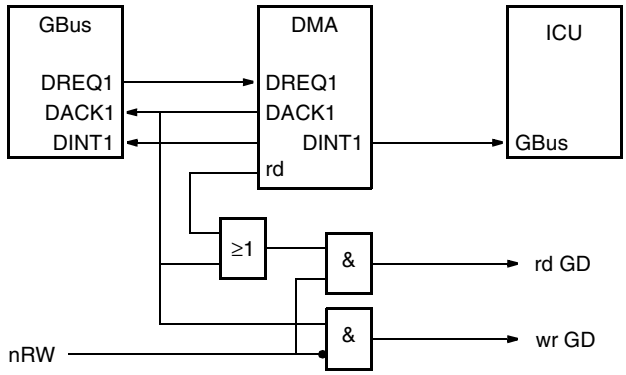


Fig. 20–4: DMA Port Interaction

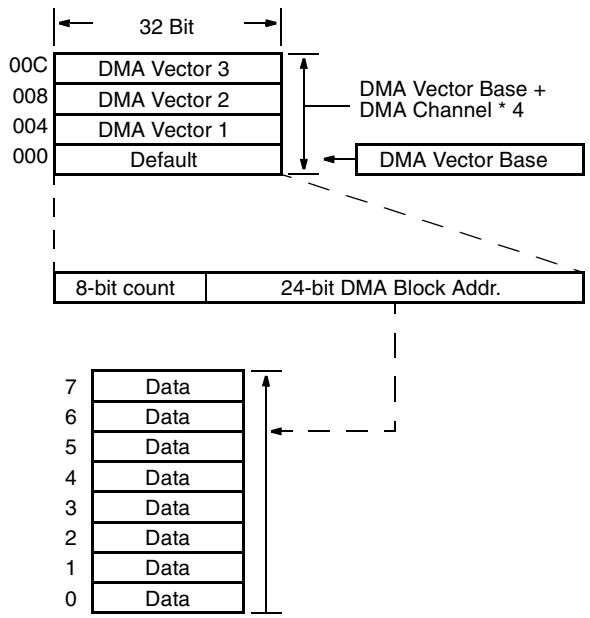


Fig. 20–5: DMA Vector Table

20.2. Registers

The DMA registers can be read or written 32-bit wide, asynchronous and without wait states.

DVB DMA Vector Base

	7	6	5	4	3	2	1	0	Offs
r/w	0	0	0	0	0	0	0	0	3
r/w	A23 to A16								2
r/w	A15 to A8								1
r/w	A7	0	0	0	0	0	0	0	0
	0x0000								Res

DST DMA Status Register

	7	6	5	4	3	2	1	0	Offs
r/w	DE	x	x	SRC					0
	0x00								Res

DE **DMA Enable**
r/w1: enable DMA controller
r/w0: disable DMA controller
Enables the DMA controller clock (fSYS) and the clock for all DMA Timer (fDMA).Before setting to 0, make sure that all individual DMA channels are terminated.

SRC **Priority source output**
r31-0: The number of the highest pending and enabled DMA request.

DCxM DMA Channel x Mode Register

	7	6	5	4	3	2	1	0	Offs
r/w	P	DMAT			TRIG				1
r/w	EN	x	x	x	BYP	DIR	MAS		0
	0x0000								Res

P **DMA Pending**
r1: DMA transfer pending
r0: No DMA transfer pending
w1: No action
w0: Clear P

DMAT **DMA Timer**
r/w7-0: DMA timing, equation:

$$f_{DMAT} = \frac{f_{DMA}}{2^{DMAT+1}}$$

TRIG **Trigger Source**
r/w15-0: (see Table 20–2)

Table 20–2: DMA Trigger Sources

TRIG				Source
3	2	1	0	
x	x	0	0	DMA request from I/O-module
x	x	0	1	DMATx
x	x	1	0	PINT0
x	x	1	1	PINT1

EN **Enable DMA channel**
r1: DMA sequence active
r0: DMA sequence finished
w1: enable DMA channel
w0: disable DMA channel

BYP **Bypass Interrupt**
r/w1: don't bypass DMA-Request to ICU
r/w0: bypass DMA-Request to ICU.

DIR **DMA Direction**
r/w1: write to I/O-module
r/w0: read from I/O-module

MAS **Memory Access Size**
r/w3: reserved
r/w2: 32-bit (not supported)
r/w1: 16-bit (not supported)
r/w0: 8-bit

20.3. Principle of Operation

The DMA Controller is operable in all CPU modes.

20.3.1. Initialization of the DMA Controller

The DMA vector table has to be installed starting at a 128 byte aligned address. See figure 20–5 for DMA vector layout. Write the start address of the DMA vector table as a 32 bit address to the DMA Vector Base register (DVB) and note that only bits 7 to 23 may be modified. The other bits are forced to zero. Enable the DMA controller by setting flag DE in the DMA Status register (DST).

The input frequency fDMA for all DMA timer can be selected by the register DMAC in the HW Options field.

20.3.2. Initialization of a DMA Channel

All steps necessary to initialize the involved I/O module have to be taken according to the description in the respective chapter.

Write the appropriate values to the DMA Channel Mode register (DCxM). Select the trigger source by field TRIG, program the DMA timer by field DMAT if necessary, select transfer direction (DIR) and size (MAS) and set BYP to one.

20.3.3. Self Timed DMA Write to I/O Operation

Flag DIR in register DCxM must contain a one for writing to an I/O module.

Write the source address (24 bit), pointing to the first plus one element, and the block size (8 bit) to the corresponding DMA vector table entry.

Start the DMA sequence by writing the first element to be transferred to the data register of the corresponding I/O module and enable the DMA channel.

20.3.4. Self Timed DMA Read from I/O Operation

Flag DIR in register DCxM must contain a zero for reading from an I/O module.

Write the destination address (24 bit), pointing to the first element, and the block size (8 bit) to the corresponding DMA vector table entry.

Start an SPI DMA sequence by writing to register SPIxD of the corresponding SPI module. The data of this write may be omitted. Then enable the DMA channel.

Start a Graphic Bus DMA sequence by reading from register GD. The data of this read may be omitted. Then enable the DMA channel.

20.3.5. External Triggered DMA Operation

The procedure is the same as with the self timed operation with some distinctions.

In both cases (read/write) the SW initiates the first action in the peripheral module. Enable the DMA channel after this module has finished it's work. Otherwise a DMA cycle may happen to early transferring invalid data.

It is possible to do external triggered DMA transfers without the SW initiating the first action. In this case the maximum block size is limited to 255 byte because the count value in the DMA vector has to be programmed with block size plus one. In a write case (Fig. 20–7), the sequence starts with data D1. In a read case (Fig. 20–8), the first DMA cycle reads invalid data D0. The first element of the transferred block has to be omitted in the latter case.

20.3.6. End of DMA Sequence

The end of the DMA sequence is indicated by the enable flag (EN=0) and an interrupt which calls the ISR of the corresponding I/O module.

The address field of the corresponding DMA vector points to the next element after the last transferred element. The counter field is at zero.

20.3.7. Enabling of a DMA Channel

Setting the flag EN to one enables the DMA channel. Make sure that there is no pending DMA request at that point of time. Clearing an active pending flag P and enabling the corresponding DMA channel must not be done with a single instruction. This might lead to an unwanted DMA cycle. First clear P and then set EN in two instructions.

20.3.8. Termination of a DMA Sequence

A final termination of a DMA sequence can be achieved by first disabling the DMA channel (DCxM.EN=0) and the source of the DMA requests and secondly clearing the pending flag (DCxM.P=0).

20.3.9. Disabling of the DMA Controller

First terminate all DMA channels (see 20.3.8.) and then clear flag DST.DE. Do not simply clear flag DST.DE, as this might result in undefined clock system behaviour.

20.4. Timing Diagrams

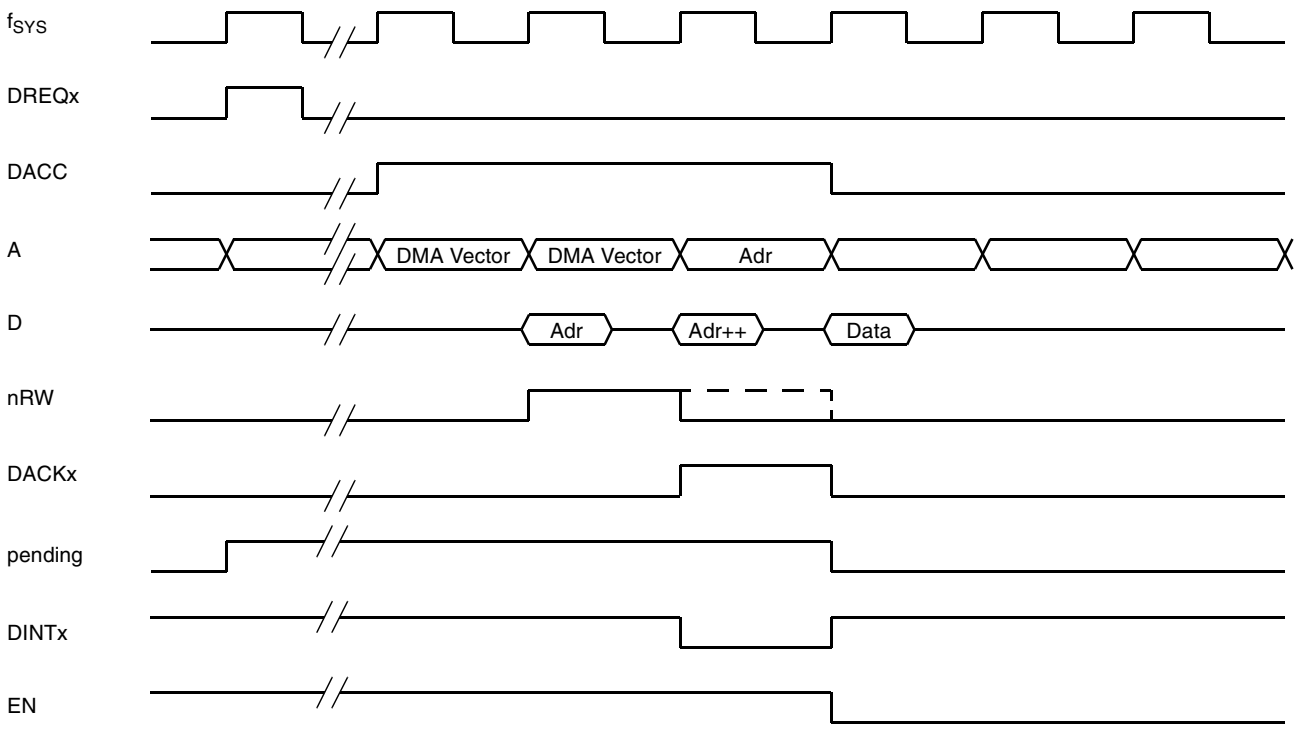


Fig. 20–6: DMA Cycle Timing

20.4.1. DMA Sequences SPI

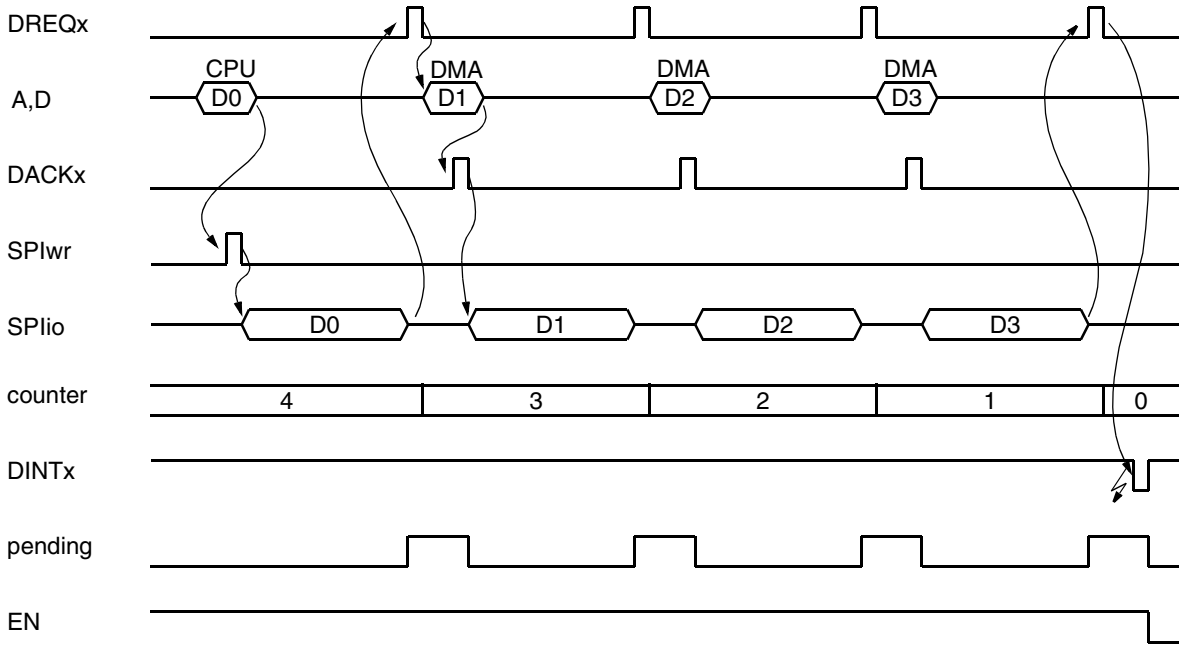


Fig. 20–7: SPI Write Sequence (serial out)

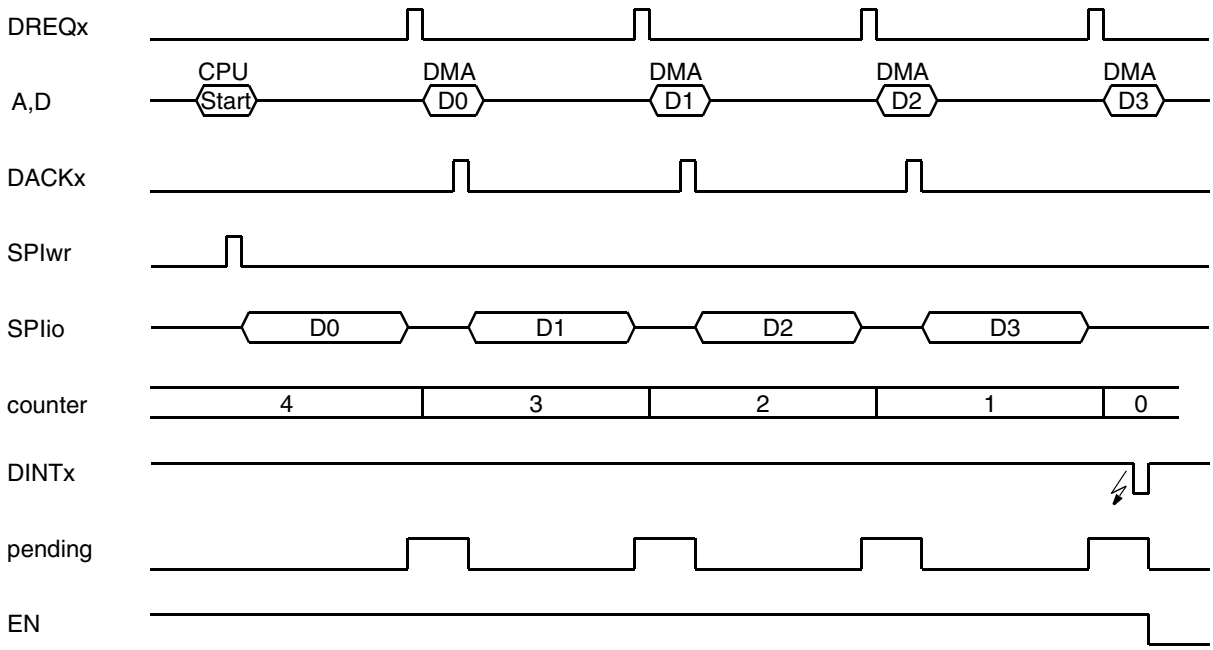


Fig. 20–8: SPI Read Sequence (serial in)

20.4.2. DMA Sequences Graphic Bus Interface

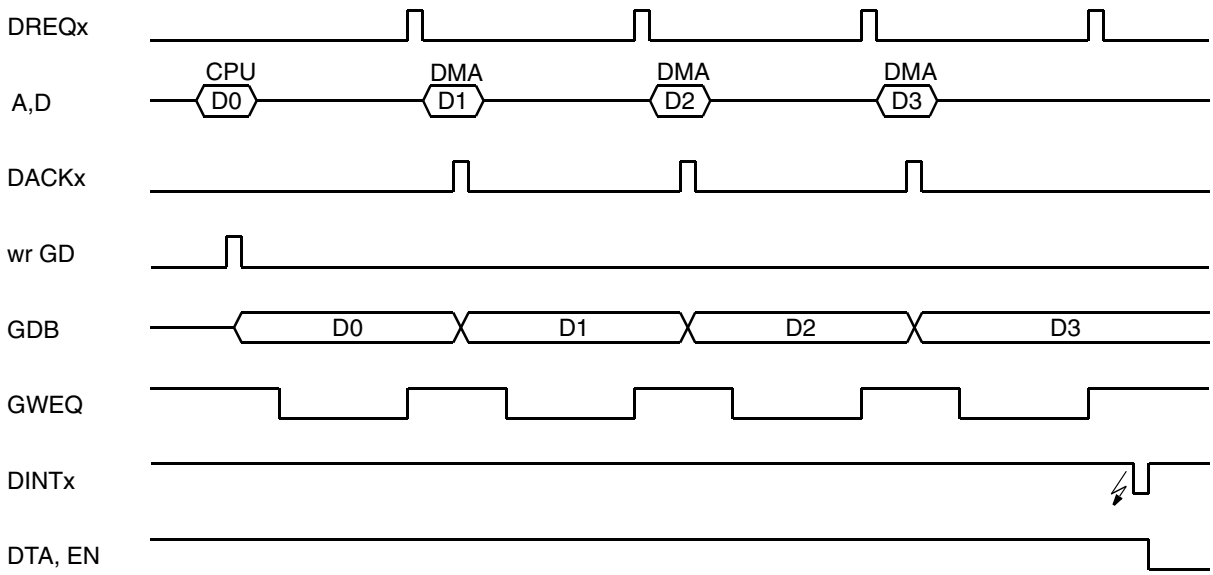


Fig. 20–9: Graphic Bus Write Sequence (parallel out)

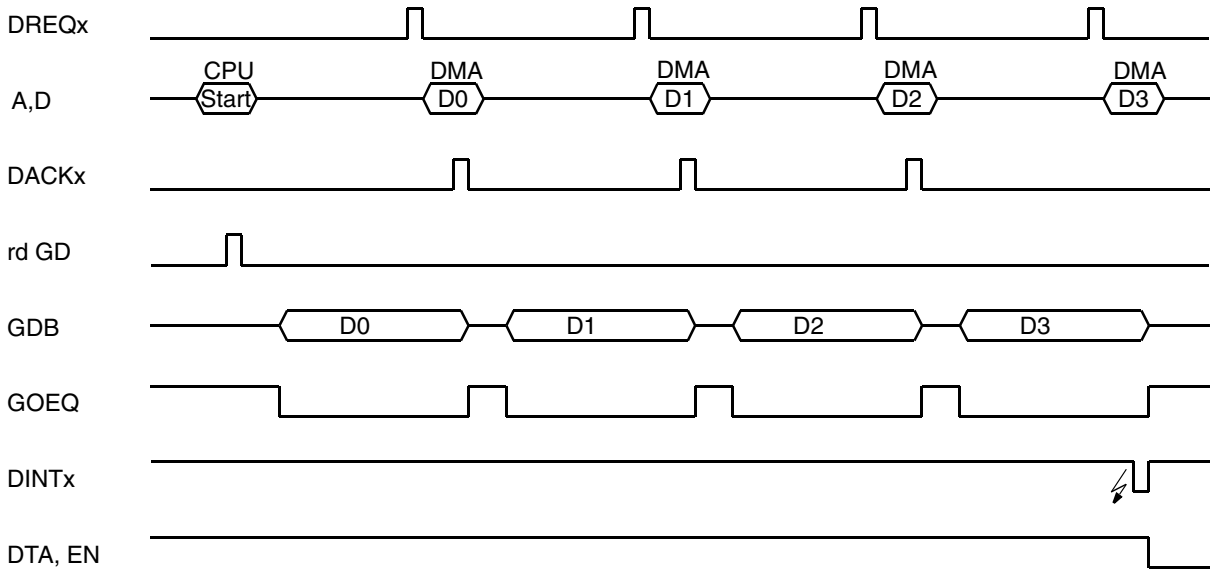


Fig. 20–10: Graphic Bus Read Sequence (parallel in)

The final DMA request pulse clears the DMA Transfer Active (DTA) flag additional to generating an interrupt.

21. Graphic Bus Interface

The Graphic Bus Interface (GB) is intended to support the operation of external LCD driver ICs (e.g. SED1560 by Epson).

Features

- DMA read/write to external device
- CPU read/write to external device
- Read/write timing generation
- Read/write control signals generation

21.1. Functions

The DMA module copies 8bit pixel data bytes by direct memory access (DMA) to the external IC's graphic RAM with help of that IC's internal autoincrement address counter, and without CPU interaction. Other off-chip registers, allowing control of the display behavior (blinking, scrolling, etc.), have to be written and read by CPU operations.

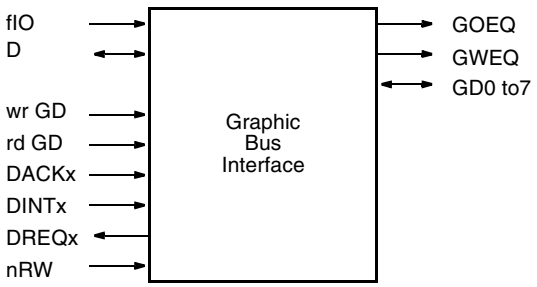


Fig. 21–1: Port Bus Block Diagram

The necessary timing is done autonomously by the GB logic. Any U-Port may be used as address output port operated by the CPU. Please refer to section DMA for information about GB DMA interaction.

The register GD provides the data interface for the GB. Writing to GD outputs the data byte at U5.0 to U5.3 (low nibble) and U7.4 to U7.7 (high nibble). Reading from GD inputs a data byte from above pins. The assignment to external signals is shown in table 21–1.

Table 21–1: Port Assignment

Port	Name	
U5.0	GDB0	External data bus
:	:	
U7.7	GDB7	
1)	GADB	External address bus
U6.2	GWEQ	External write signal
U6.1	GOEQ	External read signal
1) Any U-Port may be used as address output port.		

21.2. GB Registers

GD Graphic Bus Data Register

	7	6	5	4	3	2	1	0	Offs
r/w	Data								0
	0x00								Res

A write access to this register generates the DACK signal and writes to registers UxD. A read access to this register generates the DACK signal and reads from registers UxPIN.

GC Graphic Bus Control Register

	7	6	5	4	3	2	1	0	Offs
r/w	TIM				E	BSY	SEQ	DTA	0
	0x00								Res

TIM **GB Timer**

w15-1: GB timing, equation:

$$t_{GB} = \frac{2^{TIM+1}}{f_{IO}}$$

w0: GB logic is disabled, clock input is disabled

E **Enable**
r/w1: Enable timing generation
r/w0: Disable timing generation

BSY **Busy**
r1: GB timing is active
r0: GB timing is not active
Every DACKx signal or access to GD sets this flag and every DREQx signal clears it again.

SEQ **DMA Sequence**
r1: DMA sequence is active
r0: DMA sequence is not active
Every DACKx or access to GD signal sets this flag and the DINTx signal clears it again.

DTA **DMA Transfer Active**
r1: DMA sequence started
r0: DMA sequence is finished
w1: Set DTA
w0: No action
This flag indicates the end of a DMA sequence. It has to be set by SW before a DMA sequence is started. It is cleared by signal DINTx.

21.3. Principle of Operation

21.3.1. Initialization

Table 21–2 shows the necessary settings of the port configuration registers.

Table 21–2: Port Configurations

Register	Setting	Mode
U5MODE, U7MODE, U6MODE	0x00	Port mode
U5NS, U7NS	0x00	Normal
U6NS	0x06	Special
U5TRI, U7TRI, U6TRI	0x00	Out

Enable the timing generation by setting flag E in register GC. Enable the clock input and select the desired timing of the control signals GOEQ and GWEQ in the field GC.TIM. The minimum high time of the control signals is one fIO cycle.

21.3.2. Data transfer

Data to/from an external device can be transferred directly by CPU access or, especially for bigger amounts of data and with help of the external device's autoincrement address counter, a DMA sequence can be started. Make sure not to start a GB transfer unless the flags DTA, SEQ and BSY are zero.

21.3.2.1. DMA Write Sequence

After initialization of the corresponding DMA channel, set flag DTA to show others that a DMA sequence was initiated but not finished and write the first value to be transferred via the GB to the register GD. The DMA Controller writes the remaining bytes to register GD and generates an interrupt when finished. DTA low marks the end of the DMA sequence.

21.3.2.2. DMA Read Sequence

After initialization of the corresponding DMA channel, set flag DTA to show others that a DMA sequence was initiated but not finished and read the register GD. The DMA Controller reads the remaining bytes from register GD and generates an interrupt when finished. DTA low marks the end of the DMA sequence.

21.3.2.3. CPU Write Access

Writing the byte to register GD is sufficient. The end of the transfer is indicated by flag BSY.

21.3.2.4. CPU Read Access

The read access must be initiated by a dummy read access to register GD. After BSY is low the desired byte can be read from register GD. This last step automatically initiates the next read timing of the GB logic. If this is not desired, because GOEQ stays active until the next access to GD, after BSY became low, first disable the GB timing generation by clearing flag E in register GC and then read register GD.

21.3.3. Inactivation

Inactivation is easily done by writing GC.TIM to zero. Make sure not to switch off the GB as long as a transfer is active (DTA or SEQ or BUSY are set).

21.3.4. Precautions

A write to register GD alters the universal ports data latches U5D and U7D even if the GB is disabled (GC.TIM = 0).

21.3.5. Timings

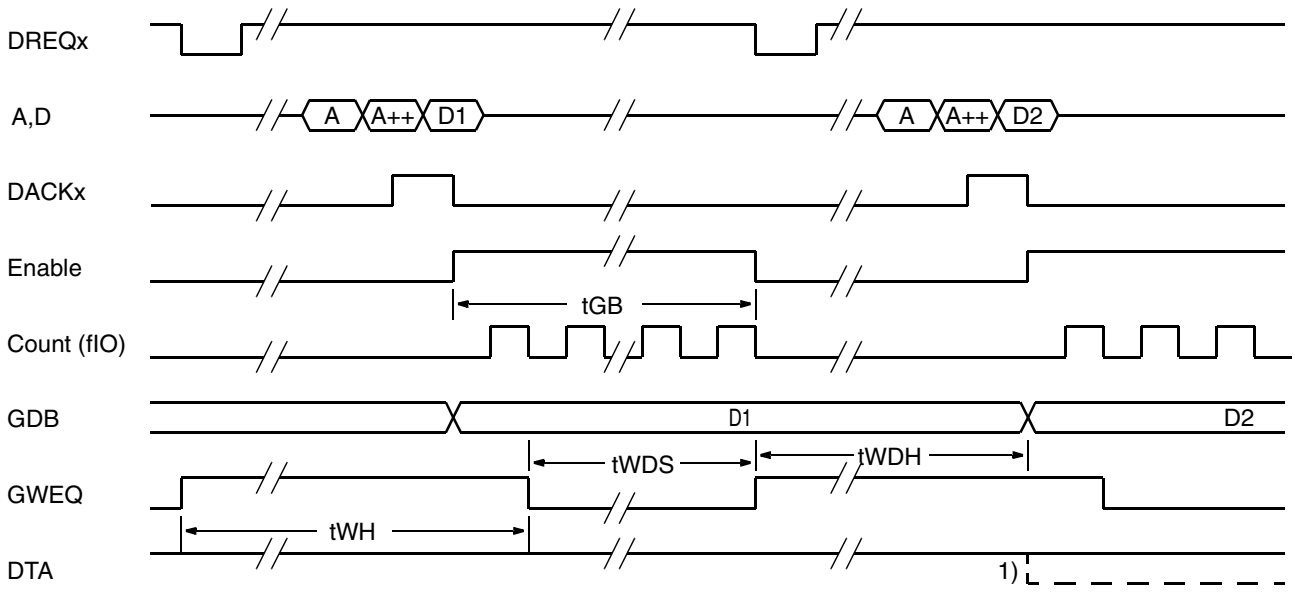


Fig. 21–2: DMA Write (parallel out)

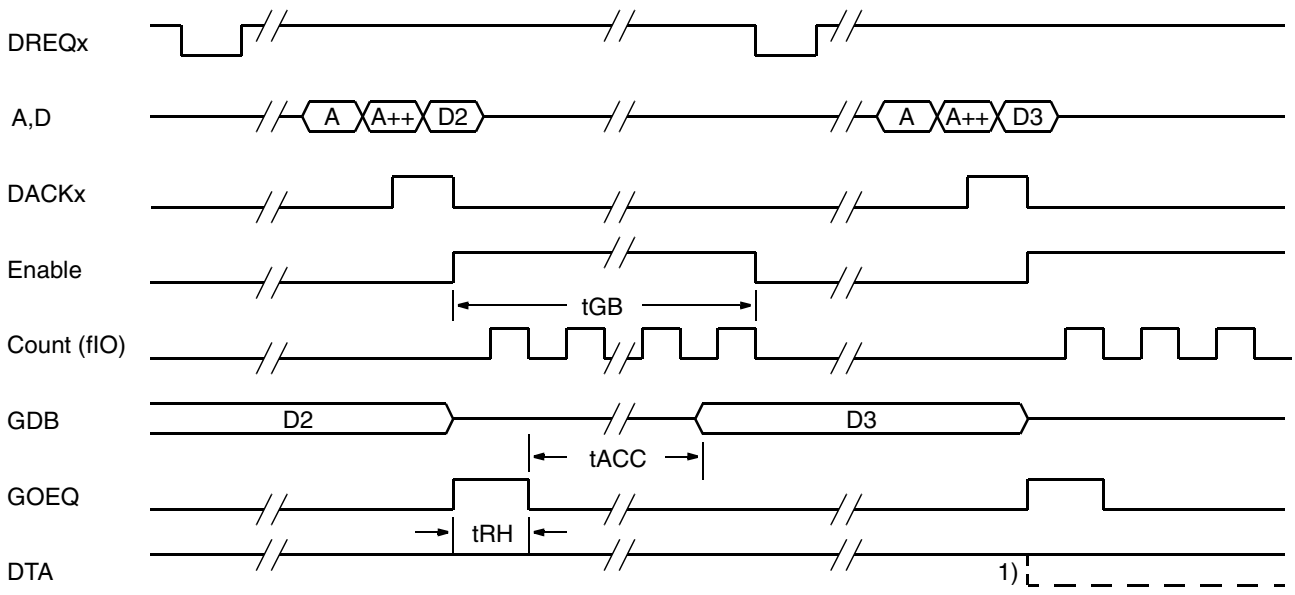


Fig. 21–3: DMA Read (parallel in)

1) DTA at the end of the last DMA cycle.

tWDS: Write data setup time
tWDH: Write data hold time
tWH: DMA write high time
tRH: DMA read high time
tACC: Read access time
tGB: GB time

DACKx can be replaced by write to GD or read from GD if direct CPU access is desired. The signals Enable and Count are internal signals.

22. Serial Synchronous Peripheral Interface (SPI)

A SPI module provides a serial input and output link to external hardware. An 8 or 9 bit data frame can be transmitted in synchronism to an internally or externally generated clock.

The SPI module can be operated via direct access or via DMA.

The number of SPIs implemented is given in Table 22–1. The “x” in register names distinguishes the module number.

Features

- 8 or 9 bit frames
- Internal or external clock
- Programmable data valid edge
- Programmable clock polarity
- Three internal clock sources programmable
- Input deglitcher for clock and data
- DMA interface

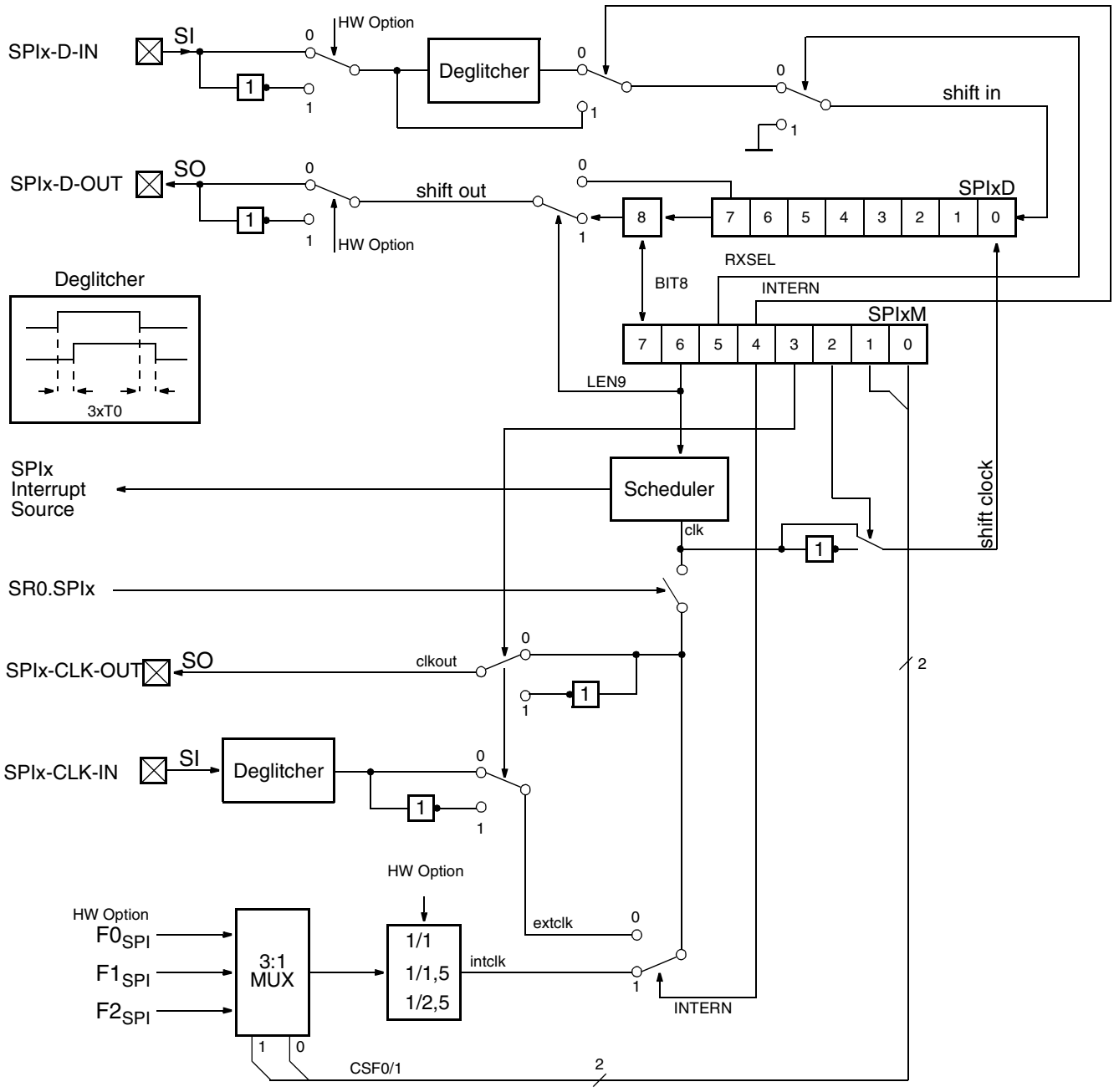


Fig. 22–1: Block Diagram

22.1. Principle of Operation

22.1.1. General

A SPI serves as an 8 or 9 bit wide input/output shift register. Either an internally or an externally generated clock can be used to shift data in and out.

The input SPIx-D-IN is connected to the LSB of the shift register. The output of the shift register is connected to output signal SPIx-D-OUT. Thus each time a frame is transmitted by shifting bits out, bits are shifted in simultaneously and vice versa. Deglitchers in the data and clock input paths are active only in external clock mode. The input and output can be inverted by HW Option.

If the deglitcher is active, input changes polarity after three consecutive samples have shown the same new polarity. Thus, a delay of three oscillator clock cycles is introduced. This feature imposes a limit on the maximum transmission frequency.

The interrupt is generated after the last bit is clocked out. The interrupt source output of this module is routed to the Interrupt Controller logic. But this does not necessarily select it as input to the Interrupt Controller. Check section “Interrupt Controller” for the actually selectable sources and how to select them.

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

22.1.2. Hardware settings

Clock frequency settings and the polarity of the data connections of the SPIs are settable by HW Options (Table 22–1). Refer to “HW Options” for setting them.

22.1.3. Initialization

After reset, a SPI is in standby mode (inactive).

Prior to entering active mode, proper SW configuration of the U-Ports assigned to function as data in- or outputs and clock in- or outputs has to be made (Table 22–1). Refer to “Ports” for details.

For entering active mode of a SPI, set the respective enable bit (Table 22–1).

Prior to operation, the desired clock frequency and telegram length have to be selected.

22.1.3.1. Clock Source

The SPI can be operated as clock master, using an internally generated clock, or as clock slave, using an externally generated clock.

The flag INTERN must be set in the SPIxM Mode register to operate the SPI as clock master. There are several options for selection of the internal clock. Each input of a 3 to 1 multiplexer can be programmed by HW Options to a different frequency. These three input frequencies F0SPI, F1SPI and F2SPI are used for all SPIs. The output of the 3 to 1 multiplexer is programmed by way of clock selection field (CSF) in register SPIxM. This clock can be used as shift clock directly, inverted and divided by 1.5 or 2.5. The shift clock is output by signal SPIx-CLK-OUT.

Table 22–1: Module specific settings

Module Name	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
All SPIs	F0SPI clock	SP0C			
	F1SPI clock	SP1C			
	F2SPI clock	SP2C			
SPI0	D in inversion	SP0C	SPI0-D-IN input	U3.5 special in	SR0. SPI0
	D out inversion	SP0C	SPI0-D-OUT output	U3.6 special out	
	Prescaler	SMC	SPI0-CLK-IN input	U3.4 special in	
			SPI0-CLK-OUT output	U3.4 special out	
SPI1	D in inversion	SP1C	SPI1-D-IN input	U4.0 special in	SR0. SPI1
	D out inversion	SP1C	SPI1-D-OUT output	U4.1 special out	
	Prescaler	SMC	SPI1-CLK-IN input	U3.7 special in	
			SPI1-CLK-OUT output	U3.7 special out	

If flag INTERN is zero, the SPI operates as clock slave and an externally generated clock is used. The external clock is input by signal SPIx-CLK-IN.

The polarity and the sampling edge of the clock is defined by field SCLK in register SPIxM.

22.1.3.2. Telegram Length

Flag LEN9 in register SPIxM defines the length of a transferred frame. The ninth bit of the shift register is read or written at the location of flag BIT8 in register SPIxM.

22.1.4. Operation

22.1.4.1. Transmit Mode

Transmission is initiated by a write access to data register SPIxD. The SPI will immediately begin transmitting the selected number of data bits out from its shift register, in synchronism with the selected clock. A write access during a transmission is ignored. The frame is transmitted MSB first. In nine-bit mode flag BIT8 is MSB of the shift register (Fig. 22–2 to 22–5). At the end of the frame, an interrupt source signal is generated which may be selected to trigger an interrupt.

22.1.4.2. Receive Mode

The receive mode must be activated by a write access to register SPIxD. The SPI will immediately begin clocking in the selected number of data bits into its shift register, in synchronism with the selected clock. At the end of the frame, an interrupt source signal is generated which may be selected to trigger an interrupt.

22.1.4.3. DMA

Please refer to section “DMA” for information about operation of the SPI in DMA mode.

22.1.5. Inactivation

Returning a SPI module to standby mode by resetting its respective enable bit (Table 22–1) will immediately terminate any running receive or transmit operation and will reset all internal registers.

22.1.6. Precautions

A single wire bus is easiest implemented by a wired-or configuration of the SPIx-D-OUT output port and the open drain output of the external transmitter:
simply configure the SPIx-D-OUT output port in Port Slow mode, always operate it in Port Special Output mode and connect it directly to the external open drain output. An external pull-up resistor is not necessary in this configuration because the SPIx-D-OUT output port supplies the necessary pull-up drive.
If the SPIx-D-OUT output port has to be operated in Port Fast mode, this simple scheme is not possible, because the pull-down action of the external open drain output may exceed the absolute maximum current rating of the SPIx-D-OUT output port. A discrete external wired-or is recommended for this situation.

During operation, make sure, that the external clock does not start until after SPIxD has been written, otherwise correct data transfer is not be guaranteed.

22.2. Registers

The following registers are available once for SPI0 and SPI1 each.

SPIxD **SPI x Data Register**

	7	6	5	4	3	2	1	0	
r/w	Bit 7 to 0 of Rx/Tx Data								
	0	0	0	0	0	0	0	0	Res

SPIxM **SPI x Mode Register**

	7	6	5	4	3	2	1	0	
r/w	BIT8	LEN9	RXSEL	INTERN	SCLK		CSF		
	0	0	0	0	0	0	0	0	Res

BIT8 **Bit 8 of Rx/Tx Data**
r/w: Rx/Tx data bit.
In 8 bit mode (LEN9 = 0) this bit is undefined when read.

LEN9 **Frame Length 9 Bit Selection**
r/w0: 8 bit mode.
r/w1: 9 bit mode.

RXSEL **Receive Selection**
r/w0: Input active.
r/w1: Low level at input.

INTERN **Internal/External Clock Selection**
r/w0: Use external clock.
r/w1: Use internal clock.

SCLK **Sample Clock**
r/w: Clock polarity and edge of data sampling. (Table 22–2)

Table 22–2: SCLK usage

SCLK		Clock Polarity	Sampling Edge	See Fig.
1	0			
0	0	low	falling	22–3
0	1		rising	22–5
1	0	high	rising	22–2
1	1		falling	22–4

CSF **Clock Selection Field**
wr: Source of internal clock (Table 22–3)

Table 22–3: CSF usage

CSF		Source of internal clock
1	0	
0	0	F0SPI
0	1	F1SPI
1	x	F2SPI

22.3. Timing

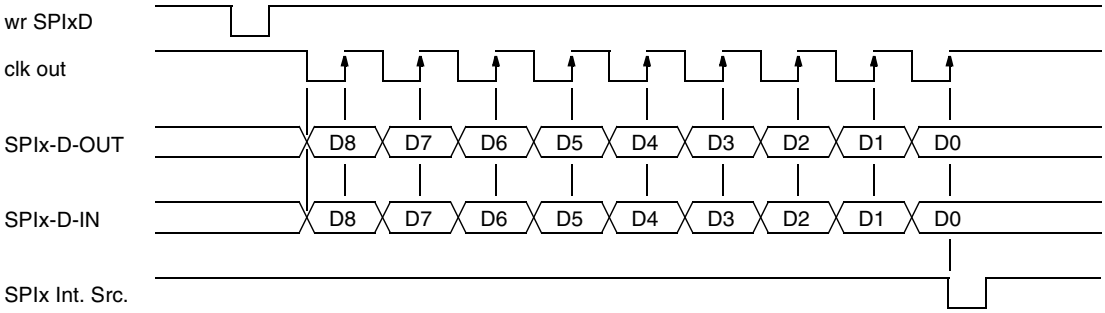


Fig. 22–2: Nine bit frame. Data valid at rising edge. Clock inactive high

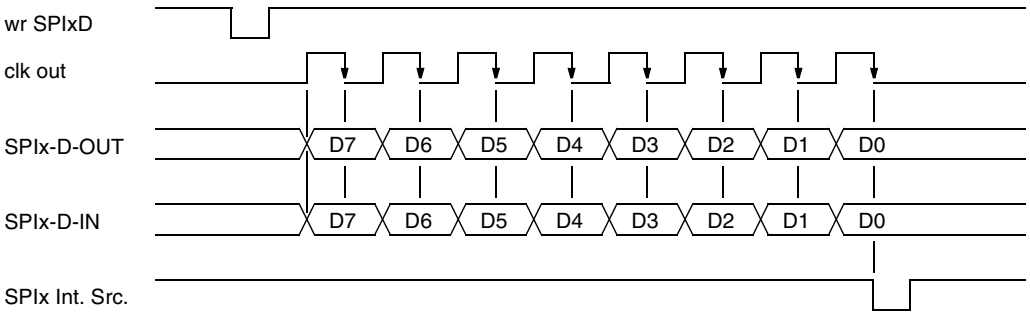


Fig. 22–3: Eight bit frame. Data valid at falling edge. Clock inactive low

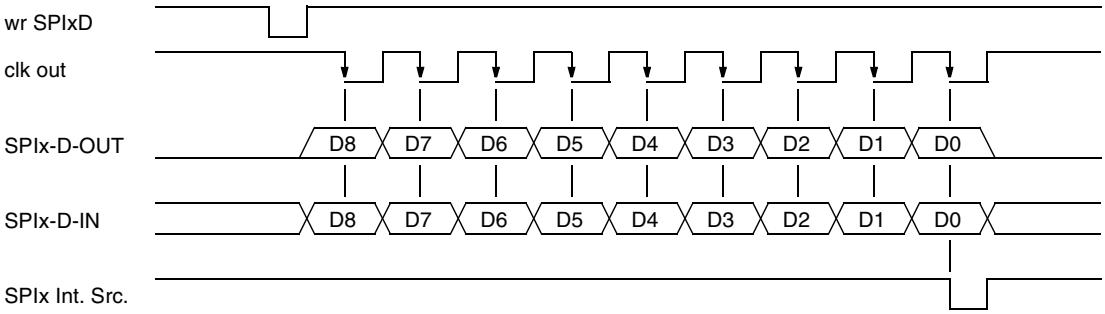


Fig. 22–4: Nine bit frame. Data valid at falling edge. Clock inactive high

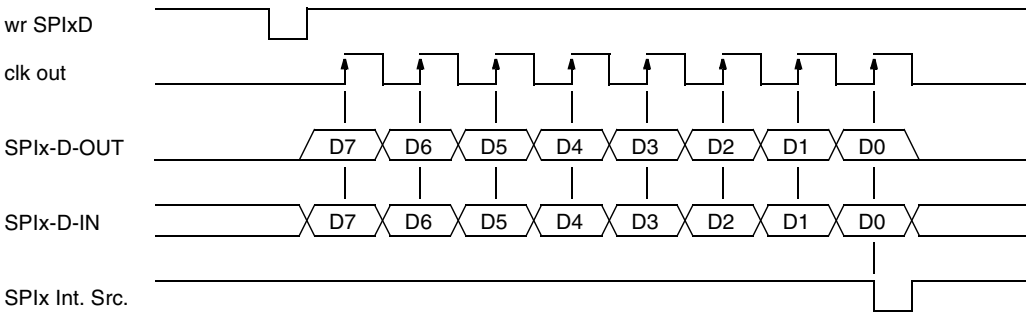


Fig. 22–5: Eight bit frame. Data valid at rising edge. Clock inactive low

23. Universal Asynchronous Receiver Transmitter (UART)

A UART provides a serial Receiver/Transmitter. A 7bit or 8bit telegram can be transferred asynchronously with or without a parity bit and with one or two stop bits. A 13bit baud rate generator allows a wide variety of baud rates. A two word receive FIFO unburdens the SW. Incoming telegrams are compared with a register value. Interrupts can be triggered on transmission complete, reception complete, compare and break.

The number of UARTs implemented is given in Table 23–1. The “x” in register names distinguishes the module number.

Features

- Full duplex.
- 7bit or 8bit frames.
- Parity: None, odd or even.
- One or two stop bits.
- Receive compare register.
- Two word receive FIFO.
- 13bit baud rate generator.

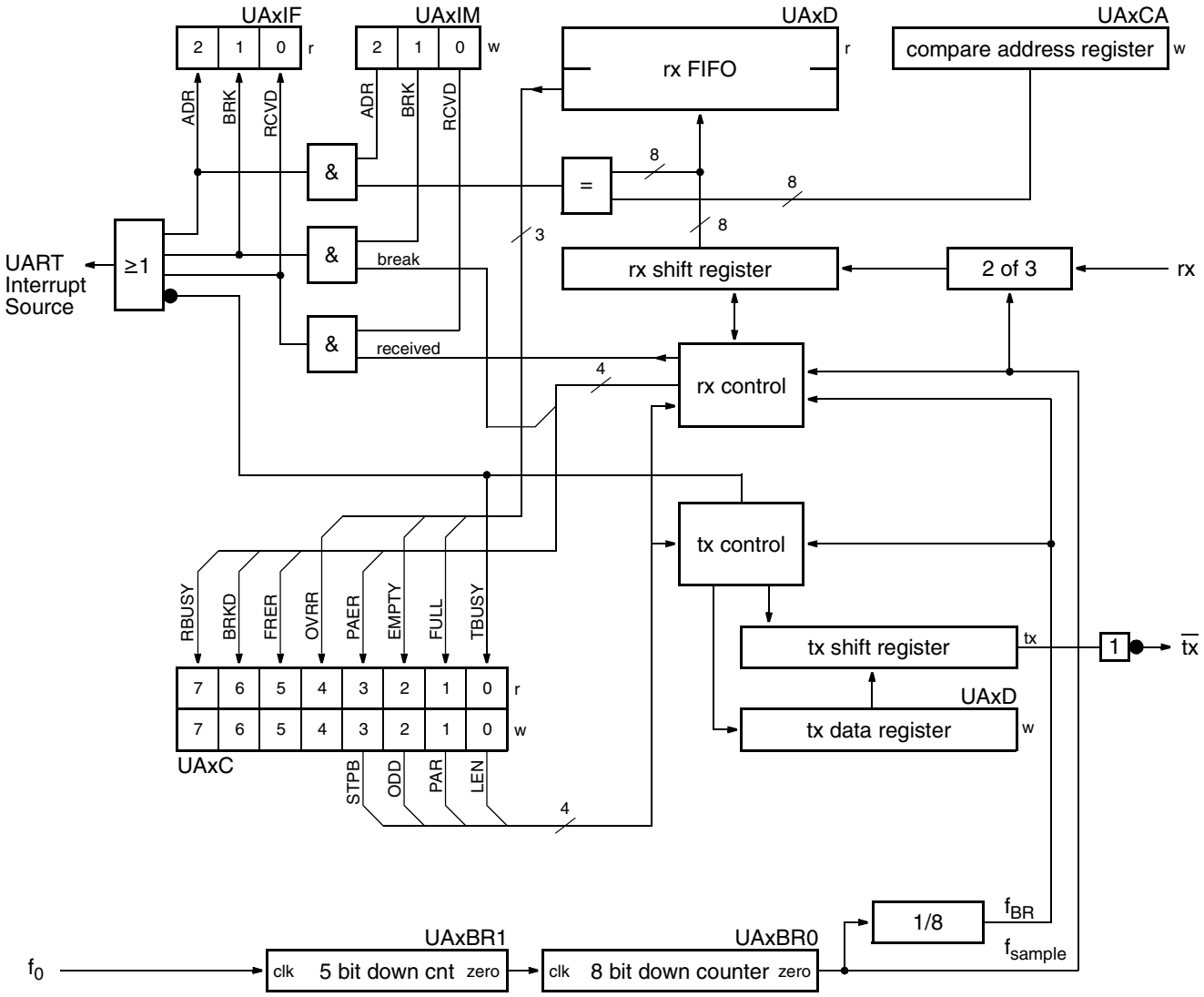


Fig. 23–1: Block Diagram

23.1. Principle of Operation

23.1.1. General

A UART module contains a receive shift register that serves to receive a telegram via its RX input. A FIFO is affixed to it that stores two previously received telegrams.

A transmit shift register serves to transmit a telegram via its TX output.

Other features include a receive compare function, flexible interrupt generation and handling, and a set of control, error and status flags that facilitate management of the UART by SW.

The interrupt source output of this module is routed to the Interrupt Controller logic. But this does not necessarily select it as input to the Interrupt Controller. Check section “Interrupt Controller” for the actually selectable sources and how to select them.

A programmable baud rate generator generates the required bit clock frequency.

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

A UART module is only capable to receive telegrams that differ by no more than ± 2.5% from its own baud rate setting.

23.1.2. Hardware settings

The polarity of most RX and TX connections of the UART is settable by HW Options (See table 23–1 and figure 23–2). Refer to “HW Options” for setting them.

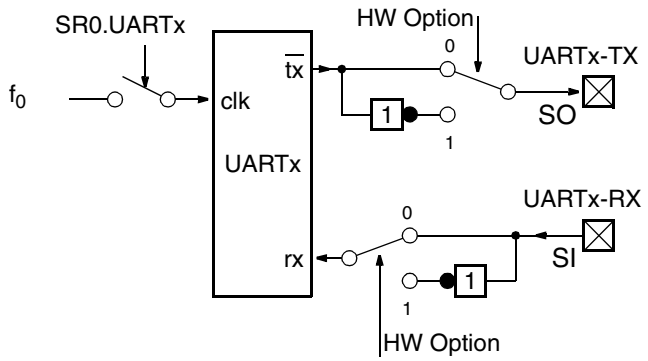


Fig. 23–2: Context Diagram

23.1.3.2. Telegram Format

The format of a telegram is configured in the Control and Status register UAxC. A telegram starts with a start bit followed by the data field. The data field consists of 7 or 8 data bit. There can be a parity bit after the data field. The telegram is finished by one or two stop bits (see Table 23–3 on page 138).

23.1.3. Initialization

After reset, a UART is in standby mode (inactive).

Prior to entering active mode, proper SW configuration of the U-Ports assigned to function as RX input and TX output has to be made (Table 23–1). The RX port has to be configured Special In and the TX port has to be configured Special Out. Refer to “Ports” for details.

For entering active mode of a UART, set the respective enable bit (Table 23–1).

Prior to operation, the desired baud rate, telegram format, compare address and interrupt source configuration have to be made.

23.1.3.1. Baud Rate Generator

The receive and transmit baud rate is internally generated. The Baud Rate registers UAxBR0 (low byte) and UAxBR1 (high byte) serve to enter the desired 13bit setting. Write UAxBR0 first, UAxBR1 last.

The baud rate generator is a 13bit down-counter which is clocked by f_0. It generates the sample frequency:

$$f_{sample} = \frac{f_0}{\text{Value of Baud Rate Registers} + 1}$$

Its output frequency f_{sample} is divided by eight to generate the baud rate (bit/second).

$$BR = \frac{f_0}{(\text{Value of Baud Rate Registers} + 1) \times 8} = \frac{f_{sample}}{8}$$

$$\text{Value of Baud Rate Registers} = \frac{f_0}{BR \times 8} - 1$$

Table 23–1: Module specific settings

Module Name	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
UART0	RX inversion	UA0	UART0-RX input	U2.5 special in	SR0.UART0
	TX inversion		UART0-TX output	U2.4 special out	
UART1	RX inversion	UA1	UART1-RX input	U2.3 special in	SR0.UART1
	TX inversion		UART1-TX output	U2.2 special out	

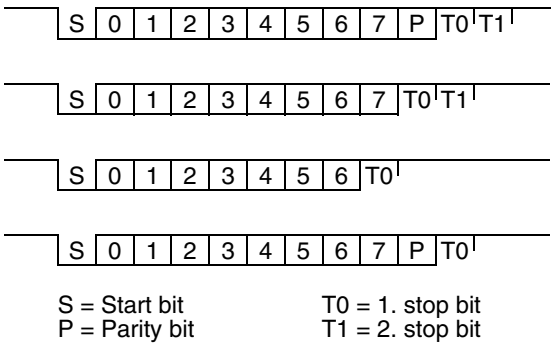


Fig. 23–3: Examples of Telegram Formats

The level of the start bit is always opposite to the neutral level. The level of the stop bits is always the same as the neutral level. If a parity bit is programmed, odd or even parity can be selected.

Table 23–2: Definition of Parity Bit

Parity Flag	Number of Ones	Parity Bit
odd	odd	0
odd	even	1
even	odd	1
even	even	0

As a general rule, the parity bit completes the number of ones in the data field to the selected parity.

23.1.3.3. Compare Address

The content of the Compare Address register UAxCA is compared with each received telegram. On a match, the interrupt flag ADR is set and the interrupt source signal is triggered.

The MSB of register UAxCA must be set to zero if transmission of a seven bit data field is configured in register UAxC.

23.1.3.4. Interrupt

Four signals can trigger the UART interrupt source output. Three of them set their own flags in the Interrupt Flag register UAxIF and can be enabled by setting bits in the Interrupt Mask register UAxIM.

1. When the flag TBUSY in register UAxC is set to zero, the interrupt source output is triggered. This indicates that a transmission is finished and the transmit buffer is empty. There is neither an interrupt flag to indicate this event, nor a mask flag to disable this interrupt.

2. RCVD is generated by the receive control logic at the end of each received telegram even if the FIFO is full. This signal is enabled by setting the corresponding bit in register UAxIM.

3. BRK is generated by the receive control logic each time a break is detected. This signal is enabled by setting the corresponding bit in register UAxIM.

4. ADR is generated by the address comparator. This signal is enabled by setting the corresponding bit in register UAxIM.

BRK and ADR also set flags in the Interrupt Flag register UAxIF when enabled. The first RCVD interrupt, when the FIFO has been empty before, sets a flag in UAxIF too. Even if all interrupts are enabled in register UAxIM, the interrupt source output is triggered only once within a telegram. UAxIF flags remain valid until the end of the next telegram. ADR is not generated and the ADR flag is not set if a frame or parity error was detected in the corresponding telegram.

23.1.4. Operation

With proper HW configuration and SW initialization, a UART module is ready to transmit and receive telegrams in the selected format.

23.1.4.1. Transmit

A write access to UART Data register UAxD immediately loads the transmit shift register and starts transmission with sending the start bit. The flag TBUSY in register UAxD is set.

At the end of transmission the interrupt source signal is triggered and the flag TBUSY is reset.

To avoid data corruption, ensure that flag TBUSY is LOW before writing to UAxD

23.1.4.2. Receive

A first negative edge of a telegram on the RX line of a UART starts a receive cycle and sets the flag RBUSY in UAxC. After reception of the last bit of the telegram, the telegram content, together with its status information, is transferred to the receive FIFO and an interrupt is generated. RBUSY is resetted. Telegram data are available in register UAxD, telegram status in register UAxC.

During reception, the following checks are performed according to the register UAxC setting:

1. A parity error is detected if the parity of the received telegram does not match the programmed parity. The flag PAER in register UAxC is set in this case. Differing telegram length settings in register UAxC and receiver may also cause parity errors.

2. A frame error is detected if the level of start or stop bits violate the transmission rule. The flag FRER in register UAxC is set in this case.

3. A break condition is detected if the receive input remains low for one complete telegram duration. When a break starts during telegram, this condition must extend over another telegram length to be properly detected. This event sets the flag BRKD in register UAxC and can trigger the interrupt source output if enabled. After a break, the receive input must be high for at least 1/4 of the bit length before a new telegram can be received.

Telegrams of an external RS232 interface are correctly received, even if they are transmitted without gaps (the start bit immediately follows the stop bit of the preceding telegram).

23.1.4.3. Receive FIFO

The receive FIFO is able to buffer the data fields of two consecutive telegrams. But not only the data field of a telegram is double buffered, the related information is double buffered too. The flags PAER, FRER and BRKD in register UAxC apply to a certain telegram and are thus double buffered.

The receive FIFO is full if two telegrams were received but the SW did not yet read register UAxD. If there is a third telegram, it is not written to the FIFO and its data are lost. The flags EMPTY, FULL and OVRR show the status of the FIFO. EMPTY indicates that there is no entry in the FIFO. FULL will be set with the second entry in the receive FIFO and indicates that there is no more entry free. OVRR indicates that there was a third telegram which could not be written to the FIFO.

Status flags are readable as long as the corresponding data field was not read from register UAxD. As soon as a FIFO entry is read out, the status flags of this entry are lost. They are overwritten by the flags of the second entry. SW first has to read the flags and then the corresponding FIFO entry.

The flags PAER, FRER and BRKD apply to a certain telegram and are only valid if there is at least one entry in the FIFO (EMPTY = 0). The flags EMPTY, FULL and OVRR apply to the FIFO and are valid all the time.

23.1.5. Inactivation

Returning a UART module to standby mode by resetting its respective enable bit (Table 23–1) will immediately terminate any running receive or transmit operation and will reset all internal registers.

23.2. Timing

The duration of a telegram results from the total telegram length in bits (L_{TG}) (see Table 23–3 on page 138) and the baud rate (BR).

$$t_{TG} = \frac{L_{TG}}{BR}$$

The incoming signal is sampled with the sample frequency and filtered by a 2 of 3 majority filter. A falling edge at the output of the majority filter starts the receive timing frame for the telegram. An individual bit is sampled with the fifth sample clock pulse within that timing frame (cf. Fig. 23–4 and 23–5). If a bit was the last bit of its telegram, reception of a new telegram can start immediately after this sample. With a receive telegram, interrupt source is triggered and flags are set just after the sample of the last stop bit. With a transmit telegram, interrupt source is triggered and BUSY reset after the nominal end of the last stop bit.

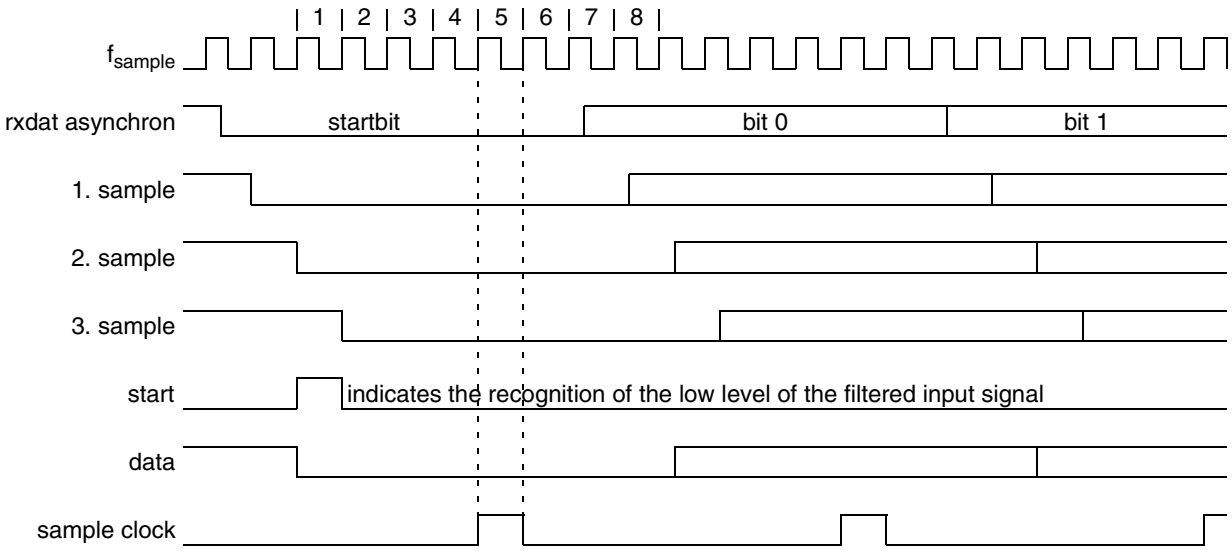


Fig. 23–4: Start of Telegram

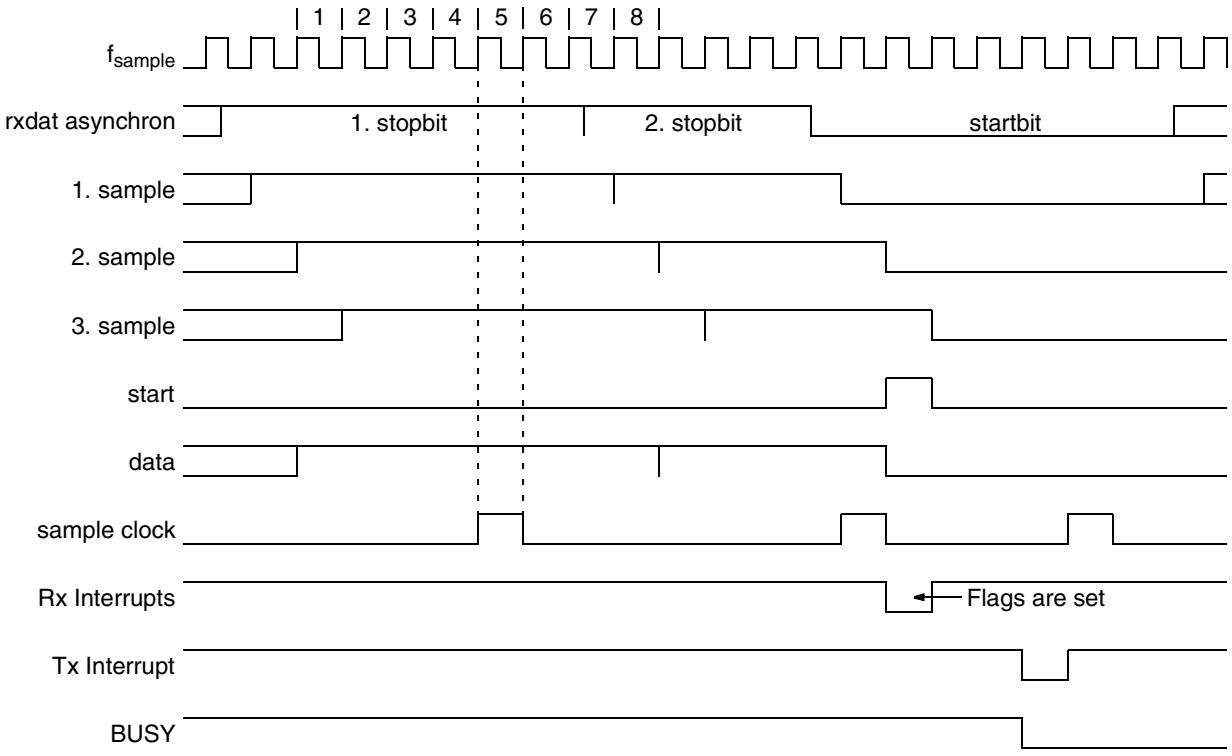


Fig. 23–5: End of Telegram

23.3. Registers

UAxD UART x Data Register

	7	6	5	4	3	2	1	0	
r	Receive register								
w	Transmit register								
	x	x	x	x	x	x	x	x	Res

UAxC UART x Control and Status Register

	7	6	5	4	3	2	1	0	
r	RBUSY	BRKD	FRER	OVRR	PAER	EMPTY	FULL	TBUSY	
	0	x	x	0	x	1	0	0	Res
w	x	x	x	x	STPB	ODD	PAR	LEN	
	x	x	x	x	0	0	0	0	Res

RBUSY Receiver Busy
r0: Not busy.
r1: Busy.

BRKD Break Detected
r0: No break.
r1: Break.

FRER Frame Error Detected
r0: No error.
r1: Error.

OVRR Overrun Detected
r0: No overrun.
r1: Overrun.

PAER Parity Error Detected
r0: No error.
r1: Error.

EMPTY Rx FIFO Empty
r0: Not empty.
r1: Empty.
There is at least one entry present if EMPTY is zero. PAER, FRER and BRKD are not valid if EMPTY is set.

FULL Rx FIFO Full
r0: Not full.
r1: Full.

TBUSY Transmitter Busy
r0: Not busy.
r1: Busy.
Do not write to register UAxD as long as BUSY is true.

STPB Stop Bits
w0: One stop bit.
w1: Two stop bits.

ODD Odd Parity
w0: Even parity.
w1: Odd parity.

PAR Parity On
w0: No parity.
w1: Parity on.

LEN Length of Frame
w0: 7bit frame.
w1: 8bit frame.

Table 23–3: Telegram Format and Length

LEN	PAR	STPB	Format	L_{TG}
0	0	0	S, 7D, T0	9
0	0	1	S, 7D, T0, T1	10
0	1	0	S, 7D, P, T0	10
0	1	1	S, 7D, P, T0, T1	11
1	0	0	S, 8D, T0	10
1	0	1	S, 8D, T0, T1	11
1	1	0	S, 8D, P, T0	11
1	1	1	S, 8D, P, T0, T1	12

UAxBR0 UART x Baud Rate Register low byte

	7	6	5	4	3	2	1	0	
w	Bit 7 to 0 of Baud Rate								
	0	0	0	0	0	0	0	0	Res

UAxBR1 UART x Baud Rate Register high byte

	7	6	5	4	3	2	1	0	
w	x	x	x	Bit 12 to 8 of Baud Rate					
	-	-	-	0	0	0	0	0	Res

The Baud Rate Registers UAxBR0 and UAxBR1 have to be written low byte first to avoid inconsistencies. UAxBR0 is the low byte.

Valid entries in the Baud Rate Registers range from 1 to 8191. Don't operate the baud rate generator with its reset value zero.

UAxCA UART x Compare Address Register

	7	6	5	4	3	2	1	0	
w	Bit 7 to 0 of address								
	0	0	0	0	0	0	0	0	Res

UAxIM UART x Interrupt Mask Register

	7	6	5	4	3	2	1	0	
w	x	x	x	x	x	ADR	BRK	RCVD	
	-	-	-	-	-	0	0	0	Res

ADR **Mask Compare Address Detected**
w0: Disable interrupt.
w1: Enable interrupt.

BRK **Mask Break Detected**
w0: Disable interrupt.
w1: Enable interrupt.

RCVD **Mask Received a Telegram**
w0: Disable interrupt.
w1: Enable interrupt.

UAxIF UART x Interrupt Flag Register

	7	6	5	4	3	2	1	0	
r	Test	Test	Test	Test	Test	ADR	BRK	RCVD	
	-	-	-	-	-	x	0	0	Res

Test **Reserved for test (do not use)**

ADR **Compare Address Detected**
r0: No Interrupt.
r1: Interrupt pending.

BRK **Break Detected**
r0: No Interrupt.
r1: Interrupt pending.

RCVD **Received a Telegram**
r0: No Interrupt.
r1: Interrupt pending.

24. I²C-Bus Master Interface

The IC contains two independent I²C-bus Master Interface units (I²C), 0 and 1. They are pure master systems, multi master busses are not realizable. The units contain read and write buffers with interrupt logic which makes automatic and software independent operation possible for most types of I²C telegrams. Because of the internal clock pre-scaler, telegram clock rate does not depend on system clock rate.

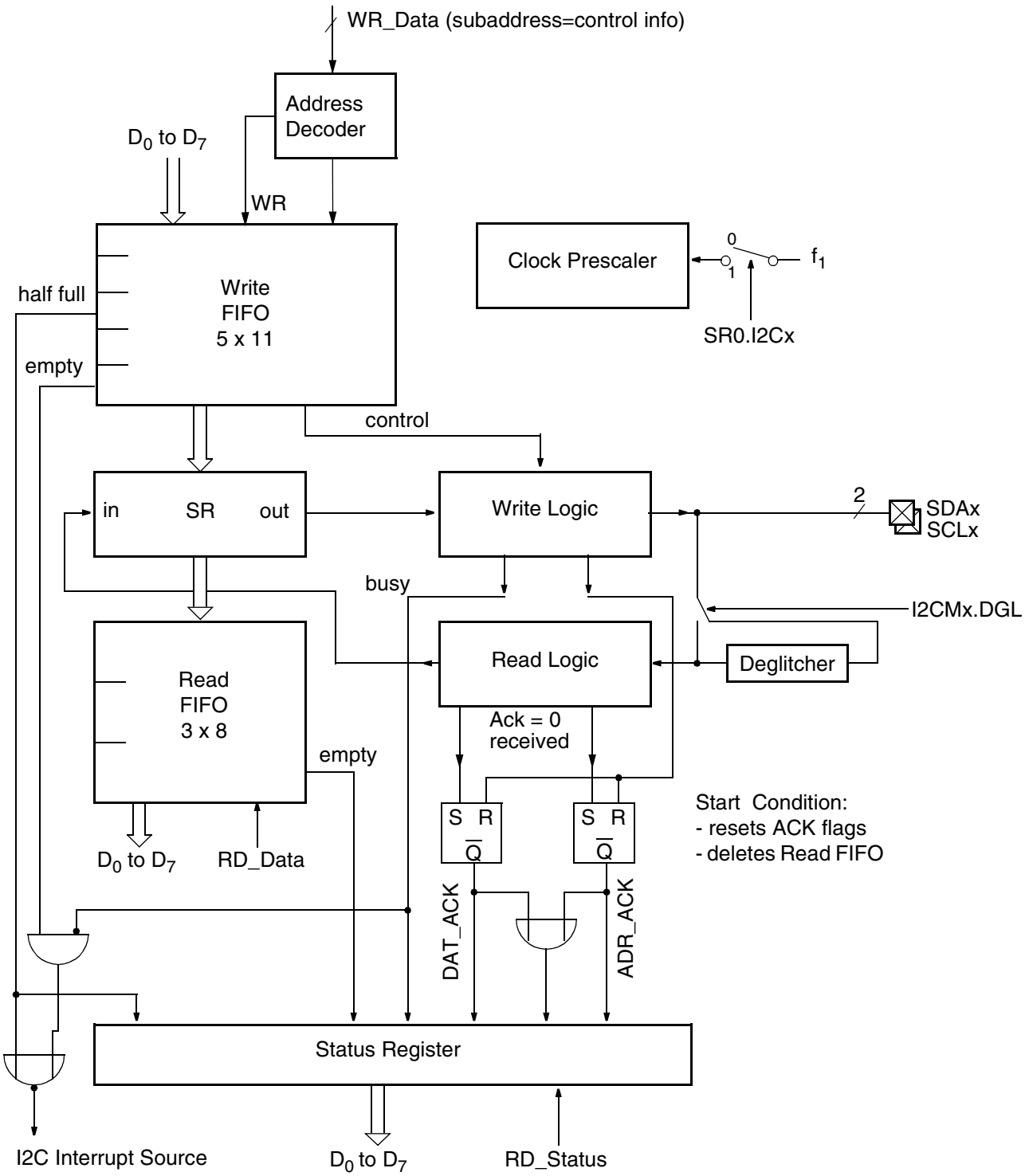


Fig. 24–1: Block diagram of I²C-Bus Master Interface

24.1. Principle of Operation

24.1.1. General

24.1.2. Hardware Settings

Since the telegram clock rate is register programable there is no HW option for the I²C-Bus Master Interface.

24.1.3. Initialization

After system reset the I²C is in standby mode, i.e. the block internal clock is halted and all registers are set to their reset value. By default, the input deglitcher is on, limiting the obtainable bit rate to 208.3kbit/s (see Table 24–2).

In standby mode the clock is halted. Programming of the I²C registers is possible and the Write-FIFO can be filled.

Prior to operation, proper SW configuration of the U-Ports assigned to function as I²C Double Pull-down port has to be made. See table 24–1 and section "Ports" for details.

Table 24–1: Module specific settings

Module Name	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
I2C0	U2.0 CAN0/SCL0 output multiplexer	PM.U20	SCL0	U2.0 special out, double pull-down mode	SR0.I2C0
	U2.1 CAN0/SDA0 output multiplexer		SDA0	U2.1 special out, double pull-down mode	
I2C1			SCL1	U5.1 special out, double pull-down mode	SR0.I2C1
			SDA1	U5.2 special out, double pull-down mode	

The bit rate and the desired input deglitcher configuration has to be set up in register I2CMx in order to get into an active and useful mode. All other registers serve I²C data I/O purposes.

24.1.4. Operation

A complete telegram is assembled by the software out of individual sections. Each section contains 8-bit data. This data is written into one of the six possible write registers. Depending on the chosen address, a certain part of an I²C-bus cycle is generated: start, data, stop, with or without acknowledge. By means of corresponding calling sequences it is therefore possible to join even very long telegrams (e.g. long data files for auto increment addressing of I²C slaves).

The software interface contains a 5 word deep Write-FIFO for the control-data registers as well as a 3 word deep Read-FIFO for the received data. Thus most of the I²C telegrams can be transmitted to the hardware without the software having to wait for empty space in the FIFO.

An interrupt is generated on two conditions:

- The Write-FIFO was filled with 5 entries and reaches the ‘half full’ state.
- The Write-FIFO is empty and stop condition is completed.

There is no ‘Write-FIFO half full’ interrupt unless the Write-FIFO was previously filled completely.

All address and data fields appearing on the bus are constantly monitored and written into the Read-FIFO. The software can then check these data in comparison with the scheduled data.

Every reception of a start or restart condition immediately empties the Read-FIFO. The Read-FIFO stops if it is full. It’s not overwritten, further received data are lost.

If a read instruction is handled, the interface must send the data word 0xFF so that the responding slave can insert its data. In this case the Read-FIFO contains the read-in data.

If telegrams longer than 3 bytes (1 address, 2 data bytes) are received, the software must check the filling condition of the Write-FIFO and, if necessary, fill it up and read out the Read-FIFO. A variety of status flags is available for this purpose:

- The ‘half full’ flag I2CRSx.WFH is set if the Write-FIFO is filled with exactly three bytes.
- The ‘empty’ flag I2CRSx.RFE is set if there is no more data available in the Read-FIFO.
- The ‘busy’ flag I2CRSx.BUSY is activated by writing any byte to any one of the Write registers. It stays active until the I²C-bus activities are stopped after the stop condition generation.

Moreover the ACK-bit is recorded separately on the bus lines for the address and the data fields. However, the interface itself can set the address ACK=0. In any case the two ACK flags show the actual bus condition. These flags will be reset with the next I²C start condition.

There is one data acknowledge (DACK) flag available. It indicates the level of the last received ACK bit. It will be cleared to zero with the reception of a zero and it will be set to one with the reception of a one within the acknowledge field of a data byte. Thus, after the stop condition, it indicates whether the last of the data bytes was acknowledged or not.

The bus activity starts immediately after the first write to the Write-FIFO. The transmission can be synchronized by an artificial extension of the low phase of the clock line. Transmission is not continued until the state of the clock line is high once again. Thus an I²C slave device can adjust the transmission rate to its own abilities.

The figures 24–2, 24–3 and 24–4 show the basic principle of I2C telegram transmission as a quick reference. Refer to the official I²C documentation for more details.

24.1.4.1. Example of Operation

The software has to work in the following sequence (ACK=1) to read a 16-bit word from an I²C device address 0x10 (on condition that the bus is not active):

-write 0x21 to	I2CWS0x
-write 0xFF to	I2CWD0x
-write 0xFF to	I2CWP1x
-read RFE bit from	I2CRSx
-read dev. address from	I2CRDx
-read RFE bit from	I2CRSx
-read 1st databyte from	I2CRDx
-read RFE bit from	I2CRSx
-read 2nd databyte from	I2CRDx

The value 0x21 in the first step results from the device address in the 7 MSBs and the R/W-bit (read=1) in the LSB. If the telegrams are longer, the software has to ensure that neither the Write-FIFO nor the Read-FIFO can overflow.

To write data to this device:

-write 0x20 to	I2CWS0x
-write 1st databyte to	I2CWD0x
-write 2nd databyte to	I2CWP0x

24.1.5. Inactivation

Since the described block is an I²C master, all I²C bus activity stops if the end of a telegram is reached. I²C slaves cannot start any bus activity on their own. However, the block internal clock is always running at full speed of I²C clock (4 or 5 MHz), independent of the bit rate divider setting. The standby mode is therefore intended for the lowest possible power consumption.

Make sure to switch off the module only if it is not active. Switching off during transmission of a telegram may cause an output to stay at low level. Hence lowest possible power consumption can't be achieved because SDA and SCL use open drain output ports.

24.1.6. Precautions

For the effect of CPU clock modes on the operation of this module refer to section "CPU and Clock System" (see Table 4–1 on page 36).

Note: The I²C block uses U-Ports as connection to the outside world. This implies that neither logic output low level switching specs nor logic input value specs of the official I²C specification document are literally met. Refer to section "Ports" for the actual spec values of this implementation.

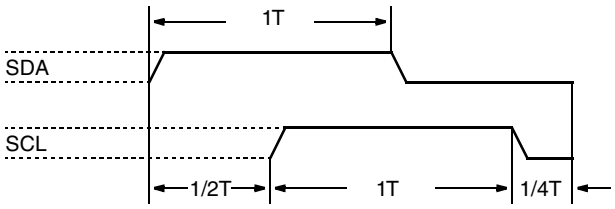


Fig. 24–2: Start or Restart Condition I²C-Bus

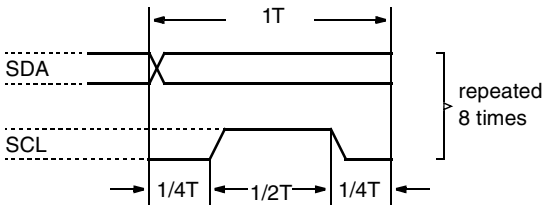


Fig. 24–3: Single Bit on I²C-Bus

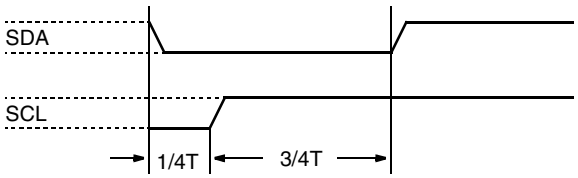
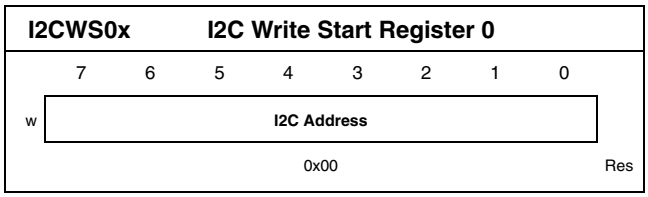
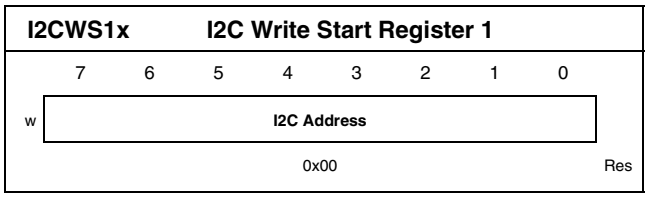


Fig. 24–4: Stop Condition I²C-Bus

24.2. Registers



Writing this register moves I2C start condition, I2C Address and ACK=1 into the Write FIFO.



Writing this register moves I2C start condition, I2C Address and ACK=0 into the Write FIFO.

I2CWD0x	I2C Write Data Register 0							
	7	6	5	4	3	2	1	0
w	I2C Data							
	0x00							Res

Writing this register moves I2C Data and ACK=1 into the Write FIFO.

I2CWD1x	I2C Write Data Register 1							
	7	6	5	4	3	2	1	0
w	I2C Data							
	0x00							Res

Writing this register moves I2C Data and ACK=0 into the Write FIFO.

I2CWP0x	I2C Write Stop Register 0							
	7	6	5	4	3	2	1	0
w	I2C Data							
	0x00							Res

Writing this register moves I2C Data, ACK=1 and I2C stop condition into the Write FIFO.

I2CWP1x	I2C Write Stop Register 1							
	7	6	5	4	3	2	1	0
w	I2C Data							
	0x00							Res

Writing this register moves I2C Data, ACK=0 and I2C stop condition into the Write FIFO.

I2CRDx	I2C Read Data Register							
	7	6	5	4	3	2	1	0
r	I2C Data							
	0x00							Res

Reading this register returns the content of the Read FIFO.

I2CRSx	I2C Read Status Register							
	7	6	5	4	3	2	1	0
r	x	OACK	AACK	DACK	BUSY	WFH	RFE	x
	0	0	0	0	0	0	0	0 Res

OACK **"OR"ed Acknowledge**
r: AACK OR DACK.

AACK **Address Acknowledge**
r1: Not acknowledged (received a one)
r0: Acknowledged (received a zero)

DACK **Data Acknowledge**
r1: Not acknowledged (received a one)
r0: Acknowledged (received a zero)

BUSY **Busy**
r1: I^2C Master Interface is busy.
r0: I^2C Master Interface is not busy.

WFH **Write-FIFO Half Full**
r1: Write-FIFO contains exactly 3 bytes.
r0: Write-FIFO contains more or less than 3 bytes.

RFE **Read-FIFO Empty**
r1: Read-FIFO is empty.
r0: Read-FIFO is not empty.

I2CMx	I2C Mode Register							
	7	6	5	4	3	2	1	0
w	DGL	SPEED						
	1	0x02						Res

DGL **Input Deglitcher**
w1: Deglitcher is active.
w0: Deglitcher is bypassed.
If the deglitcher is active, the maximum bit rate is limited. SPEED must be programmed to 6 at least. The maximum bit rate may be further reduced by the bus load.

SPEED **Speed Select** (Table 24–2)
w: I^2C Bit Rate = f_1 / (4 * SPEED).

Table 24–2: SPEED Usage: I2C Bit Rates

SPEED	f_1 Division by	Bit Rate @ f_1=5MHz	Bit Rate @ f_1=4MHz
0	128*4 (!)	**9.8 kbit/s**	**7.8 kbit/s**
1 [1)]	1*4	**1.25 Mbit/s**	**1.00 Mbit/s**
2 [1)]	2*4	**625 kbit/s**	**500 kbit/s**
3 [1)]	3*4	**416.7 kbit/s**	**333.3 kbit/s**
4 [1)]	4*4	**312.5 kbit/s**	**250 kbit/s**
5 [1)]	5*4	**250 kbit/s**	**200 kbit/s**
6	6*4	**208.3 kbit/s**	**166.7 kbit/s**
7	7*4	**178.6 kbit/s**	**142.9 kbit/s**
...		**...**	
127	127*4	**9.8 kbit/s**	**7.9 kbit/s**

1) These bit rates may only be set with a bypassed input deglitcher (I2CMx.DGL=0)

25. CAN Manual

This manual describes the user interface of the CAN module. For further information about the CAN bus, please refer to the CAN specification 2.0B from Bosch.

Features

- Bus controller according to CAN Licence Specification 1992 2.0B
- Supports standard and extended telegrams
- FullCAN: up to 32 Rx and Tx telegrams
- Variable number of receive buffers
- Programmable acceptance filter
  Single, group or all telegrams received.
- Time stamp for each telegram
- Overwrite mode programmable for each telegram
- Programmable baud rate. Max. 1 MBd @ 8 MHz
- Sleep mode

The CAN interface is a VLSI module which enables coupling to a serial bus in compliance with CAN specification 2.0B. It controls the receiving and sending of telegrams, searches for Tx telegrams and interrupts and carries out acceptance filtering. It supports transmission of telegrams with standard (11 bit) and extended (29 bit) addresses.

The CAN interface can be configured as BasicCAN or FullCAN. It enables several active receive and transmit telegrams and supports the remote transmission request. The number of telegrams which can be handled depends mainly on the size of the communication RAM (16 byte per telegram), the system clock and the transmission speed. A maximum of 254 telegrams can be handled.

A mask register makes it possible to receive different groups of telegram addresses with different receive telegrams. Transmitting or receiving of a telegram as well as the occurrence of an error can trigger an interrupt.

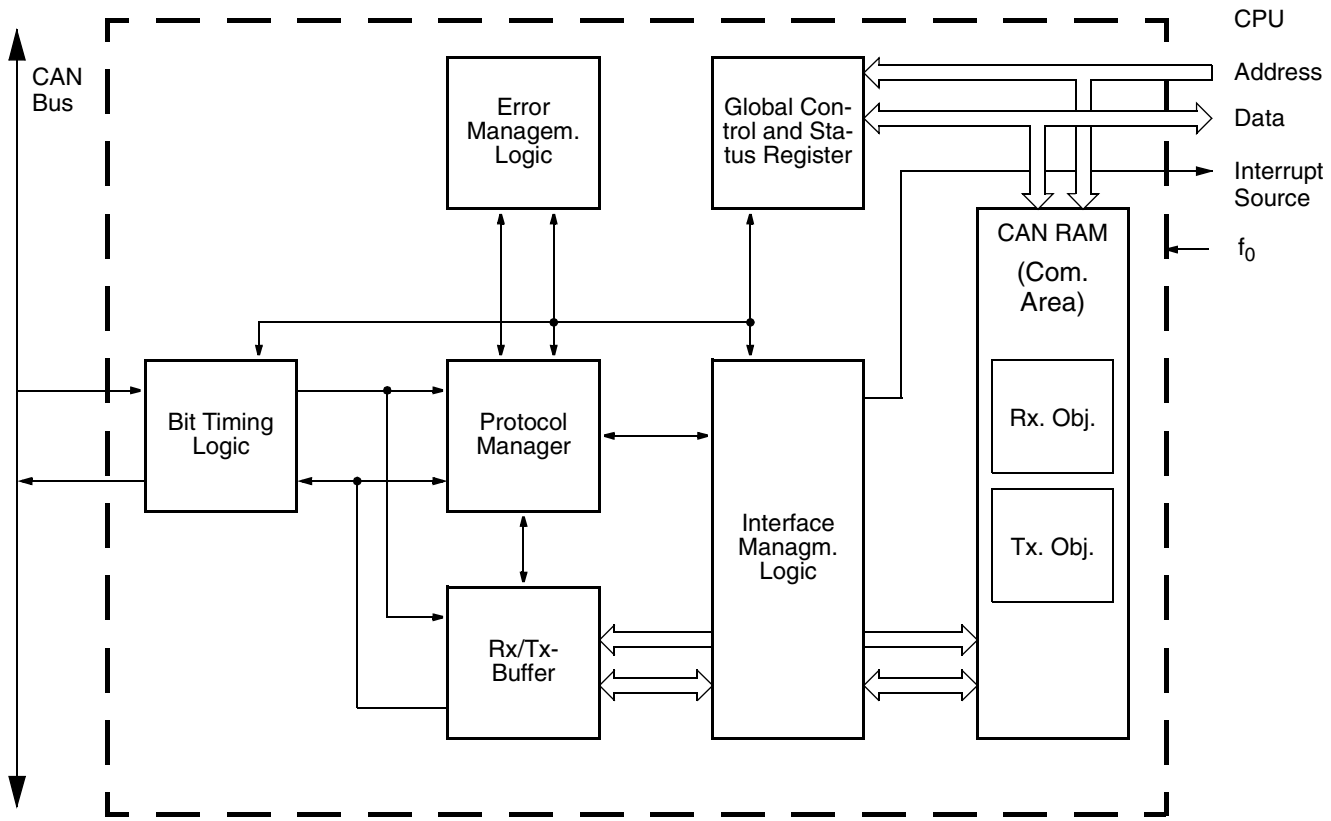


Fig. 25–1: Block diagram of the CAN bus interface

25.1. Abbreviations

BI	CAN Bus Interface
BTL	Bit Timing Logic
CAN	Controller Area Network
CA	Communication Area
CO	Communication Object
CM	Communication Mode
CRC	Cyclic Redundancy Code
DLC	Data Length Code
EoCA	End of CA
Ext. ID	Extended Identifier
Ext. Tg	Extended Telegram
GCS	Global Control and Status Register
ID	Identifier
IML	Interface Management Logic
Rx. Obj.	Receive Object
RxTg	Receive Telegram
Std. ID	Standard Identifier
Std. Tg	Standard Telegram
TD	Telegram Descriptor
Tg	Telegram
TQ	Time Quantum
Tx. Obj.	Transmit Object
TxTg	Transmit Telegram

25.2. Functional Description

25.2.1. HW Description

The CAN bus interface consists of the following components:

Bit Timing Logic: Scans the bus and synchronizes the CAN bus controller to the bus signal.

Protocol Manager: The PM monitors or generates the composition of a telegram and performs the arbitration, the CRC and the bit stuffing. It controls the data flow between Rx/Tx buffer and CAN bus. It also drives the Error Management Logic.

Error Management Logic: Adds up the error messages received from the protocol manager and generates error messages when particular values are exceeded. Guarantees the error limitation as per the CAN Spec. V2.0B.

Interface Management Logic: The IML scans the Communication Area (CA) in the CAN-RAM for transmit telegrams. As soon as it finds one, it enters it into the Rx/Tx buffer and reports it to the protocol manager as ready for transmission. If a telegram is received, the IML carries out the acceptance filtering, i.e. scans the CA, taking into account the Identifier Mask Register in the GCS, for a Tg with the appropriate address. After correct reception, it copies the Tg from the Rx/Tx buffer to the CA. The IML also reports to the CPU the valid transfer of a telegram or given errors per interrupt.

The interrupt source output of this module is routed to the Interrupt Controller logic. But this does not necessarily select it as input to the Interrupt Controller. Check section “Interrupt Controller” for the actually selectable sources and how to select them.

Rx/Tx buffer: This is used to buffer a full telegram (ID, DLC, data) during sending and receiving.

Global Control and Status Register: The GCS contains registers for the configuration of the BI. It also contains error and status flags and an identifier mask. The Error Counter and the Capture Timer can be read from the GCS.

Receive Object: The BI enters received telegrams into a matching Rx-Object. It can be retrieved from the application.

Transmit Object: The application enters data into the Tx-Object and reports it ready for transmission. The BI sends the telegram as soon as the bus traffic allows.

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

25.2.2. Memory Map

From the CAN bus interface the user sees two storage areas in the user RAM area. The BI is configured with the Global Control and Status Registers (GCS). It also indicates the status here. The communication area (CA) contains the Rx and Tx telegrams.

The communication area lies in the CAN-RAM. The end of the Com. Area is fixed by the first control byte of an object whose 3 MSBs contain only ones (Communication Mode = 7 = EoCA). The area after this is available to the user.

The CA consists of communication objects (COs). A CO consists of 6 bytes telegram descriptor (TD), 8 data bytes and the Time Stamp which is 2 bytes long. The TD contains the address (ID) and the length of a telegram (DLC) as well as control bits which are needed for access to the CO and for the transmission of a telegram.

In the BasicCAN and the FullCAN versions, all the communication objects have the same, maximum size of 16 byte. Unassigned storage locations in the data area of a CO can be freely used.

The maximum number of COs is limited by the time which the CAN interface has to search for an identifier in the Com. Area.

25.2.3. Global Control and Status Registers (GCS)

The GCS registers can be used to determine the behavior of the CAN interface. As well as flags for the interrupts, halt and sleep modes, they also contain interrupt index, ID mask, bus timing, error status, output control registers, baud rate prescalers, Tx and Rx error counters as well as the capture timer.

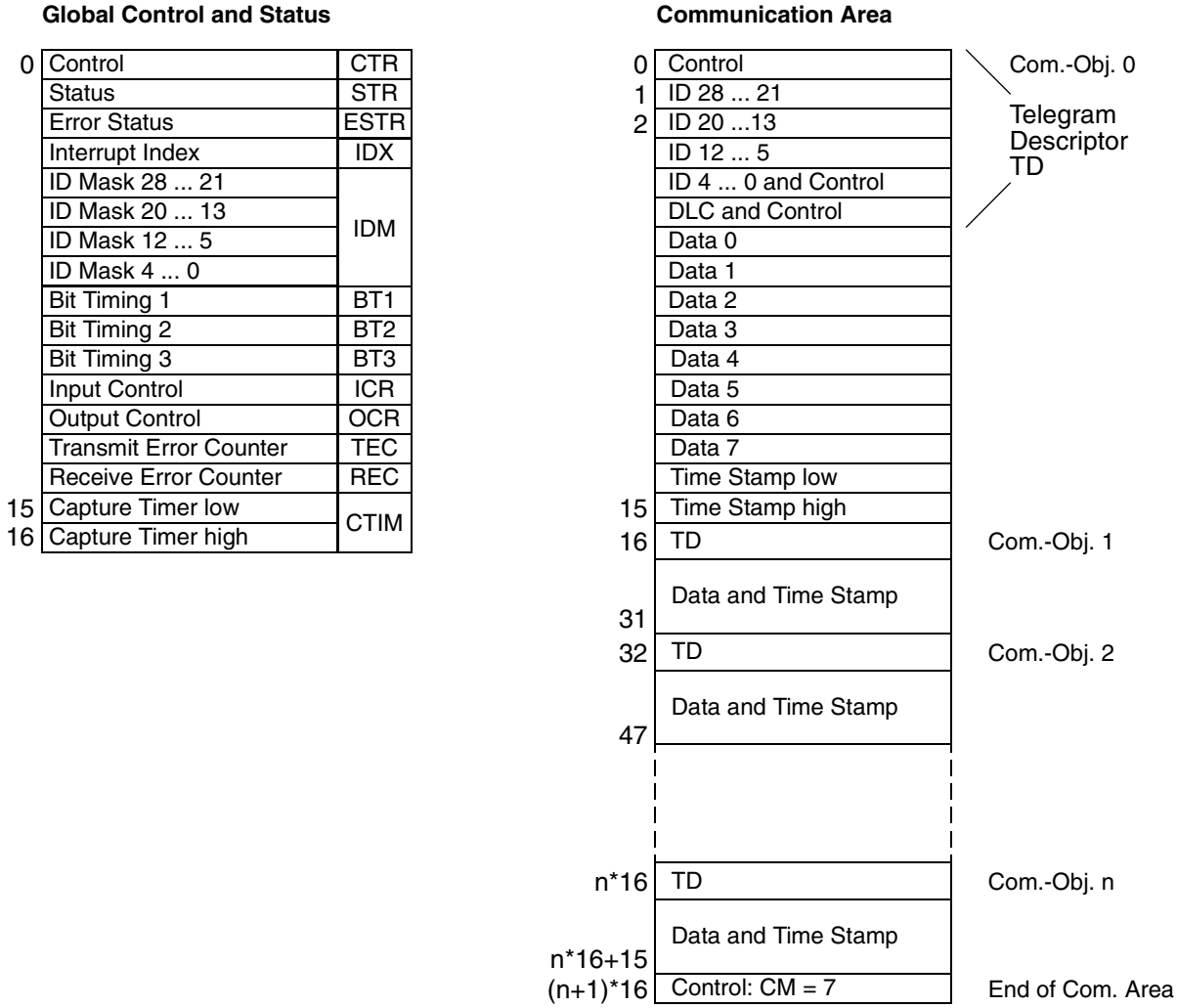


Fig. 25–2: Memory allocation

Access modes:
r: read
w: write
i: init (BI halted)
w0: clear
w1: set

CANxCTR Control Register

	7	6	5	4	3	2	1	0	
r/w	HLT	SLP	GRSC	EIE	GRIE	GTIE	rsvd	rsvd	
	1	0	0	0	0	0	x	x	Res

HLT **Halt**
r/w0: Run.
r/w1: Halt.

Puts the CAN interface in the halt mode. Transmissions which have been started are brought to an end. The halt acknowledge is indicated in the status register (HACK). Re-initialization can be carried out in the halt mode (HACK is set). After this, the halt flag must be deleted again. After a reset, HLT is set.

If HLT is set during a Tx-Tg and this has to be repeated (error or no acknowledge), the BI stops yet. The corresponding TxCO is still reserved, however, and can no longer be operated from BI. Therefore, when HLT is set, the CA should always be re-initialized if the last Tx-Tg has not been correctly transmitted (Status Transfer Flag is still deleted).

If HLT is set during the BI is in Bus-Off mode, the BI stops after Bus-Off mode is finished. Flag BOFF is cleared then and receive and transmit error counters are reset to zero.

SLP **Sleep**
r/w0: Run.
r/w1: Sleep.
The BI goes into the sleep mode when the sleep flag is set and a started Tg is terminated. The sleep mode is finished as soon as a dominant bus level is detected, or the sleep flag is deleted.

GRSC **Global Rescan**
r0: Don't rescan.
r/w1: Rescan.
The microprocessor can set this flag in order to initiate a transmit telegram search at the beginning of the Com. Area. The BI resets the bit. The BI also sets the GRSC flag if the flag RSC has been set in a telegram descriptor of a Tx-Tg just operated, and thereby initiates a rescan. If the microprocessor writes a zero, nothing happens.

EIE **Error-Interrupt-Enable**
r/w0: Disabled.
r/w1: Enabled.

GRIE **Global Rx-Interrupt-Enable**
r/w0: Disabled.
r/w1: Enabled.

GTIE **Global Tx-Interrupt-Enable**
r/w0: Disabled.
r/w1: Enabled.

CANxSTR Status Register

	7	6	5	4	3	2	1	0	
r	HACK	BOFF	EPAS	ERS	rsvd	rsvd	rsvd	rsvd	
	1	0	0	0	x	x	x	x	Res

HACK **Halt-Acknowledge**
r0: Running.
r1: Halted.
Is set by the BI when it enters the halt mode. It is deleted again when the halt mode is exited.

BOFF **Bus-Off**
r0: Bus active.
r1: Bus off.
With this flag the BI indicates whether the node is still actively participating in the bus. If the transmit error counter reaches a value of > 255 (overflow), the node is separated from the bus and the flag is set.

EPAS **Error-Passive**
r0: Error active.
r1: Error passive.
With this flag the BI indicates whether the node is still participating in the bus with active Error Frames. If an error counter has reached a value > 127, the node only transmits passive error frames and the flag is set.

ERS **Error-Status**
r0: No Errors.
r1: Errors.
This flag is set when the BI detects an error. It is set even if an error counter is greater than 96. It means that a bit has been set in the error status register. As soon as all the flags in the error status register are deleted, ERS is also deleted.

As long as a bit is set in the CANxESTR, the ERS bit is also set in the status register. If EIE has been set in the control register, an interrupt is triggered too; i.e. the value 254 is entered in the register CANxIDX as soon as it is free, and the interrupt source output is triggered.

To erase a bit in the CANxESTR the user must write a one at the appropriate place. Places at which he writes a zero will not be changed. Because it makes sense to erase only those bits which have previously been read, only the byte which has been read has to be re-written.

CANxESTR Error Status Register

	7	6	5	4	3	2	1	0	
r/w	GDM	CTOV	ECNT	BIT	STF	CRC	FRM	ACK	
	0	0	0	0	0	0	0	0	Res

Read-Modify-Write operations on single flags of this register must be avoided. Unwanted clearing of other flags of this register may be the result otherwise.

GDM **Good Morning**
r0: No wake-up.
r1: Wake-up.
w0: Unaffected.
w1: Clear.
Is set by the BI when it is aroused from the sleep mode by a dominant bus level. The user must delete it.

CTOV **Capture Time Overflow**
r0: No overflow.
r1: Overflow.
w0: Unaffected.
w1: Clear.
Is set by the BI when the capture timer (CTIM) overflows. The user must delete it.

ECNT **Error Counter Level**
r0: No error counter.
r1: Error counter.
w0: Unaffected.
w1: Clear.
Is set by the BI as soon as the transmit error counter or the receive error counter exceeds a limit value. The user must delete it.

BIT **Bit Error**
r0: No bit error.
r1: Bit error.
w0: Unaffected.
w1: Clear.
Is set by the BI when a transmitted bit is not the same as the bit received. The user must delete the flag.

STF **Stuff Error**
r0: No stuff error.
r1: Stuff error.
w0: Unaffected.
w1: Clear.
Is set by the BI when 6 identical bits are received successively in one Tg. The user must delete it.

CRC **CRC Error**
r0: No stuff error.
r1: Stuff error.
w0: Unaffected.
w1: Clear.
Is set by the BI when the CRC received does not coincide with the CRC calculated. The user must delete it.

FRM **Form Error**
r0: No form error.

r1: Form error.
w0: Unaffected.
w1: Clear.
Is set by the BI when an incorrect bit is received in a field with specified bit level (start of frame, end of frame, ...). The user must delete it.

ACK **Acknowledge Error**
r0: No acknowledge error.
r1: Acknowledge error.
w0: Unaffected.
w1: Clear.
Is set by the BI when there is no acknowledge for a transmitted Tg. The user must delete it.

CANxIDX Interrupt Index Register

	7	6	5	4	3	2	1	0	
r/w	Interrupt Index								
	1	1	1	1	1	1	1	1	Res

The interrupt index indicates the source of the interrupt. If a transmission has been the cause of an interrupt, the interrupt index points to the corresponding telegram descriptor (CANxIDX = 0..253). If an error has been responsible for the interrupt, the interrupt index designates the error status register (CANxIDX = 254). After dealing with the interrupt, the user must eliminate the cause of the interrupt and set the interrupt index to minus one (255 = EMPTY). As soon as CANxIDX is empty, the BI can enter a new index and initiate an interrupt. An interrupt can only be initiated when CANxIDX contains the value 255.

CANxIDM Identifier Mask Register

	7	6	5	4	3	2	1	0	
r/w	Identifier Mask Bits 4 to 0					x	x	x	3
r/w	Identifier Mask Bits 12 to 5								2
r/w	Identifier Mask Bits 20 to 13								1
r/w	Identifier Mask Bits 28 to 21								0
	0	0	0	0	0	0	0	0	Res

r/w0: Don't care.
r/w1: Compare.
The identifier mask register is 29 bits long; the MSB is in the MSB position in the lowest byte address. The CANxIDM defines a mask for the acceptance of address groups. Only the permitted bits are used for comparison with a received identifier. Whether the mask is used can be determined individually for each receive object.

CANxBT1 Bit Timing Register 1

	7	6	5	4	3	2	1	0	
r/w	MSAM	SYN	BPR						
	0	0	0	0	0	0	0	0	Res

MSAM **Multi Sample**
r/w0: Bus level is determined only once per bit.
r/w1: Bus level is determined three times per bit.

SYN **Sync On**
r/w0: Synchronization with falling edges only.
r/w1: Synchronization with rising edges too.

BPR **Baud Rate Pre-scaler**
r/w: Pre-scaler value.
The baud rate pre-scaler sets the length of a time quantum for the bit timing logic.

$t_Q = (BPR + 1) / f_0$.

With the 6-bit counter it is possible to extend t_Q by a factor of 1...64. Values from 0 to 63 are allowed.

0: $t_Q = 1 / f_0$
1: $t_Q = 2 / f_0$
2: $t_Q = 3 / f_0$
3: $t_Q = 4 / f_0$ etc.

CANxBT2 Bit Timing Register 2

	7	6	5	4	3	2	1	0	
r/w	rsvd	TSEG2			TSEG1				
	0	0	0	0	0	0	0	0	Res

TSEG2 **Time Segment 2**
r/i: TSEG2 value.
TSEG2 determines the number of time quanta after the sample point. Permitted entries: 1...7 (result in 2...8 TQ).

TSEG1 **Time Segment 1**
r/i: TSEG1 value.
TSEG1 determines the number of time quanta before the sample point. Permitted entries: 2...15 (result in 3...16 TQ).

CANxBT3 Bit Timing Register 3

	7	6	5	4	3	2	1	0	
r/w	rsvd	rsvd	rsvd	rsvd	rsvd	SJW			
	x	x	x	x	x	0	0	0	Res

SJW **Synchronization Jump Width**
r/i: SJW value.
SJW defines by how many TQs a bit may be lengthened or shortened because of resynchronization. Permitted entries: 1...4 (result in 1...4 TQ). Values greater than 4 must not be used.

CANxICR Input Control Register

	7	6	5	4	3	2	1	0	
r/w	rsvd	rsvd	rsvd	rsvd	rsvd	XREF	REF1	REF0	
	x	x	x	x	x	0	0	0	Res

XREF **External Reference**
r/w0: The internal reference is used.
r/w1: The external reference is used where available.

REF1 **Use Reference for RxD1**
r/w0: RxD is used as inverted input signal.
r/w1: Supply voltage is used as inverted input signal.

REF0 **Use Reference for RxD0**
r/w0: RxD is used as input signal.
r/w1: Ground is used as input signal.

CANxOCR Output Control Register

	7	6	5	4	3	2	1	0	
r/w	rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	ITX	
	x	x	x	x	x	x	x	0	Res

ITX **Inverted transmission**
r/w0: Tx output is not inverted.
r/w1: output is inverted.

CANxTEC Transmit Error Counter

	7	6	5	4	3	2	1	0	
r	Counter Bit 7 to 0								
	0	0	0	0	0	0	0	0	Res

CANxREC Receive Error Counter

	7	6	5	4	3	2	1	0	
r	x	Counter Bit 6 to 0							
	x	0	0	0	0	0	0	0	Res

CANxCTIM Capture Timer

	7	6	5	4	3	2	1	0	
r	Timer Bit 15 to 8								1
r	Timer Bit 7 to 0								0
	0	0	0	0	0	0	0	0	Res

The Capture Timer is incremented with a clock pulse derived from the CAN bus. Because it can only be read byte-wise, the low byte must be read first. The corresponding high byte is latched at the same time. When CANxCTIM overflows, the flag CTOV in the error status register is set. The Capture Timer will not be incremented during CAN module sleep mode (SLP = 1).

25.2.4. Communication Area (CA)

The CA is located in the CAN-RAM. It consists of com. objects each of which is 16 bytes long. The CA begins at address 0 of the CAN-RAM with the first byte of a CO. It ends with the first byte of a CO which contains ones in its 3 MSBs (communication mode = 7 = EoCA). The following bytes can be used by the application. If the CAN-RAM is filled completely with COs, there is no place left and no need to mark the end of CA.

Every telegram which this node is to receive or transmit is represented by a CO. As well as the data and the time stamp, this also contains a header, the telegram descriptor (TD), in which the attributes of the communication object are stored.

The COs are entered in order of priority into the CA. This starts with the highest priority (the lowest identifier). The identifier defines the priority of a Tg. If the first eleven bits of an ext. Tg are the same as the identifier of a std. Tg, the Tg with standard identifier has higher priority.

25.2.4.1. Telegram Descriptor (TD)

The telegram descriptor is 6 bytes (TD0 to TD5) long and forms the beginning of a CO. Telegrams with std. and ext. identifiers have different TDs. They differ only in the length of the identifiers. 18 bits therefore are not allocated in the TD of a std. Tg. They cannot be used by the application because they are overwritten by the reception of a Tg.

Extended Addr. Format (EXF is set)

	7	6	5	4	3	2	1	0
0	CM			RSC	MID	OW	rsvd	LCK
1	28	ID						21
2	20	ID						13
3	12	ID						5
4	4	ID			0	EXF	RSR	ACC
5	DLC				TIE	RIE	SR	TS

Standard Addr. Format (EXF is deleted)

	7	6	5	4	3	2	1	0
0	CM			RSC	MID	OW	rsvd	LCK
1	28	ID						21
2	20	ID	18	don't use				
3	don't use							
4	don't use					EXF	RSR	ACC
5	DLC				TIE	RIE	SR	TS

Fig. 25–3: Extended and Standard TD Map

Forms of access:
r: read
w: write
i: init (BI halted or CM = inactive)
w0: clear
w1: set

CM **Communication Mode**
r/i: Mode.
CM defines the type of telegram.

0: Inactive Inactive. No participation in the bus traffic.
1: Send Send data.
2: Receive Receive data.
3: Fetch Fetch data via remote frame.
4: Provide Have data fetched via remote frame.
5: Rx-All Receive every telegram.
6: rsvd Don't use (provis. EoCA).
7: EoCA End of Communication Area.

As long as the CO is inactive (CM = 0) or locked (LCK = TRUE), the BI accesses the first byte of the CO only by reading. All other bytes are neither read nor written. The inactive mode is suitable therefore for re-configuration of a CO online; i.e. while the node is taking part in the bus traffic.

RSC **Rescan**
r/w0: Don't rescan.
r/w1: Rescan.
If the rescan bit has been set in a transmit object just processed, the search for active Tx objects is started at the beginning of the communication area. Otherwise, the search continues at this transmit object until the end of the CA is reached. From there, the system jumps back to the beginning of the CA.

MID **Mask Identifier**
r/w0: Don't mask.
r/w1: Mask.
If MID has been deleted, the identifier received is compared bit-by-bit with the identifier from the telegram descriptor, i.e. the entire identifier must be the same so that the telegram received is transferred into this CO. If MID has been set, only bits which are allowed in the ID mask register of the GCS are used for the comparison.

OW **Overwrite**
r/w0: Don't overwrite.
r/w1: Overwrite.
When OW is set, the com. object may be overwritten even if the application has not yet fetched the contents (TS set). The BI must of course obtain right of access (LCK deleted).

LCK **Lock**
r/w0: BI has right of access.
r/w1: BI does not have right of access.
Lock determines the right of access for the BI.

ID **Identifier**
r/i: Identifier.
The ID contains the address of the telegram. 11 bits in the standard mode or 29 bits in the extended mode.

ACC **Access**
r/w0: CPU does not have right of access.
r/w1: CPU has right of access.
Access determines the right of access for the CPU. The CPU should not modify this flag after initialization. In operation mode only the BI modifies it and the CPU reads it.

RSR **Remote Send Request**
r/w0: Remote telegram received.
r/w1: Corresponding data transmitted.
In the provide mode, RSR signals a send request from outside; in the fetch mode it means that a remote Tg is being sent. It is set by the BI if a remote telegram has been received. It is deleted as soon as the corresponding data telegram has been transmitted.

EXF **Extended Format**
r/w0: Standard.
r/w1: Extended.
In order to send/receive telegrams with extended address format, this flag must be switched on. For standard telegrams it is deleted.

DLC **Data Length Code**
r/w: Data length.
The DLC defines the number of data bytes transmitted. Only telegrams with 0 to max. 8 data bytes are transmitted. If the DLC of a TxTg contains a value >8, the entered DLC and exactly 8 bytes will be transmitted. In the case of RxTgs the received DLC, and therefore also values > 8 will be entered by BI.

TIE **Tx Interrupt Enable**
r/w0: Disable.
r/w1: Enable.
Masks the Tx interrupt for this com. object.

RIE **Rx Interrupt Enable**
r/w0: Disable.
r/w1: Enable.
Masks the Rx interrupt for this com. object.

SR **Send Request**
r0: Successful transmission.
r/w1: Send request.
With SR, the microprocessor issues a send request. Both the microprocessor and the BI write the SR flag. If the microprocessor writes a one, the telegram is sent. The BI deletes the SR flag after successful transmission.

TS **Transfer Status**
r/w0: Ready for Transfer.
r/w1: Successful transfer.
The TS flag is set by BI after a successful transfer and is deleted by the microprocessor after a com. object has been processed.

25.2.4.2. Data Field

The data field consists of 8 Byte. They are filled with telegram data according to the DLC. Unused data bytes (DLC less than 8) can be used by the user.

25.2.4.3. Time Stamp

TIMST **Time Stamp**
r: Counter value.
The last two bytes in the CO are used for the time stamp.

At each SoF (Start of Frame) the free-running 16-bit counter CANxCTIM is loaded into a register. When the Tg has been correctly transmitted, this register is copied to the two time stamp bytes of the corresponding CO.

	Data 5
	Data 6
	Data 7
14	Time Stamp low
15	Time Stamp high

Fig. 25–4: Time stamp

25.3. Application Notes

25.3.1. Initialization

After reset, a CAN Module is in standby mode (inactive).

Prior to entering active mode, proper SW configuration of the U-Ports assigned to function as RX input and TX output has to be made (Table 25–1). The RX port has to be configured Special In and the TX port has to be configured Special Out. Refer to “Ports” for details.

For entering active mode of a CAN, set the respective enable bit (Table 25–1).

Table 25–1: Module specific settings

Module Name	HW Options		Initialization		Enable Bit
	Item	Address	Item	Setting	
CAN0	CAN0-RX input multiplexer	PM.U20	CAN0-RX	U2.1 or U4.3 special in	SR0.CAN0
	CAN0-TX output multiplexer		CAN0-TX	U2.0 or U4.2 special out	
CAN1			CAN1-RX	U6.1 special in	SR0.CAN1
			CAN1-TX	U6.0 special out	
CAN2			CAN2-RX	U8.5 special in	SR0.CAN2
			CAN2-TX	U8.4 special out	

In the initialization phase, a configuration of the CAN node takes place. The mode of operation of the BTL and the bus coupling is set. The communication area is created in the CAN-RAM. The different telegrams are specified in it.

The CAN node must be halted (HACK = TRUE) to carry out the initialization. After a reset, the flags HLT and HACK are set and initialization can take place. If initialization is required on-line, the flag HLT must be set. However, the BI must terminate any current transmission before it comes to a halt. For the user this means that he must wait until HACK has been set. If HLT is deleted after initialization, then BI begins to participate in the bus traffic and to scan the CA for tasks.

During initialization, the error status register (CANxESTR) and the interrupt index (CANxIDX) should be deleted, otherwise no interrupts can be initiated.

If telegrams with different identifiers are to be received in a single CO, the identifier mask register must be initialized. This defines which bit of the ID received must be the same as the ID in the CO.

Bit timing registers 1, 2 and 3 and the output control registers 1 and 2 must be initialized in all cases.

The CA must be created in the CAN-RAM. The different COs are created one after the other starting at the address 0. It is important at this point that the three MSBs have been set in the first byte after the last CO, i.e. at an address divisible by 16 (CM = End of CA). This is not necessary if the CAN-RAM is completely filled with COs.

Communication mode (CM), identifier, data length code, extended format flag (EXF) and remote send request flag must be initialized in each CO. Lock flag (LCK) must be deleted and access flag (ACC) must be set in order that the BI may also view this CO. Transfer status flag (TS) must be deleted so that interrupts are not initiated erroneously.

25.3.2. Handling the COs

25.3.2.1. Principles

If the user wishes to access a CO, then he must lock out the BI from access to it. Also the BI reserves access for itself to one CO. In this case the user may not have access. When scanning the CA, the BI ignores inactive or locked COs; i.e. it reads only the first byte and then jumps to the next CO.

Reservations Procedure
If the user would like to access a com. object, then he must first set LCK. Then he must read ACC. If it is TRUE, he has right of access. After the operation he must delete LCK.

```
LCK = TRUE;
if (ACC == TRUE)
    {
    /* CPU has right of access */
    }
LCK = FALSE;
  _________________ or _____________________
LCK = TRUE;
while (ACC == FALSE)
    {
    /* wait until BI is ready */
    }
/* CPU has right of access */
LCK = FALSE;
```

Fig. 25–5: Access to a CO by the user

When the BI is accessing a com. object, it first deletes ACC and then reads LCK. If LCK is FALSE, it has right of access.

```
ACC = FALSE;
if (LCK == FALSE)
     {
     /* BI has right of access */
     }
ACC = TRUE;
```

Fig. 25–6: Access to a CO by the BI

The BI does not wait at a CO until it becomes free.

The BI scans the CA from beginning to end. After a TxTg has been transmitted, the next TxTg entered is reported ready to send.

It makes sense to enter the COs in the CA in order of their priority. The priority is determined by the ID. The lowest ID has the highest priority. If the first bits of an extended ID are identical with a standard ID, the standard ID has higher priority. The CO with the highest priority is at the beginning of the CA. This ensures that Tx-Tgs with high priority are transmitted first when a rescan is initiated.

25.3.2.2. Configuration

A CO may be configured only in the inactive and/or locked mode or when HACK has been set. Otherwise it can lead to access conflicts between the user and BI.

The communication mode (CM) is determined in the configuration phase. The identifiers are also entered. The flag EXF must not be overlooked. The flag RSR and DLC determine whether and how many data bytes will be transmitted in the telegram. The interrupts can be permitted. In case of a receive telegram it is necessary under certain circumstances to set the flags MID and OW. In case of a transmit telegram, the flag RSC must be adjusted.

25.3.2.3. Transmit Telegram

CM = Send

A transmit telegram is used to send data. How many data bytes will be sent is fixed in the DLC. The data is entered directly after the TD. Unused data bytes can be freely used by the user. If after the transmission of this telegram the user would like the next Tx-Tg in the CA to be sent, he deletes the RSC flag. If he sets the RSC, then the transmit search starts again at the beginning of the CA. The RSR flag has to be deleted.

The set SR flag tells BI that this telegram is to be sent; SR can be likened to a postage stamp. The TS flag must be deleted before the CO is released with the deletion of LCK.

If the BI finds a CO whose SR flag has been set, it reserves this (ACC = FALSE) and reports it ”ready to send”. It will be transmitted as soon as no higher-priority telegrams occupy the bus. After successful transmission, it deletes the flag SR and sets TS. The setting of ACC re-releases the CO. Whether an interrupt will be triggered depends on whether CANxIDX in the GCS contains the value minus one (255) and transmit interrupts are permitted.

The user should now reserve the CO, reset the flag TS and delete CANxIDX so that other interrupts can also be reported. Should he wish to send further data, he can now enter this.

25.3.2.4. Receive Telegram

CM = Receive

With a receive telegram, data is received. If the EXF flag and the unmasked bits of the identifier of a received telegram are the same as those of a receive CO, the telegram will be copied to the CO. ID, DLC and data bytes are overwritten by the received ID, DLC and data. Only as many data bytes as the received DLC specify will be overwritten (max. 8). The DLC actually received will be entered. A permitted receive CO is only used when TS has been deleted or OW has been set.

Once a telegram has been received and copied to a CO, the flag TS is set. An interrupt will also be initiated if receive interrupts are permitted and CANxIDX contains the value minus one (255).

If the user detects the reception of a telegram (TS set), he must reserve the CO. Then he can read the data and, before releasing the CO again, delete TS.

25.3.2.5. Receive All Telegrams

CM = Rx-All

If, while searching for an RX-CO, the BI comes across a free Rx-All-CO, the received telegram will be entered here without regard to ID and EXF.

Rx-All-COs should be applied at the end of the CA.

25.3.2.6. Fetch Telegram

CM = Fetch

A fetch CO is used to request data from another node. This is done by sending a telegram with the identifier of the desired data. The remote transmission request flag is set in

this Tg. No data is therefore sent with it. If another node has the desired data available, this is transmitted with the same ID as soon as bus traffic allows.

In this mode, only the reception of the data telegram can trigger an interrupt.

The sequence of a fetch cycle is represented for the user in pseudo-code.

```
if (TS == FALSE && SR == FALSE)    /* CO is empty */
  {
  LCK = TRUE;                /* claim CO */
  /* wait until BI released this CO */
  while (ACC == FALSE) {/* do anything else */}
  SR = TRUE;                 /* send this Tg */
  TS = FALSE;
  LCK = FALSE;               /* release CO */
  }
```

The BI now transmits the telegram with the RTR flag set. The other node receives the Tg, provides the data and returns the telegram with RTR flag deleted. After the reply telegram has been received, the BI sets the flag TS. The user waits for the data.

```
/* wait for answer */
while (TS == FALSE) {/* do anything else */}
LCK = TRUE;           /* claim CO */
/* wait until BI released this CO */
while (ACC == FALSE) {/* do anything else */}
/* copy data */
TS = FALSE;
LCK = FALSE;          /* release CO */
```

Instead of waiting for the answer, it is also possible for notification to be given by a receive interrupt.

25.3.2.7. Provide Telegram

CM = Provide

A provide CO is used to prepare data for fetching. It is the counterpart of a fetch CO. In a provide CO the RSR flag is cleared. It will be set and deleted by the BI. The data can be prepared in two ways:

In the first case, the user does not become active until a remote frame has been received (Rx interrupt or polling from RSR). After the CO has then been reserved, the data is written, the SR flag is set and the CO is released. The BI ensures then that the data is transferred back.

In the second case, the data has already been entered, SR has been set and TS deleted before the request. When the remote frame is received, the user does not need to become active. Also, no Rx interrupt will be initiated. The data is simply fetched. In this case the requesting RTR telegram must contain the correct DLC because, with an RTR telegram too, a received DLC overwrites the local DLC.

In both cases a Tx interrupt can occur after the data telegram has been transmitted.

25.3.2.8. Data Length Code

The data length code is 4 bits long. It can therefore contain values between 0 and 15. In principle, no more than 8 bytes can be transmitted. Empty data telegrams (DLC = 0) are also possible.

If a telegram with a DLC greater than 8 is received, this value will be written into the DLC of the CO, but exactly 8 bytes of data will be copied.

If the DLC of a Tx-CO contains a value greater than 8, this DLC will be transmitted, but only 8 bytes of data.

25.3.2.9. Overwrite Mode

The BI normally processes a CO only when the transfer status TS has been deleted; i.e. the user has processed the CO since the last transmission. In the case of COs with which telegrams are received, the TS flag can be by-passed. If overwrite (OW) is permitted, the BI may overwrite a previously received telegram. When accessing data therefore, the user always receives the most up-to-date data.

25.3.3. Interrupts

All interrupts are enabled or disabled by the global interrupt enable flags, GTIE for Tx interrupts, GRIE for Rx interrupts and EIE for error interrupts in the GCS register. This is the only location for enabling error interrupts. A Tx interrupt can be enabled in the corresponding CO with the Tx interrupt enable flag TIE. An Rx interrupt can be enabled in the corresponding CO with the Rx interrupt enable flag RIE.

An interrupt can only be initiated when the interrupt index CANxIDX is empty (minus one). To initiate an interrupt, the BI enters the number (0...253) of the appropriate CO in the CANxIDX. When an error interrupt is involved, the number 254 is entered.

The BI attempts to initiate an interrupt immediately after successful transfer. If this does not work (CANxIDX not empty), the interrupt is pending (also error interrupt).

The BI permanently scans the CA. If, while doing so, it finds a CO whose interrupt condition is satisfied (e.g. TIE and TS are set), it generates an interrupt. This means that interrupts not yet reported will not be reported in the sequence of their occurrence, but in the sequence in which they are discovered later.

The interrupt service routine of the user must read the CANxIDX. The interrupt source is stored here. If CANxIDX points to a CO (0...253), the user must reserve this. After this, he must first delete TS so that this CO does not initiate an interrupt again. Only then he may release CANxIDX (CANxIDX = 255) so that the BI can enter further interrupts.

25.3.4. Rescan

The normal transmit strategy searches for the next transmit CO in the CA. If all the transmit COs are ready to send, they are processed one after the other. This is a democratic strategy.

If higher-priority TxTgs are reported in the meantime, these are not processed until the complete list has been finished. With rescan, the search for Tx telegrams is started again at the beginning of the CA. By this means the user can force the normal strategy to be interrupted and a search to be made first of all for higher-priority TxTgs. A transmit CO already reported will of course be transmitted first.

The rescan requirement can be achieved dynamically, when a transmit CO is reported, by setting the global rescan flag GRSC.

It is also possible to configure a rescan strategy statically. Each Tx-CO has the rescan flag RSC. If it is set, the system

starts from the beginning with the transmit search after this CO has been processed. It is possible, for instance, to set RSC in the low-priority Tx-COs. Each time a low-priority Tx-CO has been handled, the search continues for higher-priority objects.

The user must ensure that each Tx-CO is processed.

25.3.5. Time Stamp

The time stamp of a CO shows the user how much time has elapsed since the transmission of the object. For this purpose, he compares the time stamp with the capture timer CANxCTIM. Because the time stamp contains the value of the CANxCTIM at the time of the start of transmission, the difference is proportional to the time which has elapsed.

The time stamp mechanism also enables network-wide synchronization. A master transmits a Tg. All nodes note the transmission time (local time). Then the master transmits its own (global) transmission time. The difference between local and global time shows by how much one's own clock (timer) is wrong.

25.3.6. Errors

In the error status register (CANxESTR) error messages and status data are collected which can generate an error interrupt. As long as a flag is set in the CANxESTR, the flag ERS is also set in the status register. This means that the value 254 is written in CANxIDX and an interrupt is generated when EIE has been set.

An error interrupt is deleted by first deleting CANxESTR and then releasing CANxIDX.

The 5 flags BIT, STF, CRC, FRM and ACK originate from the protocol manager. The flag GDM (Good Morning) is not an error flag. GDM is set when the BI is aroused from the sleep mode by a dominant bus level.

The flag ECNT (error counter level) indicates that an error counter has exceeded a limit value. It is set when the transmit error counter exceeds the values 95, 127 and 255 or the receive error counter exceeds the values 95 and 127.

When the BI is in the Bus-Off mode, it no longer actively participates in the bus traffic. Nor does it receive telegrams, but continues to observe the bus. As soon as the BI has detected 128 x 11 successive recessive bits, it reverts from the Bus-Off mode to the error-active mode. At the same time the error counters are cleared.

A Bus-Off sequence triggers two interrupts, if the error interrupt is enabled. The first interrupt (ECNT=TRUE) indicates that the transmit error counter has exceeded the value 255. This means that the module is in the Bus-Off mode now (BOFF=TRUE). The receive error counter is used to count the reception of 128 x 11 successive recessive bits in the Bus-Off mode. This is the reason for the second interrupt (ECNT=TRUE), which indicates that the receive error counter has exceeded the value 95 (warning level). The second interrupt can be ignored in Bus-Off mode. The error interrupt can be disabled during Bus-Off mode to avoid this second interrupt.

25.3.7. Layout of the CA

The CA contains all COs beginning with the lowest identifier. The three MSBs must be set in the byte after the last CO (End of CA).

If the BI has received an identifier complete, it starts at the beginning of the CA with the search for an appropriate Rx-CO. If a rescan is initiated, the BI also starts from the beginning with the transmit search.

25.3.7.1. Buffers

Several successive receive COs may be allocated with the same identifier. The BI stores a received Tg in the first free Rx-CO. Using this mechanism it is possible to construct a receive buffer. If RIE is set in the last CO, the CPU is not informed until the buffer is full.

25.3.7.2. Basic/Full CAN

For a Basic CAN application, a single Tx-CO will be used. All outgoing telegrams will be transmitted with this. The user must receive all Rx-Tgs and must himself decide whether he needs it (acceptance filtering). For this case it is possible to use an Rx-All-CO. But it is necessary to ensure that this can be processed before the next Tg arrives.

For this reason, it is a good idea to employ 2 or 3 Rx-All-COs as buffers after the Tx-CO.

In the case of a FullCAN application, one uses the built-in acceptance filtering and sets up a CO specifically for each desired Rx-Tg and Tx-Tg.

If the CAN-RAM is not big enough, mixed strategies are also possible. The acceptance filtering, of course, burdens the CPU with communication tasks.

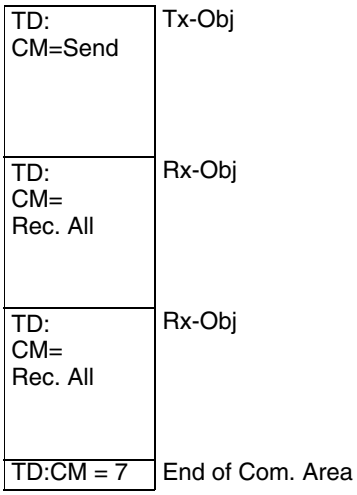


Fig. 25–7: Example: CA of a BasicCAN with 2 Rx-buffers

TD: CM= Receive	Rx-Obj
TD: CM=Send	Tx-Obj
TD: CM=Send	Tx-Obj
TD: CM= Receive	Rx-Obj
TD: CM= Rec. All	Rx-Obj
TD: CM= Rec. All	Rx-Obj
TD:CM = 7	End of Com. Area

Fig. 25–8: Example: CA of a FullCAN with 2 Rx-objects, 2 Tx-objects, and 2 Rx-buffers

TD: CM=Send	Tx-Obj
TD: CM= Rec. All	Rx-Obj
TD: CM= Rec. All	Rx-Obj
TD: CM= Rec. All	Rx-Obj
TD: CM= Rec. All	Rx-Obj
TD:CM = 7	End of Com. Area

Fig. 25–9: Example: CA of a BasicCAN with 4 Rx-buffers

25.3.7.3. Bus Monitor

With some Rx-All-COs it is possible to construct a user-friendly bus monitor. The CPU has merely to observe whether anything has been received. The contents of the CO must be stored. The transmission time can be calculated from the time stamp.

25.3.7.4. Maximum number of COs

The maximum number of COs depends on the size of the CAN-RAM, the baud rate, the system clock, the BI and the CPU accesses to the CAN-RAM.

– The BI can handle a maximum of 254 objects. The limiting factor is the 8-bit register CANxIDX in the GCS. CANxIDX can contain 256 different values. The values 255 (empty) and 254 (error) are reserved. The remaining values 0...253 can indicate 254 objects.

– The maximum number of COs is, of course, limited to a greater extent by the size of the CAN-RAM. The BI can only access the CAN-RAM. Therefore the CA can only be applied there.

  16 bytes are reserved for each CO. One extra byte for coding EoCA after the last CO must not be forgotten. The CAN-RAM area after the EoCA is freely available to the user. No EoCA is necessary if the CAN-RAM is filled completely with COs.

  There is a maximum number of 32 COs possible in a CAN-RAM of 512 bytes.

$$\text{Max. Number CO} = \frac{\text{CAN RAM Size}}{16}$$

– The next limiting factor can be calculated from the baud rate and system clock. After the BI has received an identifier, it must be possible for it to scan the entire CA before the telegram comes to an end.

$$\text{Max. Number CO} = \frac{t_{CA\ SCAN}}{t_{CO\ SCAN}}$$

$$t_{CO\ SCAN} = \frac{9}{f_0}$$

$$t_{CA\ SCAN} = 28\ t_{Bit}$$

$$t_{Bit} = (3 + TSEG1 + TSEG2)\ t_Q$$

$$t_Q = \frac{BPR + 1}{f_0}$$

$t_{CA\ Scan}$ is the time from having received an ID to the end of a minimum telegram (11 bit ID, no data), which is at the BI's disposal to scan the CA.

$t_{CO\ Scan}$ is the worst case time needed by the BI to process an object (A value of 6 I/O cycles is a more realistic size than 9).

With an input frequency of 8 MHz and a baud rate ($1/t_{bit}$) of 1 MBd, the BI could handle 24 COs. Naturally, this value needs to be rounded off.

– The value thus calculated is further limited, however, by the CPU accesses to the CAN-RAM. Each I/O cycle required by the CPU to write or read data in the CAN-RAM is missing from the BI. The BI is halted by CPU accesses. This reduces the time which the BI has to scan the CA. Where there is a reduced CPU clock, in particular, the user should have only limited access to the CAN-RAM.

With the ARM CPU accessing CAN RAM, it is easy to block the BI's CAN-RAM access over a long time. The ARM CPU can make a memory access with each I/O cycle, leaving nearly no I/O cycles to the BI.

In the above example (8 MHz, 1 MBd), $t_{CA\ Scan}$ lasts 224 I/O cycles (28 * 8). The BI needs 144 I/O cycles to scan 16 COs leaving 80 I/O cycles to the CPU to process a telegram. It is not necessary to process more than one telegram during transmission of one telegram. As long as the COs are managed via interrupt, 80 I/O cycles should be more than enough to read or write a CO.

In this worst case scenario the BI needs 288 I/O cycles to scan 32 COs. This is possible at an input frequency of 8 MHz and up to baud rate of 500 kBd. In a more realistic estimation (average $t_{CO\ Scan} = 6$) the BI needs 192 I/O cycles to scan 32 COs leaving 32 I/O cycles to the CPU to process a telegram. This means 1 MBd is possible even with 32 COs, as long as the COs are managed via interrupt only.

Due to this, care has to be taken when using free CAN-RAM (after EoCA). It is not possible here, to make an assumption about how many accesses a non CAN routine makes to its data storage.

25.4. Bit Timing Logic

In the bit timing logic the transmission speed (baud rate) and the sample point within one bit will be configured. By shifting the sample point it is possible to take account of the signal propagation delay in different buses. Furthermore, the nature of the sampling and the bit synchronization can also be defined.

25.4.1. Baud Rate Pre-scaler

The baud rate pre-scaler is a 6-bit counter. It divides the system clock down by the factor 1...64. The output is the clock for the bit timing logic. This clock TQ_{CLK} defines the time quantum (t_Q). The time quantum is the smallest time unit into which a bit is subdivided.

25.4.2. Bit Timing

A bit duration consists of a programmable number of TQ_{CLK} cycles. The cycles are split up into the segments SYNCSEG, TSEG1 and TSEG2.

25.4.2.1. Bit Timing Definition

Sync.Seg.
It is expected that a bit will begin in the synchronization segment. If the bit level changes, the resynchronization ensures that the edge lies inside this segment. The sync.seg is always one time quantum long.

Prop.Seg.
This part of a bit is necessary to compensate for delay times of the network. It is twice the sum of the signal propagation delay on the bus plus input comparator delay plus output driver delay.

Phase Seg.
Phase segments 1 and 2 are necessary to compensate phase differences. They can be lengthened or shortened by resynchronization.

Sample Point
The bus level is read at this point and interpreted as a received bit.

TSEG1
The CAN implementation combines propagation delay segment and phase segment 1 to form time segment TSEG1.

TSEG2
TSEG2 corresponds to phase segment 2.

SJW
The synchronization jump width gives the maximum number of time quanta by which a bit may be lengthened or shortened by resynchronization.

$$t_{Bit} = t_{SYNCSEG} + t_{TSEG1} + t_{TSEG2}$$

$$t_Q = \frac{BPR + 1}{f_0}$$

$$t_{SYNCSEG} = 1\ t_Q$$

$$t_{TSEG1} = (TSEG1 + 1)\ t_Q$$

$$t_{TSEG2} = (TSEG2 + 1)\ t_Q$$

$$t_{SJW} = SJW\ t_Q$$

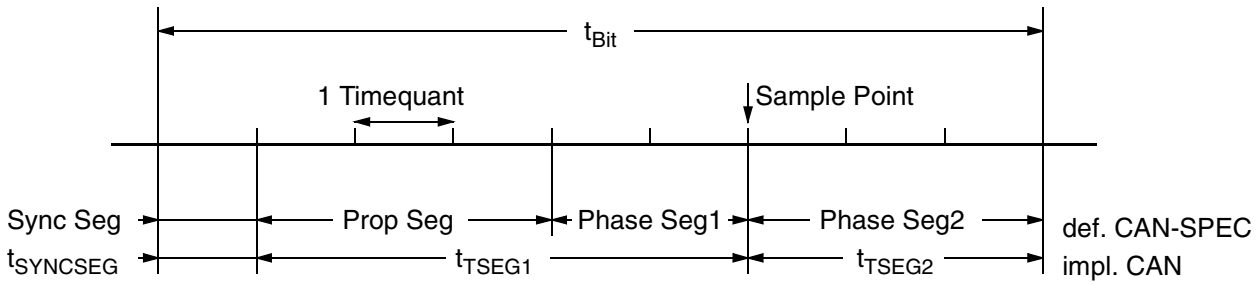


Fig. 25–10: Bit Timing Definition

The baud rate is then calculated as follows:

$$BR = \frac{1}{t_{Bit}}$$

$$t_{Bit} = \frac{(BPR + 1)\ (3 + TSEG1 + TSEG2)}{f_0}$$

$$BR = \frac{f_0}{(BPR + 1)\ (3 + TSEG1 + TSEG2)}$$

25.4.2.2. Bit Timing Configuration

Certain boundary conditions need to be observed when programming the bit timing registers. The correct location of the sample point is especially important with maximum bus length and at high baud rate.

$t_{TSEG2} \geq 2\ t_Q$ = Information Processing Time

$t_{TSEG2} \geq t_{SJW}$

$t_{TSEG1} \geq 3\ t_Q$

$t_{TSEG1} \geq t_{TSEG2}$

$t_{TSEG1} \geq t_{PROP} + t_{SJW}$

The information processing time is the internal processing time. After reception of a bit (sample point) this time is needed to calculate the next bit for transmission.

With a baud rate of 1 MBd a bit should be at least 8 t_Q long.

In case of a triple sample mode (MSAM = 1), the following boundary condition must also be observed:

$$t_{TSEG1} \geq t_{PROP} + t_{SJW} + 2t_Q$$

The triple sample mode offers better immunity to interference signals. In the single sample mode a higher transmission speed is possible.

For high baud rates and maximum bus length, neither SYN nor MSAM may be switched on. Bosch advises against both adjustment facilities. When an input filter matched to the baud rate or a bus driver is used, the triple sample mode is not necessary. If SYN is set, synchronization will also be made with the soft edge (dominant to recessive) and this will mean higher demands being imposed on the clock tolerances.

25.4.2.3. Synchronization

The BTL carries out synchronization at an edge (change of the bus level) in order to compensate for phase shifts between the oscillators of the different CAN nodes.

25.4.2.4. Hard Synchronization

Hard synchronization is carried out at the start of a telegram. The BTL ensures that the first negative edge is in the sync. seg.

25.4.2.5. Resynchronization

Resynchronization takes place during the transmission of a telegram. If the BTL detects an edge outside the sync. seg., it can lengthen or shorten the bit. If it detects the edge during TSEG1, t_{TSEG1} is lengthened. If it detects the edge during TSEG2, t_{TSEG2} is shortened. In this way, it ensures that the edges lie in the sync. seg. T_{SJW} is the maximum time a bit can be lengthened or shortened.

Two forms of resynchronization are possible. In normal operation, synchronization is carried out only with the negative edge (recessive to dominant). At low transmission speeds, synchronization can also be carried out with the rising edge (SYN = 1).

25.5. Bus Coupling

The bus coupling describes the connection of the internal signals rx (receive line) and tx (transmit line) to the pins to the CAN bus.

The output pins are push/pull drivers for TLL levels. The input pins are also designed for TTL levels.

Integrated transceivers (Siliconix Si9200, Philips 82C250 etc.) are available for physical coupling in the high-speed range in compliance with ISO/DIS 11898.

For a laboratory system a “minimum bus” can be constructed by means of a wire-Or circuit.

To utilize the advantages of differential signal transmission, an analogue comparator is necessary.

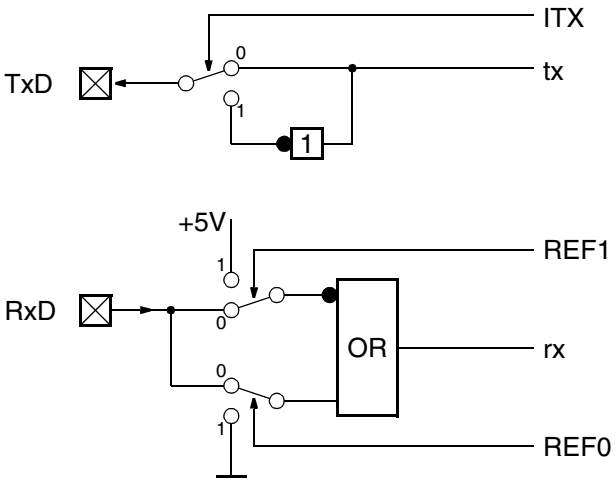


Fig. 25–11: Bus Coupling

Table 25–2: Logical Level Transmitting

ITX	tx	TxD	Bus Level	Remarks
0	0	0	Dominant	direct
0	1	1	Recessive	
1	0	1	Recessive	inverted
1	1	0	Dominant	

Table 25–3: Logical Level Receiving

REF1	REF0	RxD	rx	Bus Level	Remarks
0	0	x	1	Don’t work	
0	1	0	1	Recessive	inverted
0	1	1	0	Dominant	
1	0	0	0	Dominant	direct
1	0	1	1	Recessive	
1	1	x	0	Don’t work	

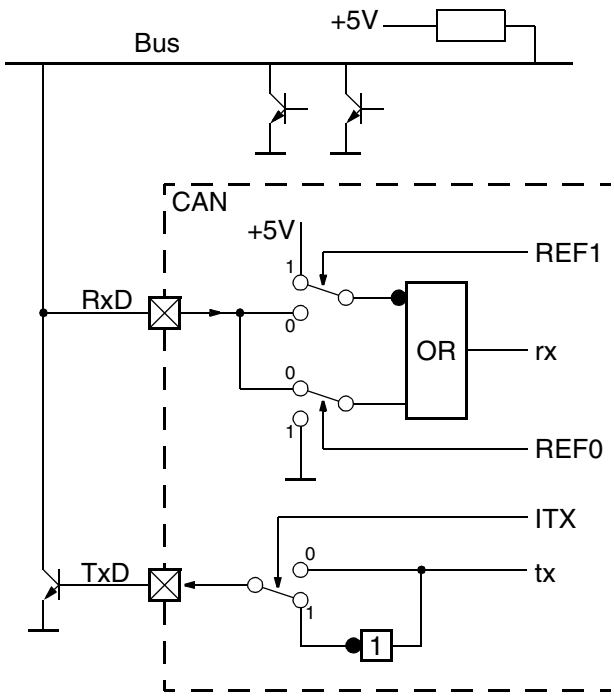


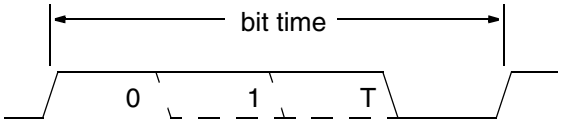
Fig. 25–12: Minimum Bus

26. DIGITbus System Description

26.1. Bus Signal and Protocol

The DIGITbus is a single line serial master-slave-bus that allows clock recovery from the sign stream. Data on the bus are represented by a pulse width modulated signal. There are three different signs:

“0”: 25% High Time
“1”: 50% High Time
“T”: 75% High Time



A permanent high bus (100% High Time) means the bus is passive high. The bus is active if there are consecutive T-Signs, ones or zeros.

A permanent low bus (0% High Time) is interpreted as bus reset or failure indicator. Reasons may be shorts or opens or even a low level forced by a bus node to indicate an internal failure or reset condition.

The sign “T” is used to provide a system wide clock for the bus nodes and to separate the address and data fields and consecutive telegrams.

A telegram normally consists of an address and a data field separated by one “T”. These fields may be as long as necessary. Thus the length of an address or data field may carry information. The end is marked by a “T”. The end of a telegram is marked by two T-Signs.

One system implementation may be confined to certain address and/or data field lengths, thus reducing the hardware or software requirements.

The transmitter of an address has to guarantee that the address is preceded by four T-Signs at least.

An isolated data field is not possible. Each non “T” sequence, which is preceded by two or more consecutive T-Signs must be interpreted as an address. An address field is valid after the reception of the following “T”. The minimum address length is one bit. The minimum data field length is zero bit.

Telegrams with more than one data field are allowed too. For instance TTTTAAATDDDDTDDDDDTT is a valid telegram format on the DIGITbus.

A telegram consisting of an address only is possible too. The length of the data field is zero in this case.

A data field is preceded by an address field and separated from this by a single “T”. It is followed by one T-Sign. After reception of two T-Signs the telegram is finished and valid.

In the idle phase (no information exchange) of the bus traffic, only the bus clock is transmitted.

After the reception of two consecutive T-Signs all bus nodes have to be prepared to receive a new telegram starting with an address field. They are ready to send an address after the reception of four consecutive T-Signs.

The modification of a T-Sign to a zero or one is done by pulling the bus line to low (dominant state) at the right time. This is done by a master sending an address or a data bit or by a slave sending a data bit.

In case of reading data from a slave, the master first sends the address. After receiving the address the slave waits one T-Sign and then modifies the following T-Signs to zeros and ones which the master can recognize.

Slaves do not have the possibility to become active on the bus if they want to communicate a local event or if they need data from a master. It is a polling bus. Only a master is able to send an address. The master has to scan the slaves for their data. But it is possible to transfer data from one slave directly to another slave. The master has to transmit an address for which one slave is the source and the second slave is the destination. Telegrams on the bus are broadcasted. Each bus node may receive them.

26.2. Other Features

There are two possibilities for a slave to signal a local event to the master. They are called wake-up and bus reset.

26.2.1. Wake-up

If the DIGITbus is passive high (permanent high level for more than one bit period) a slave may pull the bus line to low level. This will awake the master who has to store this event in a flag, to start the bus clock and to scan the bus for the source of this event. The minimum low time of the reset pulse is 1/16 of the nominal bit time (1/Baudrate).

26.2.2. Bus Reset

The rising edge of a bit or bus clock is only controlled by the bus node which generates the bus clock (clock master). No other bus node may hold down the bus line at that moment. When the clock master releases the bus line at the end of a bit, he must watch the bus line. If the bus level does not rise after at least 1/2 bit time, this must be interpreted as a protocol violation. Delay of 1/2 of a bit time is the latest moment for a master. He can indicate this protocol violation if the rising edge is delayed 1/8 bit time. Slaves may use this mechanism to signal an exception to the master. They must pull down the bus for at least 2 bit times. After such an event normal communication may be impossible until the PLL of bus nodes have synchronized again.

26.2.3. Phase Correction

On a physical bus the signal edges may be delayed by the bus load. An extra delay may be added by different trigger edges. The bus nodes see the edges at different times. This cause them to pull the bus line delayed. To compensate this effect the phase correction mechanism allows the bus node to adjust their internal counters.

The master sends a special address to which the slave answers with a single zero. The master measures the time between the rising and the falling edge. With this value he can calculate a phase correction value and transmit it to the slave. The slave may use it to adjust his internal counter.

The Phase Correction has to be done for each bus node separately.

26.2.4. Abort Transmission

The Abort Transmission feature is an option that allows the implementation of some kind of rip cord with the DIGITbus. On an alarm event, the SW of the sending master bus node may break the current telegram and send another telegram instead. The reception of an address/data field can not be stopped. The transmission of the alarm telegram is delayed until after the end of the reception in this case. Only the actual sending bus node can abort the transmission.

26.3. Standard Functions

The following standard functions have to be included in every DIGITbus implementation.

26.3.1. Send Bus Clock

The Bus Clock is the sequence of T-Signs on the DIGITbus. The rising edges of the bus signal are of constant distance. Only one bus node may generate this Bus Clock even in a multi master system. All bus nodes use this stream of T-Signs to generate telegrams. The bus clock generator knows two states. “Active Bus” means the transmission of the Bus Clock. “Passive Bus” means permanent high bus level. “Passive Bus” may be a low power mode.

26.3.2. Receive Bus Clock

Bus nodes which does not generate the bus clock need an internal clock for their operation. They may use a separate clock source or derive their clock from the bus clock by a PLL. Bus nodes which use own clock sources nevertheless have to synchronize on the bus clock if they want to transmit or receive data.

26.3.3. Send Address

The Address is the first bit field in a telegram. Only a master may send this field. The sender must guarantee, that at least two consecutive T-Signs have been visible on the DIGITbus before sending this field. Therefore he has to send four T-Signs. If one of those four transmitted T-signs is disturbed, only one of the separated telegrams is corrupted for a receiver. Sending of an address requires synchronization on the bus clock and, in case of a multi master system, collision detection and arbitration capability.

26.3.4. Receive Address

Each slave and all multi master capable bus nodes must be able to receive an address. For a receiver a valid address field must be preceded by two consecutive T-Signs. To verify a received address it is not sufficient to compare the value. The length of the address must be correct too because of the arbitrary length of the address field.

26.3.5. Send Data

Each master must be and some slaves are able to send a data field. A data field is preceded by an address or data field and one T-Sign.

26.3.6. Receive Data

Each master must be and some slaves are able to receive a data field. A data field is preceded by an address or data field and one T-Sign. It is a good idea to verify the length of a received data field if possible. But variable length data fields are possible too.

26.3.7. Collision Detection

Collision detection together with arbitration is necessary in multi master systems. It is necessary to avoid the disturbance of telegrams if two masters try to send a telegram at the same time. As long as both transmit the same sign (one or zero) at the same time, they don’t detect a collision. If one master is sending a one and the other is sending a zero, a zero will be seen at the bus. In this case the master whose one was modified to the zero stops immediately sending. He should receive this telegram.

The sender has to arbitrate his part of the telegram.
Write telegram: TTTTT**AAAATDDDDT**TTTT
Read telegram: TTTTT**AAAAT**DDDDTTTTT
The separator (T-Sign) after an address or data field is object of arbitration too.

In a single master system arbitration loss has to be managed as a bus error.

26.4. Optional Functions

The following optional functions may be designed into a certain DIGITbus implementation.

26.4.1. Abort Transmission

A master who is controlling the transmission of a telegram can abort the sending of the address and data field. After four T-Signs after the last bit he can send another, more urgent telegram. If he is receiving a data field from a slave, he must wait until the slave has finished the data field. Then he can insert a new telegram.

26.4.2. Measure Pulse Width

The capability to measure the pulse width of a high pulse at the DIGITbus may be used for a phase correction by some bus nodes. The bus node who generates the bus clock, sends a data read telegram to another bus node. The other bus node answers with a data field which consists of a single zero. The pulse width of this zero is measured by the master. With this value he can calculate a phase correction value and transmit it to this bus member, which may adjust its time slots to the system dependencies.

26.4.3. Correct Phase

Bus nodes which does not generate the bus clock may use the above described procedure to adjust their phase. They have to answer to a special address with sending back a zero. Afterwards they will receive with another special address a correction value. With this value they can adjust the point where they pull the bus line to modify a “T” to a one or a zero.

26.4.4. Generate Wake-up

If the DIGITbus is passive high (no bus clock, always high level), the clock master may be wake up by pulling the bus level to low (dominant state) for 1/16 bit time at least. All nodes without the clock master may be able to do that.

26.4.5. Receive Wake-up

If there is a low pulse of at least 1/64 bit time on a passive high DIGITbus, the clock master must start to transmit the bus clock by sending T-Signs. All Masters with a bus clock generation unit must be able to do so in a system who uses this feature.

26.4.6. Generate Reset

During active DIGITbus a slave may be allowed to pull down the bus line longer than up to the end of the actual bit time (2 bit times at least). The rising edge at the end of the bit will be delayed in this case. This will disturb the bus clock for all bus nodes.

26.4.7. Receive Reset

The clock master is generating the rising edge at the end of a bit time. He will detect the above described reset condition and set a flag if the rising edge is delayed for at least 1/8 of the bit time.

27. DIGITbus Master Module

The DIGITbus is a single line serial master-slave-bus that allows clock recovery from the sign stream. The address and data field are of arbitrary length.

The DIGITbus Master module is a HW-Module for connecting a single chip controller to the DIGITbus. It generates the bus clock and manages short telegrams autonomously. Transmission and reception of long telegrams is supported by a FIFO each. The DIGITbus Master may be used in a single or in a multi master bus system.

Features

- Single master in a single master system.
- Clock master in a multi master system.
- Passive master in a multi master system.
- Bus clock generation.
- Receive and transmit a telegram with address and data field.
- Transmit FIFO and receive FIFO.
- Collision detection and arbitration.
- Abort transmission.
- Sleep mode.
- Bus monitor mode.
- Measure pulse width for phase correction.
- Phase correction.
- Receive wake-up and bus reset signal.
- Register interface to the CPU.

27.1. Context

Apart from reset and clock line, the interface to the CPU consists of registers connected to the internal address and data bus. An output signal may be connected to the interrupt controller.

A modified universal port builds the output logic which is connected with its special input and output to the DIGITbus Master. This provides an easy way for the SW to hold the bus line permanent low or high, or investigate bus level directly, without support of DIGITbus Master HW.

An open drain output instead of a push/pull output is necessary for the universal port to build a single line wired and bus.

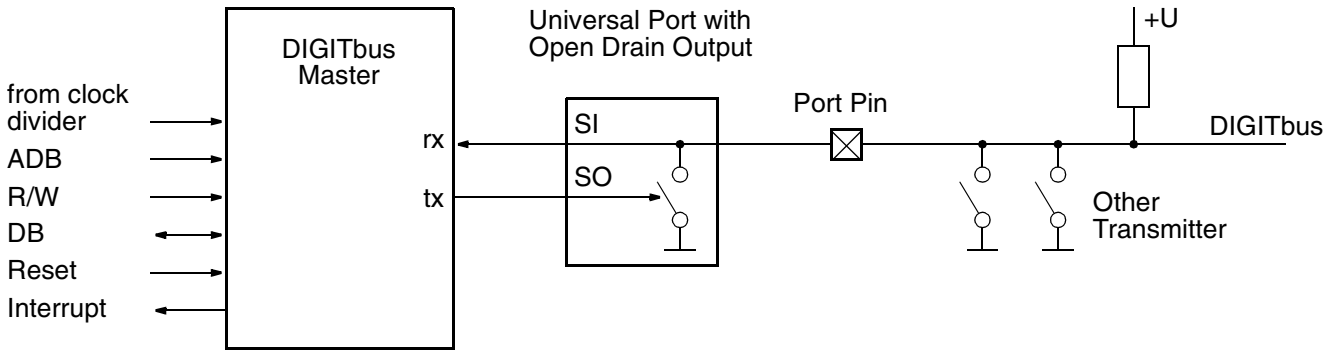


Fig. 27–1: Context Diagram

27.2. Functional Description

27.2.1. 3bit-Prescaler

The programmable 3bit-Prescaler supplies the module with clock signals. It scales down the HW option selectable clock by factor 1, 2, 3 to 8 (see Table 27–2 on page 168). The output is 64 times the bus clock. The desired input frequency from the clock divider is hardware programmable.

27.2.2. Internal Clocks

In low power mode the clock supply of the whole module with exception of the receive bit logic can be stopped. The receive bit logic needs a clock in low power mode too, because it must filter and watch the bus line for a wake-up signal.

27.2.3. Transmit T

The transmit T logic sends a continuous stream of T-signs if active. It outputs a permanent high if it is inactive.

27.2.4. Transmit Bit

Depending on the input signals the transmit bit logic modifies the T-signs to ones or zeros.

A phase correction can be done by adjusting the start time of a transmit bit sequence.

Other bus behavior than sending zeros, ones or T-signs may be forced by the SW using the universal port in normal mode directly. The bus line may be released or pulled low.

27.2.5. Receive Bit

The receive bit logic samples the bus level at a frequency of 64 times of the bus clock. It filters the input signal and decodes the input stream to supply the receive telegram logic with the logical bus signals (0, 1 and T) and the receive clock. Additional it measures the pulse width of each non T-sign. It creates a bus reset signal if the active bus is hold down beyond the end of a bit time. It creates a wake-up signal if there is a low level on the passive high bus.

27.2.6. Send Telegram

The send telegram logic will be enabled by the transmit FIFO and the receive telegram logic if four consecutive T-signs were received. It supports the transmit bit logic with the transmit bit sequence. If it recognizes the begin of a new field, it waits one bit time (separator T-sign).

27.2.7. Receive Telegram

The receive telegram logic traces the bus and indicates the state to the status register and other related modules. The received bit field is written to the receive FIFO. The receive telegram logic is active all the time. Even if the module is transmitting a telegram all bits must be received too in a multi master system, because arbitration may be lost. Reception of own telegrams can be disabled (in a single master system).

27.2.8. Collision Detection

The collision detection logic compares each incoming with the actual outgoing bit. A difference is signaled to the send telegram logic. If the module is transmitting, the send telegram logic is stopped immediately and the transmit FIFO and shift register are flushed.

27.2.9. Transmit FIFO

The transmit FIFO has five entry addresses. One for the field length of address or data field, one for a address byte, one for a data byte, one for more address bytes and one for more data bytes. The field length has to be written once before the corresponding field is entered into the FIFO unless the field length is not a multiple of 8.

An entry into the address register is inserted into the bus clock after the reception of 4 consecutive T-signs. An entry into the data register is inserted into the bus clock after the reception of a non T-sign and one T-sign. Thus it is possible to append a second data field (maybe acknowledge) after the reception of a telegram.

The transmit FIFO may be flushed to abort a transmission. It is also flushed if the transmit telegram logic is active and a collision is detected.

27.2.10. Receive FIFO

The receive FIFO will be filled from the receive shift register. It has two exit addresses. One for the field length and field type and one for the bit field. The field length has to be read before the corresponding field is taken from the FIFO. The receive FIFO will be frozen if it is full. The receive shift register will be over written.

27.2.11. Interrupt

Several flags of the status registers are connected by a logical-or to the interrupt source signal. The interrupt output can be masked by a flag in the control register.

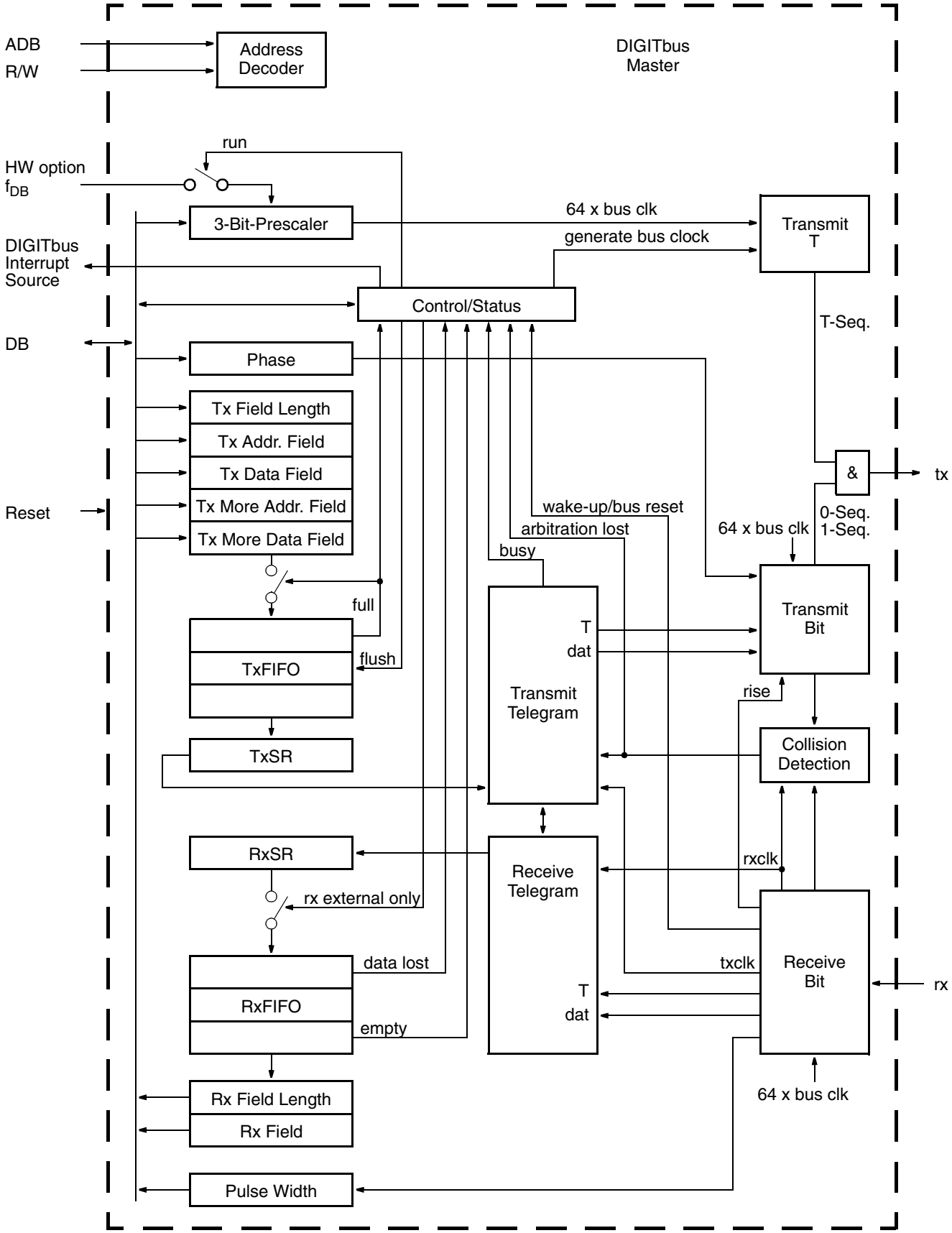


Fig. 27–2: Block Diagram

27.3. Registers

The register mnemonic prefix “DG” stands for DIGITbus.

Table 27–1: Register Mapping

Addr. Offs.	Mnem.	readable	writable
0	DGC0	Control 0	
1	DGC1	Control 1	
2	DGS0	Status 0	
3	DGRTMD	Rx Length	Tx More Data
4	DGTL	Tx Length	
5	DGS1TA	Status 1	Tx Addr.
6	DGTD	reserved	Tx Data
7	DGRTMA	Rx Field	Tx More Addr.

An “x” in a writable bit location means that this flag is reserved. The user has to write a zero to this location for further compatibility. An “x” in a readable bit location means that this flag is reserved. A read from this location results in an undefined value.

DGC0 Control Register 0

	7	6	5	4	3	2	1	0	
r/w	RUN	GBC	ACT	RXO	X	PSC 2 to 0			
	0	0	0	0	x	0	0	0	Res

RUN **Run**
r/w1: Module clock is active.
r/w0: Module is not clocked.
The module is absolute inactive if RUN is zero. Other flags are not functional then.

GBC **Generate Bus Clock**
r/w1: Module generates bus clock
r/w0: No bus clock

ACT **Activate**
r/w1: Module is active (reception and transmission).
r/w0: Module is sleeping (low power mode).
Only the receive bit logic is active in low power mode.

RXO **Receive External Only**
r/w1: Don’t receive own telegrams.
r/w0: Receive all.

PSC **Prescaler**
r/w: Scaling value

Table 27–2: Clock Prescaler

PSC	Divide by	Bus Clock in kHz		
		f_{DB} = 4 MHz	f_{DB} = 5 MHz	f_{DB} = 10 MHz
0x0	1	62.5	78.1	156.25
0x1	2	31.25	39.1	78.1
0x2	3	20.8	26.0	52.1
0x3	4	15.6	19.5	39.1
0x4	5	12.5	15.6	31.25
0x5	6	10.4	13.0	26.0
0x6	7	8.9	11.2	22.3
0x7	8	7.8	9.8	19.5

Note: With an input clock of 5 MHz, the bus clock frequency of 31.25 kHz and its derivatives (16, 8, 4, 2, 1 kHz) can’t be achieved. Thus, with a 5 MHz quartz the DIGITbus should be operated in PLL mode.

DGC1 Control Register 1

	7	6	5	4	3	2	1	0	
r/w	INTE	ENEM	ENOF	x	PHASE				
	0	0	0	x	0	0	0	0	Res

INTE **Enable Interrupt**
r/w1: Enable interrupt
r/w0: Disable interrupt

ENEM **Enable Not Empty Interrupt**
r/w1: Enable
r/w0: Disable

ENOF **Enable Not Full Interrupt**
r/w1: Enable
r/w0: Disable

PHASE **Phase Correction Field**
r/w: Transmit phase.
The start of the transmit frame can be selected in increments of 1/64 of a total bit time related to the rising edge. Values between 0 and 15 are possible, but only the interval from 0 to 9 results in correct behavior.

Set PHASE to 2 if the DIGITbus is operated as clock master (GBC = 1). This is necessary to compensate for internal delay of 2 clocks. Refer to section 27.4.9. for further information about phase correction.

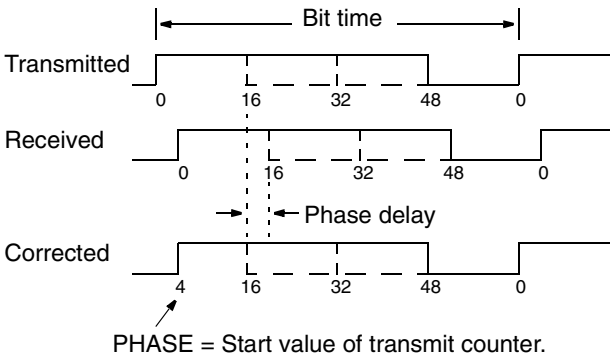
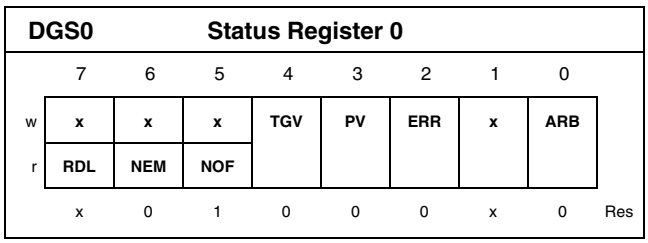


Fig. 27–3: Phase Correction



RDL **Receive Data Lost**
r1: Data lost
r0: No data lost
This flag is set if the receive FIFO is full and the shift register tries to store its contents to the FIFO because a new bit arrives. In this case the FIFO is frozen but the shift register is overwritten. It must be interpreted and cleared by the user. It is cleared by reading an entry from the FIFO.

NEM **Rx FIFO is Not Empty**
r1: There is at least one entry to read.
r0: Empty.
(see Fig. 27–4 on page 169)

NOF **Tx FIFO is Not Full**
r1: There is at least one entry free.
r0: Full.
It generates only an interrupt in the moment when the limit is passed. It doesn't generate interrupts when the FIFO is empty (see Fig. 27–4 on page 169).

TGV **Telegram Valid**
r1: Telegram valid
r0: Telegram not valid
w0: Clear flag
This flag will be set if there were received two consecutive T-signs. It is reset by the HW if a non T-sign is received. It can be cleared by the user if the related telegram is evaluated.

PV **Protocol Violation**
r1: Wake-up if bus is passive high.
Bus reset if bus is active.
r0: No trouble
w0: Clear flag
It must be interpreted and cleared by the user. It is set when the receive bit logic enters or leaves state passive high or when it enters the state passive low.

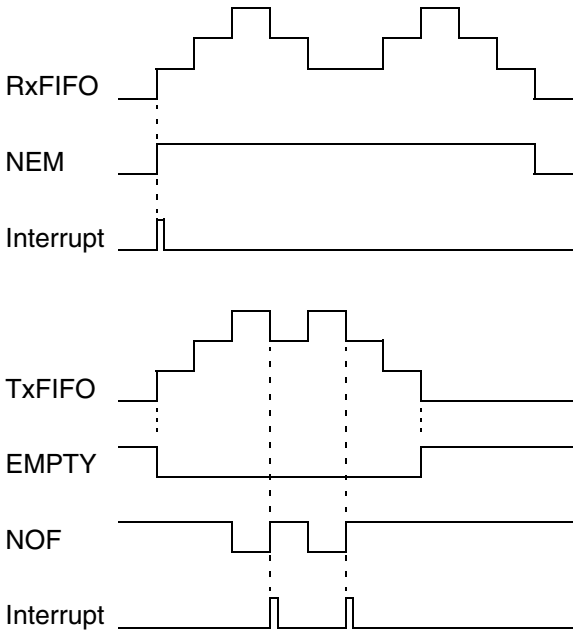
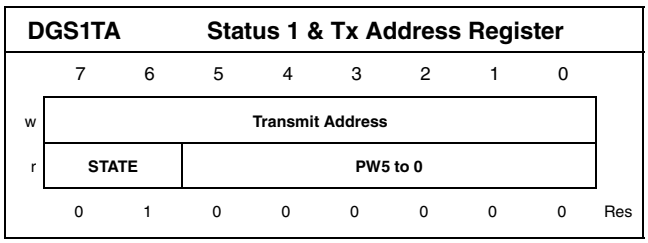


Fig. 27–4: Rx- and TxFIFO Timing

ERR **Error**
r1: Fatal error.
r0: No error
w0: Clear flag
The HW sets this flag either if a dominant level is transmitted and a recessive level is detected (collision error), or if there was a wrong edge within a received bit. If a collision error is detected during transmission, the flag ARB will be set too and transmission stops immediately. This flag has to be cleared by the user.

ARB **Arbitration Lost**
r1: Arbitration lost.
r0: No arbitration loss.
w0: Clear flag
This flag will be set if a collision is detected during transmission. It must be cleared by the user. The transmit buffer was flushed when ARB is true. It is impossible to write to the transmit FIFO as long as ARB is true. Wait until flag TGV is true before reloading TxFIFO. This is automatically done if ARB is evaluated within the TGV interrupt subroutine only.

The Flags RDL, NEM, NOF, TGV, and PV trigger the interrupt source signal (see Section 27.4.7. on page 173).



The first byte of an address field must be written to DGS1TA.

STATE **Bus State**
r: State of receive bit logic.

Table 27–3: Receiver States

STATE	Bus
0 0	Passive low
0 1	Passive high
1 0	Active low
1 1	Active high

PW **Pulse Width**
r: Pulse width
The pulse width of the most recently non T-sign is stored in this register. It is measured in increments of 1/64 of the bus clock period.

DGRTMD **Rx Length & Tx More Data Register**

	7	6	5	4	3	2	1	0	
w	Transmit More Data								
r	RDL	NEM	FTYP	EOFLD	x	LEN2 to 0			
	0	0	x	x	x	x	x	x	Res

More bytes of a data field must be written to DGRTMD.

The read part of register DGRTMD is associated with the front entry in the receive FIFO (the receive field DGRTMA). It has to be read and interpreted before the corresponding FIFO entry.

RDL **Receive Data Lost**
r1: Data lost
r0: No data lost
The flag RDL from the status register DGS0 is mirrored here. It is cleared by a read access to register DGRTMA.

NEM **Receive FIFO is Not Empty**
r1: There is at least one entry.
r0: Empty
The flag NEM from the status register DGS0 is mirrored here. FTYP, EOFLD, LEN and register DGRTMA are not valid if NEM is false.

FTYP **Field Type**
r1: Address field
r0: Data field

EOFLD **End of Field**
r1: Last byte of a field
r0: Not last byte of a field
If EOFLD is set, the corresponding FIFO entry is the last part of the actual field. The next entry, if there is one, belongs to a new field.

LEN **Length of Field**
r: Length of valid data bit
The three bit length doesn't limit the overall length of the corresponding field. The length field defines how many bits of the front entry of the receive FIFO carry valid bits. They are right aligned (Table 27–4). The real length of the field is unlimited. The user must count the bytes he fetched from the FIFO to calculate the real field length.

Table 27–4: LEN usage, Receive and Transmit Length

	LEN 2 1 0	Valid Bit Numbers 7 6 5 4 3 2 1 0
1	0 0 1	_ _ _ _ _ _ _ **x**
2	0 1 0	_ _ _ _ _ _ **x x**
3	0 1 1	_ _ _ _ _ **x x x**
4	1 0 0	_ _ _ _ **x x x x**
5	1 0 1	_ _ _ **x x x x x**
6	1 1 0	_ _ **x x x x x x**
7	1 1 1	_ **x x x x x x x**
0	0 0 0	**x x x x x x x x**

The examples in Table 27–5 illustrate the interpretation of register DGRTMD. They are valid for an address field (FTYP = 1) or a data field (FTYP = 0).

Table 27–5: DGRTMD Interpretation Examples

LEN	EOFLD	
6	1	Last byte of a field. The six right most bits belong to the field.
0	0	A byte of a field. All bits belong to the field. At least one byte follows.
0	1	Last byte of a field. Eight bits belong to the field.
≠0	0	Impossible.

DGRTMA **Rx Field & Tx More Address Register**

	7	6	5	4	3	2	1	0	
w	Transmit More Address								
r	Receive Field								
	x	x	x	x	x	x	x	x	Res

More bytes of an address field must be written to DGRTMA.

The bytes of a received field must be read from register DGRTMA. The meaning of this field (address or data) is defined by the flag FTYP.

Received bytes of a bit field are right aligned. The last byte of a long bit field (with the LSB) may be filled partially. To get the whole bit field right aligned it is necessary to shift all preceding bytes right.

A read access to this register takes the top entry of the receive FIFO. Both registers DGRTMA and DGRTMD are overwritten by the next FIFO entry as result of a read access.

DGTL	Transmit Length Register								
	7	6	5	4	3	2	1	0	
w	x	FLUSH	x	x	x	LEN2 to 0			
	x	0	x	x	x	0	0	0	Res
r	BUSY	EMPTY	x	x	x	x	x	x	
	0	1	x	x	x	x	x	x	Res

The Transmit Length Register is associated with the whole field (address or data) which will be written into the transmit FIFO. It has to be written before the first entry of the field.

BUSY **Transmitter is Busy**
r1: Busy.
r0: Idle.
This flag is true as long as there is an entry in the TxFIFO or transmission is not completed. It is set with the first entry into the TxFIFO and reset after the transmission of the first T sign after a telegram.

FLUSH **Flush Tx FIFO**
w1: Empty Tx FIFO and abort transmission.
w0: No action.
This flag will be reset by the HW autonomously. After FLUSH wait until EMPTY or TGV becomes true before rewriting TxFIFO. Setting of FLUSH clears TGV at the same time.

EMPTY **Tx FIFO is Empty**
r1: No transmit telegram in FIFO.
r0: Transmit telegram in FIFO.

LEN **Length of Field**
w: Length of address or data field.
These three bits correspond to the first byte of a bit field. They define how many bits of this byte carry valid information and should be transmitted (see Table 27–4 on page 170). DGTL must be written before the first byte of the actual bit field is written to the FIFO. It has only to be written once for each bit field. The overall length of the bit field is not limited.

DGTD	Transmit Data Register								
	7	6	5	4	3	2	1	0	
w	Transmit Data								
	x	x	x	x	x	x	x	x	Res

The first byte of a data field must be written to DGTD.

The first byte of a bit field (with the MSB) which is entered into DGS1TA or DGTD, may be partially filled. In the following bytes all bits must contain valid data.

27.4. Principle of Operation

27.4.1. Reset

The module reset signal resets all registers and internal HW. The same does a standby bit in a standby register.

Setting flag RUN in register DGC0 resets all internal HW and registers with exception of registers DGC0, DGC1, DGS0 and DGS1TA. These registers are accessible all the time, they are not reset by any setting of the DIGITbus Master flags.

Internal HW are reset to an inactive state (not transmitting, not receiving). Internal counters are reset to zero. FIFOs and shift registers are empty. Internal representations of the bus line are reset to passive bus level (high).

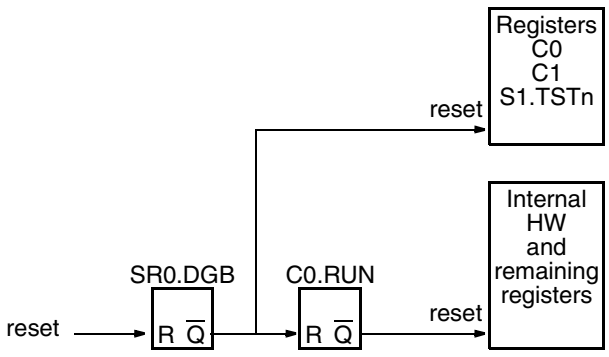


Fig. 27–5: Reset Structure

27.4.2. Initialization

The corresponding port must be configured special out, double pull-down.

After reset and after setting flag DGB in standby register SR0, the DIGITbus master is inactive. The global enable flag RUN must be set together with the appropriate prescaler entry PSC, to activate the module.

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

27.4.2.1. Clock Master

The flag GBC (generate bus clock) must be set, if the DIGITbus master should generate the bus clock. The module acts now as clock master of the connected DIGITbus system. It outputs a stream of T-signs.

27.4.2.2. Receiver/Transmitter

Setting the flag ACT activates the receive and transmit logic. From now on all telegrams are received in the receive FIFO. Writing to the transmit FIFO initiates transmission of a telegram.

The bus clock (T-signs) must be activated some time before the first telegram is transmitted. This is necessary, because other modules may use a PLL for generating the internal clock from the bus clock. No telegram shall be transmitted before all modules have locked on the bus clock.

27.4.2.3. Single Master System

In a single master system (no collision possible), you can suppress reception of transmitted telegrams by setting flag RXO (receive external only). This unburdens the CPU from clearing the receive FIFO of those telegrams.

27.4.2.4. Multi Master System

In a multi master system it is necessary that each transmitted telegram is received too, because arbitration may be lost and then the transmitter becomes a receiver. If arbitration was not lost, the receive FIFO must be read to empty it. The flag RXO has to be cleared in a multi master system.

Table 27–6: Operating modes

RUN	GBC	ACT	RXO	Remarks
0	x	x	x	Standby mode
1	0	x	x	Passive master. External bus clock generation is necessary.
1	1	x	x	Clock master
1	0	0	x	Sleep mode
1	x	1	x	Active mode
1	x	1	0	Receive all. (Recommended in multi master system)
1	x	1	1	Receive external only. (Recommended in single master system)

27.4.3. Transmission

Transmission is initiated by writing a telegram into the transmit FIFO.

If the field length is not a multiple of 8 bit, the total field length modulo 8 has to be written to register DGTL. This must be done once for each field and before any entry to registers DGS1TA, DGTD, DGRTMA or DGRTMD. If the total field length is a multiple of 8 it is not necessary to write the field length to register DGTL.

The first entry of a field (address or data) has to be written right aligned to register DGS1TA (address) or DGTD (data). Further entries of the same field, if it is longer than 8 bit, have to be written to DGRTMA (more address) or DGRTMD (more data). A telegram is transmitted MSB first, hence fields have to be written to transmit FIFO MSB first.

A new address field is transmitted if there were at least 4 consecutive T-signs on the bus. A new data field is transmitted if there was exactly one T-sign. If the last bit of a field was transmitted and there are no more entries in the transmit FIFO, the transmitter stops sending. After reception of two consecutive T-signs the telegram valid flag TGV is set. This is the signal for the SW to evaluate whether transmission was correct or whether an arbitration loss or an error canceled transmission (flags ARB, PV and ERR). In the latter case SW must initiate retransmission.

A telegram has been transmitted correctly, if ARB and ERR are false and EMPTY is true.

Transmission starts with the first entry in the transmit FIFO. Consecutive fields should be entered before the transmission of the preceding field is finished. Take care about possible interrupts.

27.4.3.1. Transmit FIFO

SW must ascertain that there is an empty entry in the transmit FIFO before writing to it. Flag NOF (not full) indicates that there is at least one entry free. Flag EMPTY indicates complete emptiness of transmit FIFO. After reset, FLUSH or ARB wait until flag TGV is true before rewriting TxFIFO.

Short telegrams can completely be buffered in the FIFO. Managing long telegrams is a SW job. The SW must buffer long telegrams and write the parts in time. The transmit FIFO is intended to unburden the CPU from immediately reaction on an NOF interrupt. If an entry becomes free, the SW has time to write, as long as it needs to transmit two FIFO entries and the contents of the transmit shift register. This time must not necessary be the duration for sending 24 bit. May be only one bit of each remaining FIFO entry has to be send.

The transmit FIFO is not intended for telegram tracking. Only one transmit telegram at a time shall be entered.

27.4.4. Reception

Every non T sign is shifted into the receive shift register. If it is full or if a T sign was received, the shift register is stored into the receive FIFO. This is done until the receive FIFO is full. In this case, the FIFO is frozen, but the shift register continues operation. The flag RDL indicates the latter case.

If the shift register is stored to the receive FIFO because a T sign was received, the corresponding flag EOFLD is set, indicating that this is the last entry of a field.

The corresponding flag FTYP is modified at the same time. If two or more consecutive T signs were received in front of the actual field, it is set, indicating that this field has to be interpreted as an address field. If only one T sign has been received in front of the actual field, it is cleared, indicating that it has to be interpreted as a data field.

The flag TGV is set if two consecutive T-signs were received. This is the moment to read status flags and Receive FIFO. The flags PV and ERR have to be interpreted. Even if an error occurred, the Receive FIFO must be emptied by reading it because every telegram or fragment is stored there. Otherwise reception of the next telegram may overflow the receive FIFO, which is indicated by flag RDL.

Every time you want to read DGRTMA, it is ingenious to read DGRTMD first, because DGRTMD and DGRTMA are overwritten with a read access to DGRTMA.

27.4.4.1. Receive FIFO

The receive FIFO contains entries as long as flag NEM is true.

Short telegrams can be buffered completely in the receive FIFO. SW must buffer long telegrams and read parts of it in time.

27.4.5. Sleep Mode

Only the receive bit logic is active in sleep mode. Neither transmission nor reception of telegrams is possible.

A wake-up (passive high to low edge) is signaled by flag PV.

The DIGITbus master is not automatically activated by a wake-up. This has to be done by SW. The flag PV can be used to trigger an interrupt.

Switching to Sleep Mode while a telegram is transmitted can cause problems. Hence make sure, that bus clock generation is switched off only if bus is idle (T-signs).

27.4.6. Abort Transmission

Writing a one to flag FLUSH aborts the transmission of a telegram after completion of the actual transmitted bit, if the DIGITbus master is the transmitter. The transmit FIFO is emptied and another, more urgent telegram can be transmitted. Transmission of the new telegram starts, as soon as 4 consecutive T signs were received after the aborted telegram.

Flag TGV is cleared with a FLUSH. This is the reason why TGV is set (and interrupt is triggered if enabled) after reception of 2 T signs, even if no telegram was aborted by FLUSH because it happened during transmission of T signs.

Resetting of Flag TGV is the reason why an aborted address field is marked as data field (FTYP = 0) in the RxFIFO.

It is not possible to abort a telegram or a field which is transmitted by another bus node.

27.4.7. Interrupt

Five flags (RDL, NEM, NOF, TGV, PV) are connected to the interrupt source output by an or operation. This output can be enabled globally by flag INTE. The interrupt generation of two flags (NEM, NOF) can be enabled locally by flags ENEM and ENOF. A rising edge of a flag triggers the interrupt source output.

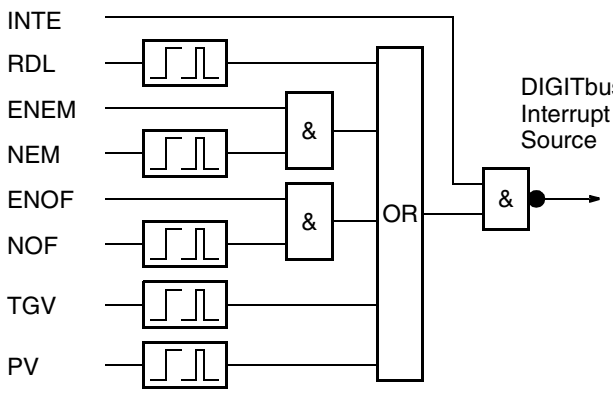


Fig. 27–6: Interrupt Sources

27.4.8. Measure Pulse Width

The pulse width (high time) of every non T sign is stored with the falling edge of the bus signal in status register DGS1TA in the field PW. T signs doesn't affect PW. It must be read before the falling edge of the next non T sign.

27.4.9. Correct Phase

The rising edge of the bus signal can be delayed by inner (sampling and filter) or outer (bus load) influences. This delayed rising edge resets a 6 bit transmit counter in the transmit bit logic. The transmit counter pushes the bus line low when it reaches 15 (transmitting 0) or 31 (transmitting 1). It releases the bus line when it reaches 55.

The transmit counter is reset to a value which contains two zeros at the most significant position and the four PHASE bits of the control register DGC1 at the least significant position. This allows an adjustment of the transmitted non T signs between 0 and 15/64 of the whole bit length.

27.4.10. Error

The setting of flag ERR may have one of the following causes:

– Wrong baud rate of DIGITbus Master or other bus nodes.

– Wrong port configuration of DIGITbus Master.

– Disturbances on bus line.

– HW damaged of DIGITbus Master.

27.4.11. Precautions

Don't access DIGITbus registers in CPU Slow and Deep Slow mode. This can cause interrupts.

If f_{XTAL} is 5 MHz, a bus clock of 31.25 kHz is only in PLL mode possible (Table 27–2).

27.5. Timings

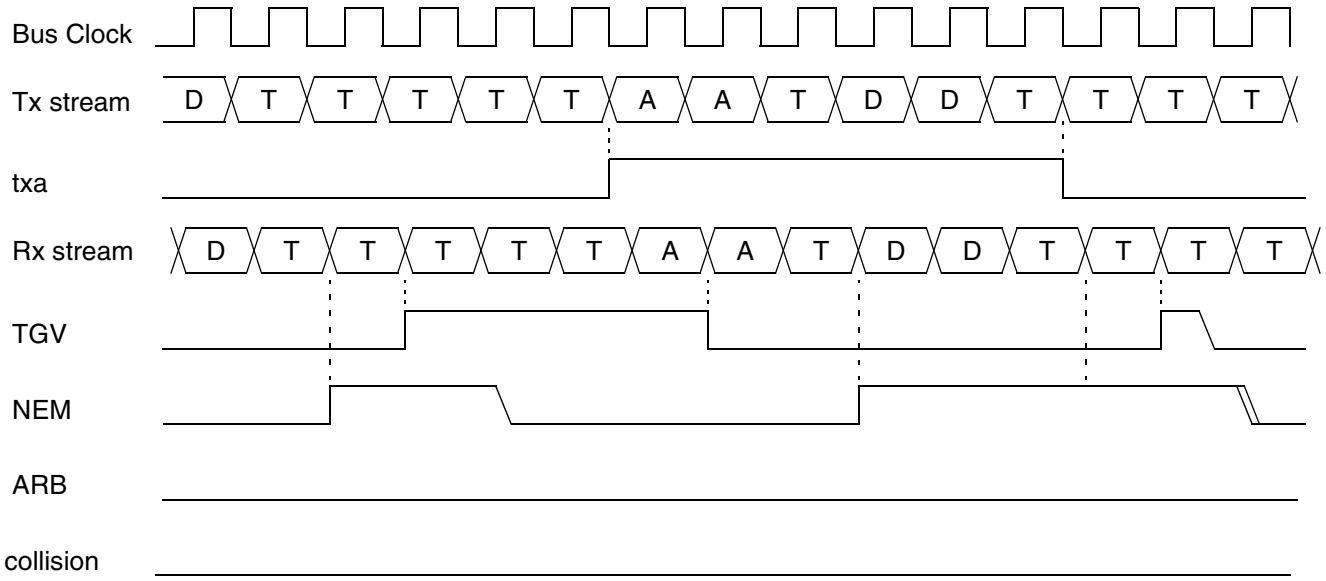


Fig. 27–7: Tx Timing

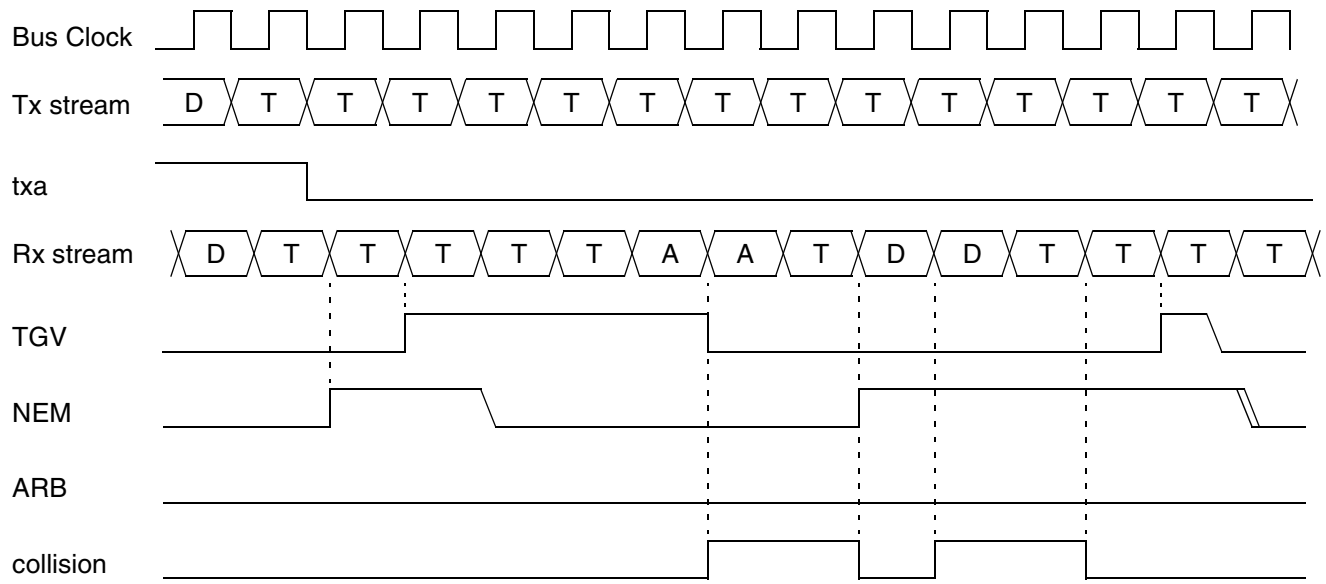


Fig. 27–8: Rx Timing

28. Audio Module (AM)

The Audio Module AM provides a gong output signal that may be used to drive a speaker circuit.

The output signal is a square wave signal with selectable gong frequency.

The gong signal amplitude is defined by the pulse width of a PWM signal. An internal accumulator is selectable to automatically decrease this pulse width and thus the gong amplitude following an exponential function.

Features

- Programmable gong frequency
- Programmable gong duration
- Programmable initial amplitude
- Gong can be stopped and retriggered
- Generation of an exponentially decreasing gong amplitude function without CPU interaction

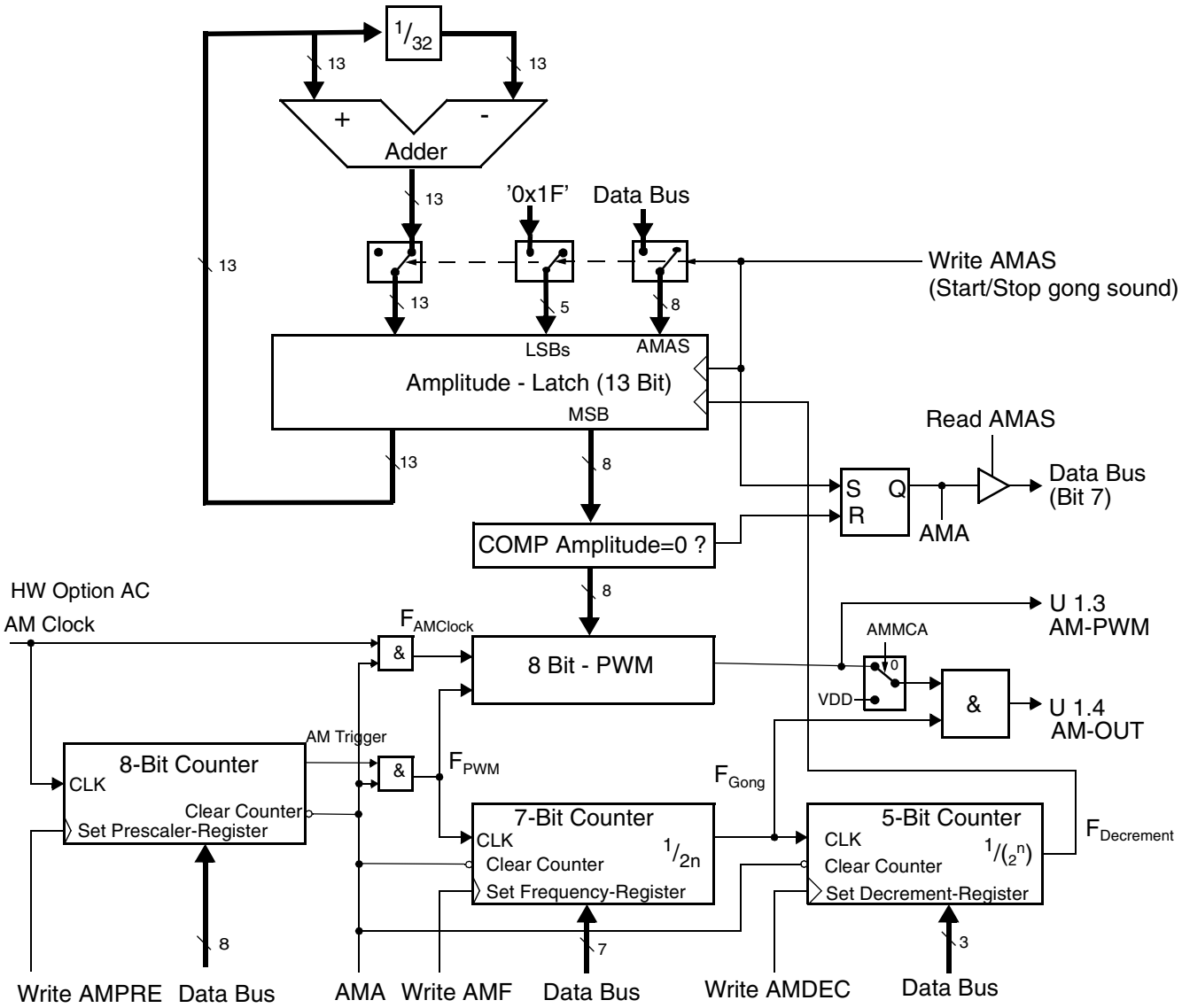


Fig. 28–1: Block diagram of the audio module

28.1. Functional Description

The Audio Module output frequency is defined by the following formulas:

Frequency:

$$F_{Gong} = \frac{F_{AMTrigger}}{2(AMF+1)} = \frac{F_{\mathrm{AMClock}}}{2(AMF+1)(AMPRE+1)}$$

$$t_d \cong \frac{\ln 0{,}5 - \ln \mathrm{AMAS}}{\ln\left(1-\frac{1}{32}\right)} \cdot \frac{2^{\mathrm{GDF}}}{F_{\mathrm{Gong}}}$$

Amplitude:

$$\mathrm{Ampl.} \cong \frac{(\mathrm{AMAS}+1)}{(\mathrm{AMPRE}+1)}$$

where the maximum amplitude is 1 if AMAS is equal to or bigger than AMPRE. In the latter case the amplitude remains constant until the decay mechanism has decreased AMAS below AMPRE.

Duration:

AMF, AMPRE, AMAS and GDF are register values and described later.

The initial gong sound amplitude is set by writing the Audio Module Amplitude & Status Register (AMAS), this write also starts the gong sound. An active audio module is indicated by the read only Audio Module Active Bit (AMA) in the AMAS.

Every 1st..32nd cycle of the gong sound frequency (depending on the Gong Duration Factor (AMDEC.GDF)) a new amplitude value is calculated ($F_{Decrement}$). The falling edge of the amplitude decrement frequency $F_{Decrement}$ is latching the output of the adder into the amplitude latch (13 Bit) and simultaneously the 8 MSBs into the PWM.

During the first low cycle of F_{Gong} following the active $F_{Decrement}$ edge the PWM is already running with the newly calculated amplitude, but takes effect at the output not until the next high cycle of F_{Gong}. F_{Gong} is modulating the PWM-output to generate the gong sound frequency, while the decreasing PWM-value generates an exponential decreasing amplitude.

As soon as the 8 MSBs of the amplitude latch are reaching zero, the AMA will be reset, which deactivates the audio module.

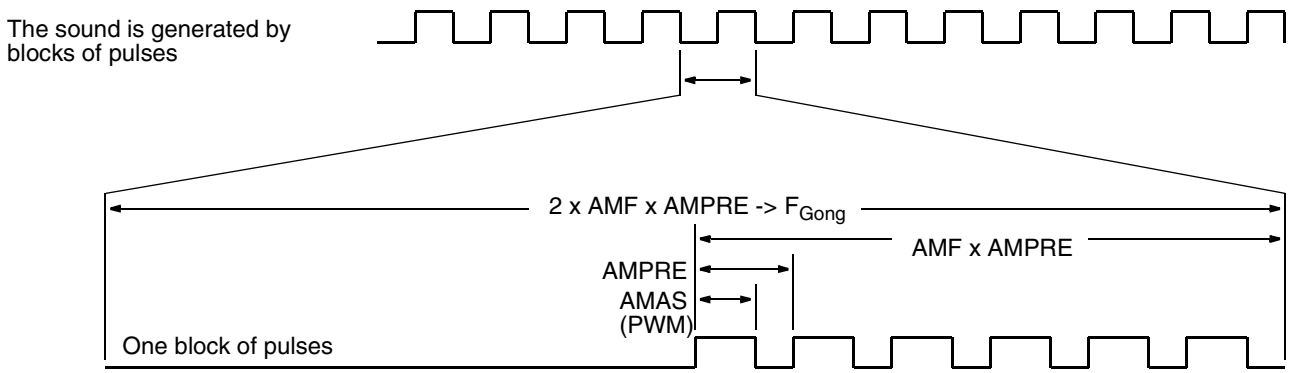


Fig. 28–2: Sound generation

28.1.1. Hardware Settings

The AM clock frequency $F_{AMClock}$ is set by HW option AC.

28.1.2. Initialization

Prior to entering active mode, proper SW initialization of the Ports has to be made. The ports have to be configured Special Out. Refer to “Ports” for details.

Three Audio Module Registers have to be set before the gong sound can be started: the gong prescaler (AMPRE), the gong sound frequency (AMF) and the gong duration factor (AMDEC.GDF) register.

For the effect of CPU clock modes on the operation of this module refer to section “CPU and Clock System” (see Table 4–1 on page 36).

28.1.3. Start Gong

The gong sound is started by writing the initial amplitude value into AMAS. Simultaneously with the write to AMAS the Flag Audio Module Active (AMA) is set, which enables the $F_{AMClock}$-input.

28.1.4. Restart Gong

It’s possible to restart the gong sound simply by writing a new initial amplitude value to AMAS independent of the

former initial value or the current value of the register. (Note: The current amplitude value can't be read out). The new gong sound will start immediately with a low cycle of F_{Gong}.

28.1.5. Stop Gong

The gong sound will stop automatically as soon as the amplitude value in AMAS reaches zero. This will reset the AMA, which indicates the inactive audio module.

To stop the gong sound, just write 0x00 into AMAS. The gong sound then will stop immediately with the writing of 0x00 (also indicated by AMA).

A continuous tone will never stop automatically. It has to be stopped by writing 0x00 into AMAS.

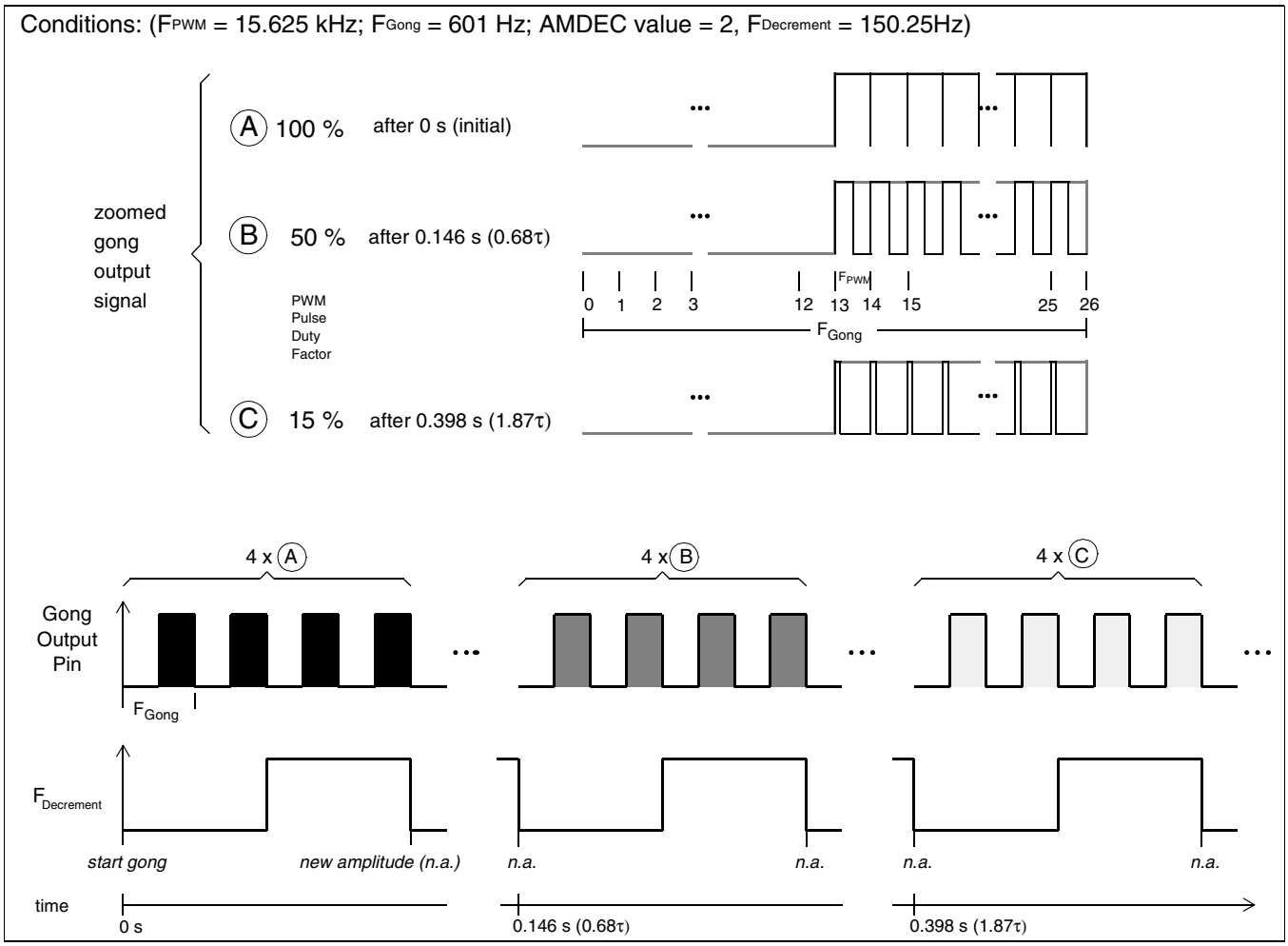


Fig. 28–3: Example sections of the audio module output signal

28.1.6. Decay of Sound

The decay characteristic used for this gong sound is described by the following exponential function:

$$A_n \cong A_0 (1 - {}^1/_{32})^n$$

with A_0 = initial amplitude (AMAS)
A_n = amplitude after n $F_{Decrement}$ cycles
n = int (t * $F_{Decrement}$)
= number of decrement cycles

Following the above formula, n can be expressed as

$$n \cong \frac{\ln A_n - \ln A_0}{\ln\left(1 - \frac{1}{32}\right)}$$

Each $F_{Decrement}$ cycle the amplitude is decreased by 1/32. $F_{Decrement}$ is determined by the value of GDF in the register AMDEC and by F_{Gong}:

$$F_{Decrement} = \frac{F_{GONG}}{2^{GDF}} \qquad GDF = 0 \ldots 5$$

With GDF settings of 6 and 7 the gong sound amplitude update frequency $F_{Decrement}$ is zero (continuous tone).

The time constant τ of the above exponential function is defined as the time interval within which the amplitude A is decreasing to 36.8%.

Given

$$0,368 = \left(1 - \frac{1}{32}\right)^{n_\tau}$$

the number n_τ of $F_{Decrement}$ cycles needed to reduce the initial amplitude to 36.8% is

$$n_\tau \cong 32$$

With an initial amplitude of 0xFF the total time $t_{255->0}$ needed to reach zero amplitude in the 8 Bit - AMAS is $n = 193$ $F_{Decrement}$ cycles, which is approximately 6τ.

With an initial amplitude lower than 0xFF the gong sound duration is shorter.

That means that τ is correlating with $F_{Decrement}$. The higher $F_{Decrement}$, the shorter is τ.

The total time from a start amplitude A_0 to an end amplitude A_n is approximately calculated according to following formula.

$$t_{A_0 \to A_n} \cong \frac{\ln A_n - \ln A_0}{\ln\left(1 - \frac{1}{32}\right)} \cdot \frac{2^{GDF}}{F_{GONG}}$$

To sum up it can be said that the total duration of the gong sound depends on F_{Gong}, set with AMF and AMPRE, the setting of the Gong Duration Factor GDF and the setting of the initial amplitude AMAS.

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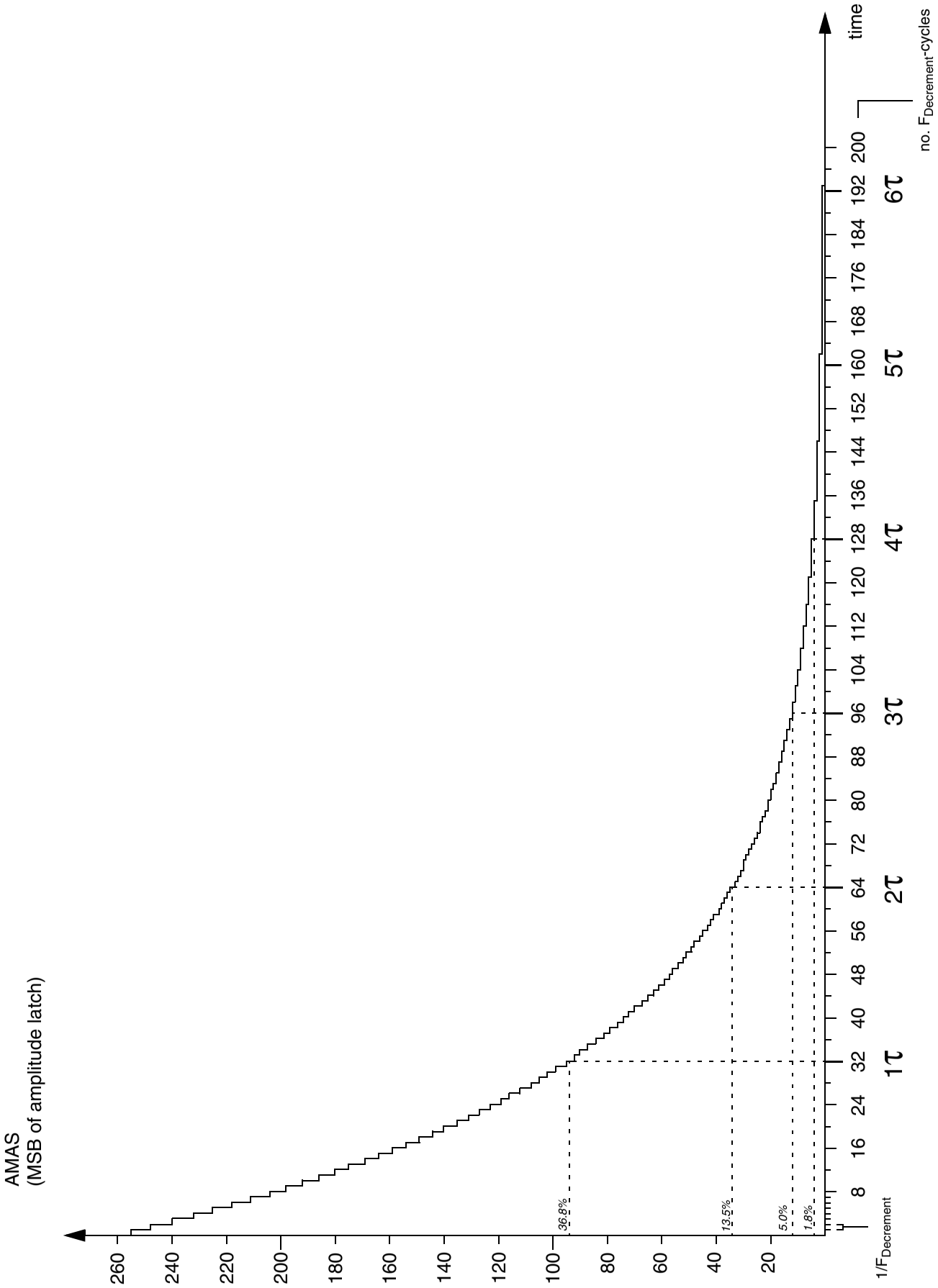


Decay of Sound - Function

28.2. Registers

AMAS	Audio Module Amplitude and Status Register							
	7	6	5	4	3	2	1	0
w	Initial Amplitude							
r	AMA	x	x	x	x	x	x	x
	0	x	x	x	x	x	x	x

Note: Res

Initial Amplitude

A write access to this register starts or stops the gong sound, while the value written is the initial amplitude. Writing the value 0x0 into this register during an active gong sound deactivates the gong sound immediately, while writing a value > 0x0 is restarting the gong sound immediately with the new Initial Amplitude.

wnn: (Re-)Start gong sound with initial amplitude.
w00: Stop gong sound.

AMA Audio Module Active Flag

This flag indicates an active Audio Module generating a gong sound.

r1: Audio Module is active.
r0: Audio Module is not active.

AMF	Audio Module Frequency Register							
	7	6	5	4	3	2	1	0
w	x	Sound Frequency						
	-	0	0	0	0	0	0	0

Note: Res

With this register the gong sound frequency is programmed. The PWM frequency is divided by twice the register value increased by one.

The value which has to be written, resp. the resulting gong sound frequency is calculated with:

$$AMF = \frac{F_{AMTrigger}}{2F_{GONG}} - 1$$

It's possible to write a new gong sound frequency during an active audio module (AMA = '1').

AMDEC	Audio Module Decrement Register							
	7	6	5	4	3	2	1	0
w	AMMCA	x	x	x	x	GDF		
	0	-	-	-	-	0	0	0

Note: Res

AMMCA Audio Module Maximum Constant Amplitude Flag

w1: Activate the AMMCA mode.
w0: Deactivate the AMMCA mode.

With the flag AMMCA the Audio Module Maximum Constant Amplitude mode is selected. If this Flag is set, the gong sound with the maximum, not decreasing amplitude is available at the audio module output pin. The only difference between this tone and a 'normal' gong sound is the constant, not decreasing amplitude. The handling of this tone (i.e. start, stop, frequency, duration) is the same. The tone is started by writing an initial value to AMAS, but this value will only influence the duration of the tone, not its amplitude.

GDF Gong sound Duration Factor

This register sets the gong sound duration in dependence of F_{Gong}. With GDF=0 the amplitude will be decreased every F_{Gong} - cycle, values 1 to 5 will result in a amplitude update frequency of F_{Gong} / 2 to F_{Gong} / 32 according to this equation:

$$F_{Decrement} = \frac{F_{GONG}}{2^{GDF}} \qquad GDF = 0\ldots5$$

A value of 6 or 7 disables decrease of the amplitude, so a continuous tone with the initial amplitude will be generated ($F_{Decrement}$ = 0). To stop the continuous tone write a 0x00 to AMAS or change the gong sound duration factor to let the tone decay. It's possible to change GDF during an active gong sound (AMA = '1').

Table 28–1: Definition of GDF

GDF	gong sound duration factor
0x0	1
0x1	2
0x2	4
0x3	8
0x4	16
0x5	32
0x6	continuous tone
0x7	

AMPRE	Audio Module Prescaler							
	7	6	5	4	3	2	1	0
w	Prescale Value							
	1	1	1	1	1	1	1	1

Note: Res

AMPRE defines the frequency of the trigger input of the Audio Module. The AM clock input is divided by the Prescale Value plus one to derive the trigger frequency F_{PWM}.

$$\mathrm{AMPRE} = \frac{F_{\mathrm{AMClock}}}{F_{\mathrm{AMTrigger}}} - 1$$

AMPRE must be greater than zero.

29. Hardware Options

29.1. Functional Description

Hardware Options are available in several areas to adapt the IC function to the host system requirements:

– clock signal selection for most of the peripheral modules from f_0 to $f_0/2^{17}$ plus some internal signals (see Table 29–4 on page 183)

– Special Out signal selection for some U- and H-ports

– Rx/Tx polarity selection for SPI and UART modules

Hardware Option setting requires two steps:

1. selection is done by programming dedicated address locations in the HW Options field (see Section 29.2. on page 182) with the desired options' code (see Section 29.3. on page 183).

2. activation is done by copying the HW Options field to the corresponding HW Options registers (see Section 29.3. on page 183) at least once after each reset.

All HW Options except these listed in table 29–1 are SW progammable.

Table 29–1: Port, Clock and CM Option Programmability

IC Type	IC Name	Port Opt.	Clock Opt.	CM.WCM setting
EMU	CDC3205G-A	mask	SW	set to 0
	CDC3205G-B	SW	SW	set to 0
MCM	CDC3207G-B	SW	SW	set to 0
Mask	ROM Part	SW	mask	mask

In mask ROM derivatives the clock options and the Watchdog, Clock and Supply Monitors are hard wired according to the HW Options field of the ROM code hex file. Those options can only be altered by changing a production mask.

To ensure compatible option settings in this IC and mask ROM derivatives when run with the same ROM code, it is mandatory to always write the HW Options field to the HW option registers directly after reset.

29.2. Listing of Dedicated Addresses of the Hardware Options Field

Please refer to section “Memory and Boot System” for the dedicated start address of the HW Options field.

Table 29–2: HW Options Field

Offs.	Mne.	Options
0x00	T0C	Timer 0 Clock
0x01	T1C	Timer 1 Clock
0x02	T2C	Timer 2 Clock
0x03	T3C	Timer 3 Clock
0x04	T4C	Timer 4 Clock
0x05	CO00C	Clock Out 0: Mux0 Pre. & Clock
0x06	CO01C	Clock Out 0: Mux1 Clock
0x07	CO02C	Clock Out 0: Mux2 Clock
0x08	DMAC	DMA Timer Clock
0x09	CO1C	Clock Out 1: Pre. & Clock
0x0A	C0C	CAPCOM Counter 0 Clock
0x0B	C1C	CAPCOM Counter 1 Clock
0x0C	DC	DIGITbus Clock
0x0D	LC	LCD Pre. & Clock
0x0E	AC	AM Clock
0x0F	PF0C	PFM 0 Clock

Table 29–2: HW Options Field

Offs.	Mne.	Options
0x10	SMC	SM, SPI0, SPI1 Pre. & SM Clock
0x11	SP0C	SPI0 I/O & F0SPI Clock
0x12	SP1C	SPI1 I/O & F1SPI Clock
0x13	SP2C	F2SPI Clock
0x14	P9C	PWM 8, 9 Clock
0x15	P9P	PWM 8, 9 Period
0x16	P11C	PWM 10, 11 Clock
0x17	P11P	PWM 10, 11 Period
0x18	P1C	PWM 0, 1 Clock
0x19	P1P	PWM 0, 1 Period
0x1A	P3C	PWM 2, 3 Clock
0x1B	P3P	PWM 2, 3 Period
0x1C	P5C	PWM 4, 5 Clock
0x1D	P5P	PWM 4, 5 Period
0x1E	P7C	PWM 6, 7 Clock
0x1F	P7P	PWM 6, 7 Period
0x20		
0x21		
0x22		
0x23		
0x24		
0x25		
0x26		
0x27		
0x28		
0x29	PM	Port Mux
0x2A	CM	Clock Monitor
0x2B		
0x2C	UA0	UART0 I/O
0x2D	UA1	UART1 I/O
0x2E		
0x2F		

29.3. HW Options Registers and Code

The mapping of the HW Options registers corresponds exactly to the HW Options field in the section above. The order of the HW Options registers description in this section does not correspond to the order of the HW Options field.

The emulator IC allow SW programming of the whole registers. Future mask ROM derivatives don't allow to write other clock option values as defined in the HW Options field.

The clock options may be programmed to values according to table 29–4 on page 183.

Some of the clocks may be pre scaled by a programmable value. Refer to table 29–3 for possible values.

Table 29–3: Clock Prescaler

PRE		Prescale Value
1	0	
x	0	direct
0	1	1/1.5
1	1	1/2.5

Table 29–4: Clock Option Selection Code

Clock Option Number	Clock Signal	Selection Code
f0	f_0	xxx0.0000
f1	f_1	xxx0.0001
f2	$f_1/2^1$	xxx0.0010
f3	$f_1/2^2$	xxx0.0011
f4	$f_1/2^3$	xxx0.0100
f5	$f_1/2^4$	xxx0.0101
f6	$f_1/2^5$	xxx0.0110
f7	$f_1/2^6$	xxx0.0111
f8	$f_1/2^7$	xxx0.1000
f9	$f_1/2^8$	xxx0.1001
f10	$f_1/2^9$	xxx0.1010
f11	$f_1/2^{10}$	xxx0.1011
f12	$f_1/2^{11}$	xxx0.1100
f13	$f_1/2^{12}$	xxx0.1101
f14	$f_1/2^{13}$	xxx0.1110
f15	$f_1/2^{14}$	xxx0.1111
f16	$f_1/2^{15}$	xxx1.0000
f17	$f_1/2^{16}$	xxx1.0001
f18	V_{SS}	xxx1.0010
f19	T0-OUT	xxx1.0011
f20	V_{SS}	xxx1.0100
f21	fSM	xxx1.0101
f22 [1])	$fSM/2^8$	xxx1.0110
f23	fCC0IN	xxx1.0111
f24	fCC1IN	xxx1.1000
f25, 26, 27	V_{SS}	xxx1.1001 ...
f28	$f_1/2^1$	xxx1.1100
f29, 30	V_{SS}	xxx1.1101 ...
f31	$f_1/2^9$	xxx1.1111

If the leading "x" in the Clock sampling table are not used for the purpose of coding other options, they must be replaced by zeros.
1) Clock option f22 is only available if the Stepper Motor Module has been enabled by the standby bit.

29.3.1. Timers

T0C Timer 0 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f1 to f31				
	x	x	x	0x01				Res

T1C Timer 1 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

T2C Timer 2 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

T3C Timer 3 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

T4C Timer 4 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

29.3.2. PWMs

The high pulse width of the trigger period must be greater than the high pulse width of the clock the PWM is provided with.

P1C PWM 0, 1 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

P1P PWM 0, 1 Period

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x08				Res

P3C PWM 2, 3 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

P3P PWM 2, 3 Period

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x08				Res

P5C PWM 4, 5 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

P5P PWM 4, 5 Period

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x08				Res

P7C PWM 6, 7 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

P7P PWM 6, 7 Period

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x08				Res

P9C PWM 8, 9 Clock

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

P9P PWM 8, 9 Period

	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x08				Res

P11C	PWM 10, 11 Clock							
	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

P11P	PWM 10, 11 Period							
	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x08				Res

29.3.3. CAPCOMs

C0C	CAPCOM Counter 0 Clock							
	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

C1C	CAPCOM Counter 1 Clock							
	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

29.3.4. DIGITbus

DC	DIGITbus Clock							
	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

29.3.5. DMA

DMAC	DMA Timer Clock							
	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

29.3.6. PFM

PF0C	PFM 0 Clock							
	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

29.3.7. Clock Out

CO00C	Clock Out 0: Mux0 Pre. & Clock							
	7	6	5	4	3	2	1	0
w	x	PRE		Clock Options f0 to f31 (all)				
	x	0x0		0x11				Res

PRE **Prescaler** (Table 29–3)

CO01C	Clock Out 0: Mux1 Clock							
	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

CO02C	Clock Out 0: Mux2 Clock							
	7	6	5	4	3	2	1	0
w	x	x	x	Clock Options f0 to f31 (all)				
	x	x	x	0x0				Res

CO1C	Clock Out 1: Pre. & Clock							
	7	6	5	4	3	2	1	0
w	x	PRE		Clock Options f0 to f31 (all)				
	x	0x0		0x11				Res

PRE **Prescaler** (Table 29–3)

29.3.8. LCD

LC	LCD Pre. & Clock							
	7	6	5	4	3	2	1	0
w	x	PRE		Clock Options f0 to f31 (all)				
	x	0x0		0x03				Res

PRE **Prescaler** (Table 29–3)

29.3.9. Stepper Motor and SPIs

SMC	SM, SPI0, SPI1 Pre. & SM Clock							
	7	6	5	4	3	2	1	0
w	x	PRE		Clock Options f0 to f31 (all)				
	x	0x0		0x0				Res

PRE **Prescaler** (Table 29–3)

The field PRE of register SMC defines the SPI0 and SPI1 prescaler setting too.

SP0C				SPI0 I/O & $F0_{SPI}$ Clock			
7	6	5	4	3	2	1	0
w SPI0OUT	SPI0IN	x	Clock Options f0 to f31 (all)				
0	0	x	0x0				Res

SPI0OUT **SPI0 Data Output Inverter**
w1: Inverted.
w0: Direct.

SPI0IN **SPI0 Data Input Inverter**
w1: Inverted.
w0: Direct.

The clock is pre scaled by SMC.PRE.

SP1C				SPI1 I/O & $F1_{SPI}$ Clock			
7	6	5	4	3	2	1	0
w SPI1OUT	SPI1IN	x	Clock Options f0 to f31 (all)				
0	0	x	0x0				Res

SPI1OUT **SPI1 Data Output Inverter**
w1: Inverted.
w0: Direct.

SPI1IN **SPI1 Data Input Inverter**
w1: Inverted.
w0: Direct.

The clock is pre scaled by SMC.PRE.

SP2C				$F2_{SPI}$ Clock			
7	6	5	4	3	2	1	0
w x	x	x	Clock Options f0 to f31 (all)				
x	x	x	0x0				Res

The clock is pre scaled by SMC.PRE.

29.3.10. Audio Module

AC				AM Clock			
7	6	5	4	3	2	1	0
w x	x	x	Clock Options f0 to f31 (all)				
x	x	x	0x0				Res

29.3.11. Port Multiplexers

PM				Port Mux			
7	6	5	4	3	2	1	0
w U15	CC4I	CACO	U20	U06	H7	H0	PINT
0	0	0	1	0	0	0	0 Res

U15 **U-Port 1.5 outputs**
w1: CO1.
w0: CO0Q.

CC4I **CAPCOM4-IN**
w1: Input from P0.0.
w0: Input from U5.3.

CACO **CAPCOM0, 1, 2-IN**
w1: Input from U4.1, U2.4, U2.2.
w0: Input from U3.2, U3.1, U3.0.

U06 **U-Port 0.6 outputs**
w1: CC3-OUT.
w0: T4-OUT.

U20 **U-Port 2.0 outputs**
w1: CAN0-TX on U4.2.
CAN0-RX on U4.3.
SCL0 on U2.0.
SDA0 on U2.1.
w0: CAN0-TX on U2.0 and U4.2.
CAN0-RX on U2.1.
SCL0, SDA0 not usable.

H7 **H-Port 7 outputs**
w1: PWM9, 8, 6, 4.
w0: SME.

H0 **H-Port 0 outputs**
w1: PWM7, 5, 3, 1.
w0: SMG.

PINT **Port interrupts**
w1: Input from P1.2 to 7.
w0: Input from U1.7, U1.6, U1.5, U0.7, U0.5, U0.4.

29.3.12. Clock Monitor

CM				Clock Monitor			
7	6	5	4	3	2	1	0
w x	WCM	x	x	x	x	x	x
x	0	x	x	x	x	x	x Res

WCM **Watchdog, Clock and Supply Monitor**
w1: Clock & Supply: Always active.
Watchdog: Always active.
w0: Clock & Supply: deactivatable by SW.
Watchdog: activatable by SW.

29.3.13. UARTs

UA0				UART0 I/O			
7	6	5	4	3	2	1	0
w U0TX	U0RX	x	x	x	x	x	x
0	0	x	x	x	x	x	x Res

U0TX **UART0 Tx Output**
w1: Inverted.
w0: Direct.

U0RX **UART0 Rx Input**
w1: Inverted.
w0: Direct.

UA1	UART1 I/O							
	7	6	5	4	3	2	1	0
w	U1TX	U1RX	x	x	x	x	x	x
	0	0	x	x	x	x	x	x

Res

U1TX **UART1 Tx Output**
w1: Inverted.
w0: Direct.

U1RX **UART1 Rx Input**
w1: Inverted.
w0: Direct.

30. Register Cross Reference Table

30.1. 8 Bit I/O Region

Table 30–1: Base address 0x00F80000

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0xFFC					5 CAN reserved	CAN RAM
0x600						
0x5FC					CAN 2	
0x400						
0x3FC					CAN 1	
0x200						
0x1FC					CAN 0	
0x000						

Table 30–2: Base address 0x00F81000

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x1FC					5 CAN reserved	CAN register
0x0C0						
0x0BC					CAN2	
0x094						
0x090				CTIM		
0x08C	CTIM	REC	TEC	OCR		
0x088	ICR	BT3	BT2	BT1		
0x084	IDM					
0x080	IDX	ESTR	STR	CTR		
0x07C					CAN1	
0x054						
0x050				CTIM		
0x04C	CTIM	REC	TEC	OCR		
0x048	ICR	BT3	BT2	BT1		
0x044	IDM					
0x040	IDX	ESTR	STR	CTR		
0x03C					CAN0	
0x014						
0x010				CTIM		
0x00C	CTIM	REC	TEC	OCR		
0x008	ICR	BT3	BT2	BT1		
0x004	IDM					
0x000	IDX	ESTR	STR	CTR		

Table 30–3: Base address 0x00F90000 (formerly 1F00)

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC	TST2	TST1	TST3	TST4		Test
0x0F8	TST5		TSTAD3	TSTAD2		
0x0F4	DGRTMA	DGTD	DGS1TA	DGTL		DIGITBus
0x0F0	DGRTMD	DGS0	DGC1	DGC0		
0x0EC					64 byte	
0x0B0						
0x0AC				ANAA		ADC
0x0A8			AD1	AD0		
0x0A4		UA0IF	UA0CA	UA0IM		UART0
0x0A0	UA0BR1	UA0BR0	UA0C	UA0D		
0x09C					32 byte	
0x080						
0x07C			CCC0H	CCC0L		CAPCOM0
0x078	CC3H	CC3L	CC3I	CC3M	CC3	
0x074	CC2H	CC2L	CC2I	CC2M	CC2	
0x070	CC1H	CC1L	CC1I	CC1M	CC1	
0x06C	CC0H	CC0L	CC0I	CC0M	CC0	
0x068					8 byte	
0x064						
0x060				CSW1		Core Logic
0x05C			SMVCMP	SMVCOS		Stepper Motor Module VDO
0x058	SMVSIN	SMVC				
0x054	TIM4	TIM3	TIM2	TIM1		Timer
0x050						
0x04C	TIM0H	TIM0L			Timer0	
0x048			CCC1H	CCC1L		CAPCOM1
0x044	CC5H	CC5L	CC5I	CC5M	CC5	
0x040	CC4H	CC4L	CC4I	CC4M	CC4	
0x03C					16 byte	
0x030						
0x02C	AMDEC	AMF	AMAS	AMPRE		Audio Module
0x028	IRPM1	IRPM0				Port Interrupt
0x024					8 byte	
0x020						
0x01C		UA1IF	UA1CA	UA1IM		UART1
0x018	UA1BR1	UA1BR0	UA1C	UA1D		
0x014				CO0SEL		Core Logic
0x010	SPI1M	SPI1D	SPI0M	SPI0D		SPI
0x00C	SR1					Core Logic
0x008	SR0					
0x004				ANAU		
0x000				CSW0		

Table 30–4: Base address 0x00F90100 (formerly 1E00)

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					16 byte	HW Options
0x0F0						
0x0EC			UA1	UA0		
0x0E8		CM	PM			
0x0E4						
0x0E0						
0x0DC	P7P	P7C	P5P	P5C		
0x0D8	P3P	P3C	P1P	P1C		
0x0D4	P11P	P11C	P9P	P9C		
0x0D0	SP2C	SP1C	SP0C	SMC		
0x0CC	PF0C	AC	LC	DC		
0x0C8	C1C	C0C	CO1C	DMAC		
0x0C4	CO02C	CO01C	CO00C	T4C		
0x0C0	T3C	T2C	T1C	T0C		
0x0BC					96 byte	
0x060						
0x05C						PFM
0x054						
0x050	PFM0					
0x04C	PWMC					PWM
0x048	PWM11	PWM10	PWM9	PWM8		
0x044	PWM7	PWM6	PWM5	PWM4		
0x040	PWM3	PWM2	PWM1	PWM0		
0x03C					32 byte	
0x020						
0x01C					I2C1	I2C
0x018	I2CM1					
0x014	I2CRS1	I2CRD1	I2CWP11	I2CWP01		
0x010	I2CWD11	I2CWD01	I2CWS11	I2CWS01		
0x00C					I2C0	
0x008	I2CM0					
0x004	I2CRS0	I2CRD0	I2CWP10	I2CWP00		
0x000	I2CWD10	I2CWD00	I2CWS10	I2CWS00		

Table 30–5: Base address 0x00F90400

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC				HxPIN	H-Port7	H-Ports
0x0F8	HxLVL	HxNS	HxTRI	HxD		
0x0F4				HxPIN	H-Port6	
0x0F0	HxLVL	HxNS	HxTRI	HxD		
0x0EC				HxPIN	H-Port5	
0x0E8	HxLVL	HxNS	HxTRI	HxD		
0x0E4				HxPIN	H-Port4	
0x0E0	HxLVL	HxNS	HxTRI	HxD		
0x0DC				HxPIN	H-Port3	
0x0D8	HxLVL	HxNS	HxTRI	HxD		
0x0D4				HxPIN	H-Port2	
0x0D0	HxLVL	HxNS	HxTRI	HxD		
0x0CC				HxPIN	H-Port1	
0x0C8	HxLVL	HxNS	HxTRI	HxD		
0x0C4				HxPIN	H-Port0	
0x0C0	HxLVL	HxNS	HxTRI	HxD		
0x0BC						P-Ports
0x0B8	P2LVL		P2IE	P2PIN	P-Port 2	
0x0B4	P1LVL		P1IE	P1PIN	P-Port1	
0x0B0	P0LVL		P0IE	P0PIN	P-Port 0	
0x0AC					reserved	U-Ports
0x090						
0x084	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 8	
0x080	UxDPM	UxNS	UxTRI	UxD		
0x074	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 7	
0x070	UxDPM	UxNS	UxTRI	UxD		
0x064	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 6	
0x060	UxDPM	UxNS	UxTRI	UxD		
0x054	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 5	
0x050	UxDPM	UxNS	UxTRI	UxD		
0x044	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 4	
0x040	UxDPM	UxNS	UxTRI	UxD		
0x034	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 3	
0x030	UxDPM	UxNS	UxTRI	UxD		
0x024	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 2	
0x020	UxDPM	UxNS	UxTRI	UxD		
0x014	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 1	
0x010	UxDPM	UxNS	UxTRI	UxD		
0x004	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 0	
0x000	UxDPM	UxNS	UxTRI	UxD		

Table 30–6: Base address 0x00F90500

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					180 Bytes	reserved
0x050						
0x04C					reserved	GBus
0x048						
0x044				GC		
0x040				GD		
0x03C					reserved	Core Logic
0x030						
0x02C				WSR	Clock, PLL, ERM	
0x028				IOC		
0x024	ERMC					
0x020				PLLC		
0x01C					reserved	LCD
0x014						
0x010				ULCDLD		
0x00C						reserved for Patch
0x008						
0x004						
0x000						

30.2. 32 Bit I/O Region

Table 30–7: Base address 0x00FFFD00

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					252 bytes reserved	Core Logic
0x004						
0x000	CR				Control Register	

Table 30–8: Base address 0x00FFFE00

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					rsvd Channel 4 to 31	DMA
0x020						
0x018			DC3M		Channel 3	
0x010			DC2M		Channel 2	
0x008			DC1M		Channel 1	
0x004				DST	Control	
0x000	DVB					

Table 30–9: Base address 0x00FFFF00

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					12 bytes reserved	IRQ and FIQ Interrupt Controller
0x0F4						
0x0F0			CRF	PRF	FIQ registers	
0x0EC					40 bytes reserved	
0x0C8						
0x0C4	VTB				IRQ registers	
0x0C0	PESRC	PEPRIO	AFP	CRI		
0x0BC					128 bytes reserved	
0x040						
0x03C					Interrupt source nodes	
0x028						
0x024	ISN39	ISN38	ISN37	ISN36		
:	:	:	:	:		
0x004	ISN7	ISN6	ISN5	ISN4		
0x000	ISN3	ISN2	ISN1	ISN0		

31. Register Quick Reference

Due to HW constraints some multi-byte registers must be accessed byte by byte only. Postfixes (_m_n) may be attached to such register mnemonics if necessary, where “m” stands for the access size in bit (m = 8 or 16) and “n” stands for the byte or half word offset (n = 0, 1, 2, 3).

The I/O area is organized in little endian format, thus the LSB, independent of the flag CR.ENDIAN setting, is always stored at the low address.

Table 31–1: Possible Postfixes

Postfix	Access Size	Byte Offset
_8_0	Byte	Byte 0 (LSB)
_8_1		Byte 1
_8_2		Byte 2
_8_3		Byte 3 (MSB)
_16_0	Half word	Low half word
_16_1		High half word

Table 31–2: Analog Section (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration	Section
			7 6 5 4 3 2 1 0	
AD0	ADC Register 0	0x0A8	r: EOC | x | x | x | x | TEST | AN1 | AN0 w: TSAMP | REF | CHANNEL 0 0 0 0 0 0 0 0 Res	13.7.
AD1	ADC Register 1	0x0A9	r: AN9 | AN8 | AN7 | AN6 | AN5 | AN4 | AN3 | AN2 w: x | x | x | x | x | x | x | BUF 0 Res	
ANAA	Analog AVDD Register	0x0AC	r/w: EP06 | P06 | WAIT | x | x | x | x | BVE 0 0 Res	

Table 31–3: Analog Input Ports (Base addr. 0xF90400)

Mnemonic	Register Name	Offs.	Register Configuration	Section
			7 6 5 4 3 2 1 0	
P0PIN	Port x Pin Register	0x0B0	r: P7 P6 P5 P4 P3 P2 P1 P0 / 1 1 1 1 1 1 1 1 Res	12.1.
P1PIN		0x0B4		
P2PIN		0x0B8		
P0IE	Port x Input Enable Register	0x0B1	r/w: I7 I6 I5 I4 I3 I2 I1 I0 / 0 0 0 0 0 0 0 0 Res	
P1IE		0x0B5		
P2IE		0x0B9		
P0LVL	Port x Level Register	0x0B3	r/w: A7 A6 A5 A4 A3 A2 A1 A0 / 0 0 0 0 0 0 0 0 Res	
P1LVL		0x0B7		
P2LVL		0x0BB		

Table 31–4: Audio Module (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration	Section
			7 6 5 4 3 2 1 0	
AMPRE	Audio Module Prescaler	0x02C	w: Prescale Value / 1 1 1 1 1 1 1 1 Res	28.2.
AMAS	Audio Module Amplitude & Status Register	0x02D	w: Initial Amplitude / r: AMA x x x x x x x / 0 x x x x x x x Res	
AMF	Audio Module Frequency Register	0x02E	w: x Sound Frequency / - 0 0 0 0 0 0 0 Res	
AMDEC	Audio Module Decrement Register	0x02F	w: AMMCA x x x x GDF / 0 - - - - 0 0 0 Res	

Table 31–5: Capture-Compare-Unit 0 (Base addr. 0xF90000)

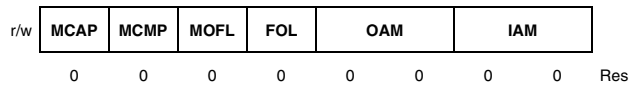
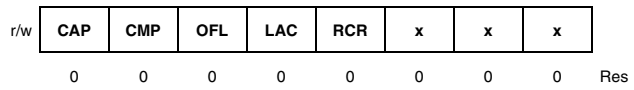
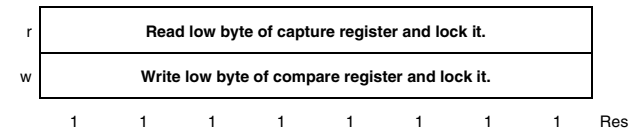
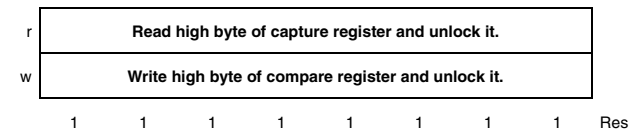
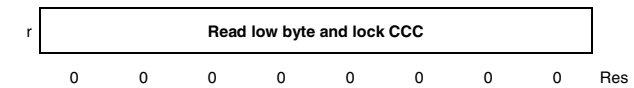
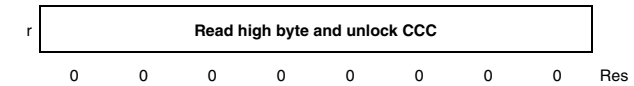
Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
CC0M	CAPCOM 0 Mode Register	0x06C		17.2.
CC1M		0x070		
CC2M		0x074		
CC3M		0x078		
CC0I	CAPCOM 0 Interrupt Register	0x06D		
CC1I		0x071		
CC2I		0x075		
CC3I		0x079		
CC0L	CAPCOM 0 Capture/ Compare Register low byte	0x06E		
CC1L		0x072		
CC2L		0x076		
CC3L		0x07A		
CC0H	CAPCOM 0 Capture/ Compare Register high byte	0x06F		
CC1H		0x073		
CC2H		0x077		
CC3H		0x07B		
CCC0L	CAPCOM Counter 0 low byte	0x07C		
CCC0H	CAPCOM Counter 0 high byte	0x07D		

Table 31–6: Capture-Compare-Unit 1 (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration	Section
			7 6 5 4 3 2 1 0	
CC4M CC5M	CAPCOM Mode Register	0x040 0x044	r/w: MCAP | MCMP | MOFL | FOL | OAM | IAM 0 0 0 0 0 0 0 0 Res	17.2.
CC4I CC5I	CAPCOM Interrupt Register	0x041 0x045	r/w: CAP | CMP | OFL | LAC | RCR | x | x | x 0 0 0 0 0 0 0 0 Res	
CC4L CC5L	CAPCOM Capture/ Compare Register low byte	0x042 0x046	r: Read low byte of capture register and lock it. w: Write low byte of compare register and lock it. 1 1 1 1 1 1 1 1 Res	
CC4H CC5H	CAPCOM Capture/ Compare Register high byte	0x043 0x047	r: Read high byte of capture register and unlock it. w: Write high byte of compare register and unlock it. 1 1 1 1 1 1 1 1 Res	
CCC1L	CAPCOM Counter 1 low byte	0x048	r: Read low byte and lock CCC 0 0 0 0 0 0 0 0 Res	
CCC1H	CAPCOM Counter 1 high byte	0x049	r: Read high byte and unlock CCC 0 0 0 0 0 0 0 0 Res	

Table 31–7: Controller Area Network Registers (Base addr. 0xF81000)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
CAN0CTR	Control Register	0x000	r/w HLT SLP GRSC EIE GRIE GTIE rsvd rsvd 1 0 0 0 0 0 x x Res	25.2.
CAN1CTR		0x040		
CAN2CTR		0x080		
CAN0STR	Status Register	0x001	r HACK BOFF EPAS ERS rsvd rsvd rsvd rsvd 1 0 0 0 x x x x Res	
CAN1STR		0x041		
CAN2STR		0x081		
CAN0ESTR	Error Status Register	0x002	r/w GDM CTOV ECNT BIT STF CRC FRM ACK 0 0 0 0 0 0 0 0 Res	
CAN1ESTR		0x042		
CAN2ESTR		0x082		
CAN0IDX	Interrupt Index Register	0x003	r/w Interrupt Index 1 1 1 1 1 1 1 1 Res	
CAN1IDX		0x043		
CAN2IDX		0x083		
CAN0IDM	Identifier Mask Register	0x004	r/w Identifier Mask Bits 4 to 0 x x x 3 r/w Identifier Mask Bits 12 to 5 2 r/w Identifier Mask Bits 20 to 13 1 r/w Identifier Mask Bits 28 to 21 0 0 0 0 0 0 0 0 0 Res	
CAN1IDM		0x044		
CAN2IDM		0x084		
CAN0BT1	Bit Timing Register 1	0x008	r/w MSAM SYN BPR 0 0 0 0 0 0 0 0 Res	
CAN1BT1		0x048		
CAN2BT1		0x088		
CAN0BT2	Bit Timing Register 2	0x009	r/w rsvd TSEG2 TSEG1 0 0 0 0 0 0 0 0 Res	
CAN1BT2		0x049		
CAN2BT2		0x089		
CAN0BT3	Bit Timing Register 3	0x00A	r/w rsvd rsvd rsvd rsvd rsvd SJW x x x x x 0 0 0 Res	
CAN1BT3		0x04A		
CAN2BT3		0x08A		
CAN0ICR	Input Control Register	0x00B	r/w rsvd rsvd rsvd rsvd rsvd XREF REF1 REF0 x x x x x 0 0 0 Res	
CAN1ICR		0x04B		
CAN2ICR		0x08B		

Table 31–7: Controller Area Network Registers (Base addr. 0xF81000)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
CAN0OCR	Output Control Register	0x00C	r/w: rsvd rsvd rsvd rsvd rsvd rsvd rsvd ITX x x x x x x x 0 Res	25.2.
CAN1OCR		0x04C		
CAN2OCR		0x08C		
CAN0TEC	Transmit Error Counter	0x00D	r: Counter Bit 7 to 0 0 0 0 0 0 0 0 0 Res	
CAN1TEC		0x04D		
CAN2TEC		0x08D		
CAN0REC	Receive Error Counter	0x00E	r: x Counter Bit 6 to 0 x 0 0 0 0 0 0 0 Res	
CAN1REC		0x04E		
CAN2REC		0x08E		
CAN0CTIM	Capture Timer	0x00F	r: Timer Bit 15 to 8 1 r: Timer Bit 7 to 0 0 0 0 0 0 0 0 0 0 Res	
CAN1CTIM		0x04F		
CAN2CTIM		0x08F		

Table 31–8: Core Logic 32 Bit (Base addr. 0xFFFD00)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
CR	Control Register	0x000	r/w: x x x x x x x x 3 r/w: STPCLK RESLNG x x x TSTTOG x PSA 2 r/w: EB2 TFT TETM EB1 EBW EASY MFM 1 r/w: JTAG ENDIAN MAP IBOOT IROM IRAM ICPU 0 Value of memory location 0x20 to 0x23 Res	6.1.

Table 31–9: Core Logic 8 Bit (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
CSW0	Clock, Supply and Watchdog Register 0	0x000	w: FHR x x x x x x CMA 0 x x x x x x 1 Res	6.
ANAU	Analog UVDD Register	0x004	r/w: EAL x LS x x FVE VE 0 0 0 0 0	
SR0	Standby Register 0	0x008	r/w: I2C1 I2C0 x x x x CAN2 CAN1 3 r/w: TIM2 TIM3 TIM4 UART1 x DGB CCC1 x 2 r/w: LCD x PSLW UART0 ADC x TIM1 XTAL 1 r/w: SM x x x SPI1 CAN0 CCC0 SPI0 0 0x00000100 Res	
SR1	Standby Register 1	0x00C	r/w: x x x x x x x x 3 r/w: x x x x x x x x 2 r/w: x PFM0 PWM11 PWM9 PWM7 PWM5 PWM3 PWM1 1 r/w: IRQ FIQ x x x CPUM 0 0x00000001 Res	
CO0SEL	Clock Out 0 Selection	0x014	w: x x x x x x CO01 CO00 x x x x x x 0 0 Res	
CSW1	Clock, Supply and Watchdog Register 1	0x060	w: Watchdog Time and Trigger Value 1 1 1 1 1 1 1 1 Res r: TST x x FHR CLM PIN POR WDRES - - - 0 0 0 0 0 Res	

Table 31–10: Core Logic 8 Bit (Base addr. 0xF90500)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
PLLC	PLL Control	0x020	r/w: ACT | LCK | PLLM | x | PMF x x x x 0 0 0 0 Res	6.
ERMC	ERM Control	0x024	r/w: TSEL 3 r/w: x x x x x x x x 2 r/w: EOM | x | x | TOL 1 r/w: INPH | x | SUP 0 0x00000000 Res	
IOC	I/O Control	0x028	w: x x x x x | IOP x x x x x 0 0 0 Res	
WSR	Wait State Register	0x02C	w: NWS | SWS 0x00 Res	

Table 31–11: DIGITbus (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration	Section
			7 6 5 4 3 2 1 0	
DGC0	Control Register 0	0x0F0	r/w: RUN | GBC | ACT | RXO | X | PSC 2 to 0 0 0 0 0 x 0 0 0 Res	27.3.
DGC1	Control Register 1	0x0F1	r/w: INTE | ENEM | ENOF | x | PHASE 0 0 0 x 0 0 0 0 Res	
DGS0	Status Register 0	0x0F2	w: x | x | x | TGV | PV | ERR | x | ARB r: RDL | NEM | NOF x 0 1 0 0 0 x 0 Res	
DGRTMD	Rx Length & Tx More Data Register	0x0F3	w: Transmit More Data r: RDL | NEM | FTYP | EOFLD | x | LEN2 to 0 0 0 x x x x x x Res	
DGTL	Tx Length Register	0x0F4	w: x | FLUSH | x | x | x | LEN2 to 0 x 0 x x x 0 0 0 Res r: BUSY | EMPTY | x | x | x | x | x | x 0 1 x x x x x x Res	
DGS1TA	Status 1 & Tx Address Register	0x0F5	w: Transmit Address r: STATE | PW5 to 0 0 1 0 0 0 0 0 0 Res	
DGTD	Tx Data Register	0x0F6	w: Transmit Data x x x x x x x x Res	
DGRTMA	Rx Field & Tx More Address Register	0x0F7	w: Transmit More Address r: Receive Field x x x x x x x x Res	

Table 31–12: DMA (Base addr. 0xFFFE00)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
DVB	DMA Vector Base	0x000	r/w 0 0 0 0 0 0 0 0 3 r/w A23 to A16 2 r/w A15 to A8 1 r/w A7 0 0 0 0 0 0 0 0 0x0000 Res	20.2.
DST	DMA Status	0x004	r/w DE x x SRC 0 0x00 Res	
DC1M	DMA Channel x Mode	0x008	r/w P DMAT TRIG 1 r/w EN x x x BYP DIR MAS 0 0x0000 Res	
DC2M		0x010		
DC3M		0x018		

Table 31–13: FIQ Interrupt Logic (Base addr. 0xFFFF00)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
PRF	Pending Register FIQ	0x0F0	r/w x x x x x x x P x x x x x x x 0 Res	10.2.
CRF	Control Register FIQ	0x0F1	r/w GE x x x SEL 0 x x x 0 0 0 0 Res	

Table 31–14: Graphic Bus Interface (Base addr. 0xF90500)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
GD	Graphic Bus Data Register	0x040	r/w Data 0 0x00 Res	21.2.
GC	Graphic Bus Control Register	0x044	r/w TIM E BSY SEQ DTA 0 0x00 Res	

Table 31–15: Hardware Options Registers (Base addr. 0xF90100)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
T0C	Timer 0 Clock	0x0C0	w: x x x Clock Options f1 to f31 x x x 0x01 Res	29.3.
T1C	Timer 1 to 4 Clock	0x0C1	w: x x x Clock Options f0 to f31 (all) x x x 0x0 Res	
T2C		0x0C2		
T3C		0x0C3		
T4C		0x0C4		
CO00C	Clock Out0: Mux0 Pre. & Clock	0x0C5	w: x PRE Clock Options f0 to f31 (all) x 0x0 0x11 Res	
CO01C	Clock Out0: Mux1 to Mux3 Clock	0x0C6	w: x x x Clock Options f0 to f31 (all) x x x 0x0 Res	
CO02C		0x0C7		
DMAC	DMA Timer Clock	0x0C8	w: x x x Clock Options f0 to f31 (all) x x x 0x0 Res	
CO1C	Clock Out1: Pre. & Clock	0x0C9	w: x PRE Clock Options f0 to f31 (all) x 0x0 0x11 Res	
C0C	CAPCOM Counter Clocks	0x0CA	w: x x x Clock Options f0 to f31 (all) x x x 0x0 Res	
C1C		0x0CB		
DC	DIGITbus Clock	0x0CC		
LC	LCD Pre. & Clock	0x0CD	w: x PRE Clock Options f0 to f31 (all) x 0x0 0x03 Res	
AC	AM Clock	0x0CE	w: x x x Clock Options f0 to f31 (all) x x x 0x0 Res	
PF0C	PFM 0 Clock	0x0CF	w: x x x Clock Options f0 to f31 (all) x x x 0x0 Res	
SMC	SM, SPI0, SPI1 Pre. & SM Clock	0x0D0	w: x PRE Clock Options f0 to f31 (all) x 0x0 0x0 Res	
SP0C	SPI0 I/O & $F0_{SPI}$ Clock	0x0D1	w: SPI0OUT SPI0IN x Clock Options f0 to f31 (all) 0 0 x 0x0 Res	

Table 31–15: Hardware Options Registers (Base addr. 0xF90100)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
SP1C	SPI1 I/O & $F1_{SPI}$ Clock	0x0D2	w: SPI1OUT | SPI1IN | x | Clock Options f0 to f31 (all) 0 0 x 0x0 Res	29.3.
SP2C	$F2_{SPI}$ Clock	0x0D3	w: x | x | x | Clock Options f0 to f31 (all) x x x 0x0 Res	
P9C	PWM Clock	0x0D4	w: x | x | x | Clock Options f0 to f31 (all) x x x 0x0 Res	
P11C		0x0D6		
P1C		0x0D8		
P3C		0x0DA		
P5C		0x0DC		
P7C		0x0DE		
P9P	PWM Period	0x0D5	w: x | x | x | Clock Options f0 to f31 (all) x x x 0x08 Res	
P11P		0x0D7		
P1P		0x0D9		
P3P		0x0DB		
P5P		0x0DD		
P7P		0x0DF		
PM	Port Multiplexer	0x0E9	w: U15 | CC4I | CACO | U20 | U06 | H7 | H0 | PINT 0 0 0 1 0 0 0 0 Res	
CM	Clock Monitor	0x0EA	w: x | WCM | x | x | x | x | x | x x 0 x x x x x x Res	
UA0	UARTs	0x0EC	w: U0TX | U0RX | x | x | x | x | x | x 0 0 x x x x x x Res	
UA1		0x0ED	w: U1TX | U1RX | x | x | x | x | x | x 0 0 x x x x x x Res	

Table 31–16: High Current Ports (Base addr. 0xF90400)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
H0D	High Current Port Data Register	0x0C0	r/w: x x x x D3 D2 D1 D0 x x x x 0 0 0 0 Res	12.5.
H1D		0x0C8		
H2D		0x0D0		
H3D		0x0D8		
H4D		0x0E0		
H5D		0x0E8		
H6D		0x0F0		
H7D		0x0F8		
H0TRI	High Current Port Tristate Register	0x0C1	r/w: x x x x T3 T2 T1 T0 x x x x 0 0 0 0 Res	
H1TRI		0x0C9		
H2TRI		0x0D1		
H3TRI		0x0D9		
H4TRI		0x0E1		
H5TRI		0x0E9		
H6TRI		0x0F1		
H7TRI		0x0F9		
H0NS	High Current Port Normal/Special Register	0x0C2	r/w: x x x x S3 S2 S1 S0 x x x x 0 0 0 0 Res	
H1NS		0x0CA		
H2NS		0x0D2		
H3NS		0x0DA		
H4NS		0x0E2		
H5NS		0x0EA		
H6NS		0x0F2		
H7NS		0x0FA		

Table 31–16: High Current Ports (Base addr. 0xF90400)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
H0LVL	High Current Port Level Register	0x0C3	r/w: x x x x A3 A2 A1 A0 x x x x 0 0 0 0 Res	12.5.
H1LVL		0x0CB		
H2LVL		0x0D3		
H3LVL		0x0DB		
H4LVL		0x0E3		
H5LVL		0x0EB		
H6LVL		0x0F3		
H7LVL		0x0FB		
H0PIN	High Current Port Pin Register	0x0C4	r: x x x x P3 P2 P1 P0 x x x x 0 0 0 0 Res	
H1PIN		0x0CC		
H2PIN		0x0D4		
H3PIN		0x0DC		
H4PIN		0x0E4		
H5PIN		0x0EC		
H6PIN		0x0F4		
H7PIN		0x0FC		

Table 31–17: I2C-Bus Master Interfaces (Base addr. 0xF90100)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
I2CWS00	I2C Write Start Register 0	0x000	w: I2C Address; 0x00; Res	24.2.
I2CWS01		0x010		
I2CWS10	I2C Write Start Register 1	0x001	w: I2C Address; 0x00; Res	
I2CWS11		0x011		
I2CWD00	I2C Write Data Register 0	0x002	w: I2C Data; 0x00; Res	
I2CWD01		0x012		
I2CWD10	I2C Write Data Register 1	0x003	w: I2C Data; 0x00; Res	
I2CWD11		0x013		
I2CWP00	I2C Write Stop Register 0	0x004	w: I2C Data; 0x00; Res	
I2CWP01		0x014		
I2CWP10	I2C Write Stop Register 1	0x005	w: I2C Data; 0x00; Res	
I2CWP11		0x015		
I2CRD0	I2C Read Data Register	0x006	r: I2C Data; 0x00; Res	
I2CRD1		0x016		
I2CRS0	I2C Read Status Register	0x007	r: x | OACK | AACK | DACK | BUSY | WFH | RFE | x; 0 0 0 0 0 0 0 0; Res	
I2CRS1		0x017		
I2CM0	I2C Mode Register	0x00B	w: DGL | SPEED; 1 0x02; Res	
I2CM1		0x01B		

Table 31–18: Interrupt Controller Unit (Base addr. 0xFFFF00)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
ISN0	Interrupt Source Node Register 0	0x000	r/w: M P E x PRIO 0 x 0 x 0 0 0 0 Res	9.3.
:	:	:		
ISN39	Interrupt Source Node Register 39	0x027		
CRI	Control Register IRQ	0x0C0	r/w: GE TE x x x x x x 0 0 x x x x x x Res	
AFP	Actual and Forced Priority Register	0x0C1	r/w: APRIO FPRIO 0 0 0 0 0 0 0 0 Res	
PEPRIO	Priority Encoder Priority output	0x0C2	r: x x x x Priority x x x x 0 0 0 0 Res	
PESRC	Priority Encoder Source output	0x0C3	r: x x Source x x 0 0 0 0 0 0 Res	
VTB	Vector Table Base	0x0C4	r/w: 0 0 0 0 0 0 0 0 3 r/w: Address bit 23 to 16 2 r/w: Address bit 15 to 9 0 1 r/w: 0 0 0 0 0 0 0 0 0 0x00000000 Res	

Table 31–19: LCD (Base addr. 0xF90500)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
ULCDLD	Universal Port LCD Load Register	0x010	w: LCDSLV x x x x x x x 0 0 0 0 0 0 0 0 Res	19.2.

Table 31–20: Port Interrupts (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
IRPM0	Interrupt Port Mode Register 0	0x02A	r/w: PIT3 PIT2 PIT1 PIT0 0 0 0 0 0 0 0 0 Res	11.
IRPM1	Interrupt Port Mode Register 1	0x02B	r/w: x x x x PIT5 PIT4 x x x x 0 0 0 0 Res	

Table 31–21: Pulse Frequency Modulator (Base addr. 0xF90100)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
PFM0	Pulse Width and Period Length Register	0x050	w: INV x x x x x x x 3 w: Pulse Width 2 w: Period Length (High Byte) 1 w: Period Length (Low Byte) 0 0x00 Res	16.2.

Table 31–22: Pulse Width Modulator (Base addr. 0xF90100)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
PWM0	PWM Register	0x040	w: Pulse width value 0 0 0 0 0 0 0 0 Res	15.2.
PWM1		0x041		
PWM2		0x042		
PWM3		0x043		
PWM4		0x044		
PWM5		0x045		
PWM6		0x046		
PWM7		0x047		
PWM8		0x048		
PWM9		0x049		
PWM10		0x04A		
PWM11		0x04B		
PWMC	PWM Control Register	0x04F	w: x | x | P1611 | P169 | P167 | P165 | P163 | P161 x x 0 0 0 0 0 0 Res	

Table 31–23: Serial Synchronous Peripheral Interfaces (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
SPI0D	SPI Data Register	0x010	r/w: Bit 7 to 0 of Rx/Tx Data 0 0 0 0 0 0 0 0 Res	22.2.
SPI1D		0x012		
SPI0M	SPI Mode Register	0x011	r/w: BIT8 | LEN9 | RXSEL | INTERN | SCLK | CSF 0 0 0 0 0 0 0 0 Res	
SPI1M		0x013		

Table 31–24: Stepper Motor VDO (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
SMVC	Stepper Motor VDO, Control Register	0x05A	w: x x SEL x QUAD x x 0 0 0 x 0 0 Res	18.2.
SMVSIN	Stepper Motor VDO, Sine Register	0x05B	r: x x x x x x x BUSY w: 8bit Sine Value 0 0 0 0 0 0 0 0 Res	
SMVCOS	Stepper Motor VDO, Cosine Register	0x05C	w: 8bit Cosine Value 0 0 0 0 0 0 0 0 Res	
SMVCMP	Stepper Motor VDO, Back-Up Comparator Register	0x05D	r/w: x ACRF ACRD ACRB ACRG ACRE ACRC ACRA x 0 0 0 0 0 0 0 Res	

Table 31–25: Test Registers (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
TSTAD2	Test Register AD2	0x0F8	w: For testing purposes only 0 0 0 0 0 0 0 0 Res	6.5.
TSTAD3	Test Register AD3	0x0F9		
TST5	Test Register 5	0x0FB		
TST4	Test Register 4	0x0FC		
TST3	Test Register 3	0x0FD		
TST1	Test Register 1	0x0FE		
TST2	Test Register 2	0x0FF		

Table 31–26: Timer (Base addr. 0xF90000)

Mnemonic	Register Name	Offs	Register Configuration 7 6 5 4 3 2 1 0	Section
TIM0L	Timer 0 low byte	0x04E	r: Read low byte of down-counter and latch high byte w: Write low byte of reload value and reload down-counter 1 1 1 1 1 1 1 1 Res	14.
TIM0H	Timer 0 high byte	0x04F	r: Latched high byte of down-counter w: High byte of reload value 1 1 1 1 1 1 1 1 Res	
TIM1	Timer 1 Register	0x054	w: Reload value 0 0 0 0 0 0 0 0 Res	
TIM2	Timer 2 Register	0x055		
TIM3	Timer 3 Register	0x056		
TIM4	Timer 4 Register	0x057		

Table 31–27: Universal Asynchronous Receiver Transmitters (Base addr. 0xF90000)

Mnemonic	Register Name	Offs.	Register Configuration	Section
			7 6 5 4 3 2 1 0	
UA0D UA1D	UART Data Register	0x0A0 0x018	r: Receive register w: Transmit register x x x x x x x x Res	23.3.
UA0C UA1C	UART Control and Status Register	0x0A1 0x019	r: RBUSY BRKD FRER OVRR PAER EMPTY FULL TBUSY 0 x x 0 x 1 0 0 Res w: x x x x STPB ODD PAR LEN x x x x 0 0 0 0 Res	
UA0BR0 UA1BR0	UART Baudrate Register low byte	0x0A2 0x01A	w: Bit 7 to 0 of Baud Rate 0 0 0 0 0 0 0 0 Res	
UA0BR1 UA1BR1	UART Baudrate Register high byte	0x0A3 0x01B	w: x x x Bit 12 to 8 of Baud Rate - - - 0 0 0 0 0 Res	
UA0IM UA1IM	UART Interrupt Mask Register	0x0A4 0x01C	w: x x x x x ADR BRK RCVD - - - - - 0 0 0 Res	
UA0CA UA1CA	UART Compare Address Register	0x0A5 0x01D	w: Bit 7 to 0 of address 0 0 0 0 0 0 0 0 Res	
UA0IF UA1IF	UART Interrupt Flag Register	0x0A6 0x01E	r: Test Test Test Test Test ADR BRK RCVD - - - - - x 0 0 Res	

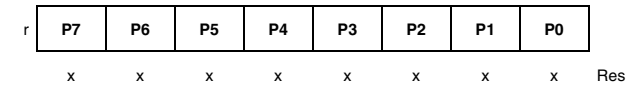
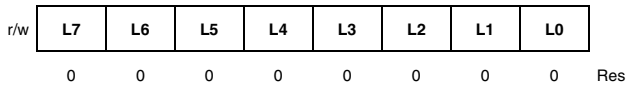
Table 31–28: Universal Ports (Base addr. 0xF90400)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
U0D	Universal Port Data/ Segment 0 Register	0x000	r/w D7 D6 D5 D4 D3 D2 D1 D0 Port r/w SG7_0 SG6_0 SG5_0 SG4_0 SG3_0 SG2_0 SG1_0 SG0_0 LCD 0 0 0 0 0 0 0 0 Res	12.3.
U1D		0x010		
U2D		0x020		
U3D		0x030		
U4D		0x040		
U5D		0x050		
U6D		0x060		
U7D		0x070		
U8D		0x080		
U0TRI	Universal Port Tristate/Segment 1 Register	0x001	r/w T7 T6 T5 T4 T3 T2 T1 T0 Port r/w SG7_1 SG6_1 SG5_1 SG4_1 SG3_1 SG2_1 SG1_1 SG0_1 LCD 1 1 1 1 1 1 1 1 Res	
U1TRI		0x011		
U2TRI		0x021		
U3TRI		0x031		
U4TRI		0x041		
U5TRI		0x051		
U6TRI		0x061		
U7TRI		0x071		
U8TRI		0x081		
U0NS	Universal Port Normal-Special/Segment 2 Register	0x002	r/w S7 S6 S5 S4 S3 S2 S1 S0 Port r/w SG7_2 SG6_2 SG5_2 SG4_2 SG3_2 SG2_2 SG1_2 SG0_2 LCD 0 0 0 0 0 0 0 0 Res	
U1NS		0x012		
U2NS		0x022		
U3NS		0x032		
U4NS		0x042		
U5NS		0x052		
U6NS		0x062		
U7NS		0x072		
U8NS		0x082		

Table 31–28: Universal Ports (Base addr. 0xF90400)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
U0DPM	Universal Port Double Pull-Down Mode/ Segment 3 Register	0x003	r/w D7 D6 D5 D4 D3 D2 D1 D0 Port r/w SG7_3 SG6_3 SG5_3 SG4_3 SG3_3 SG2_3 SG1_3 SG0_3 LCD 0 0 0 0 0 0 0 0 Res	12.3.
U1DPM		0x013		
U2DPM		0x023		
U3DPM		0x033		
U4DPM		0x043		
U5DPM		0x053		
U6DPM		0x063		
U7DPM		0x073		
U8DPM		0x083		
U0SLOW	Universal Port Slow Mode Register	0x004	r/w S7 S6 S5 S4 S3 S2 S1 S0 0 0 0 0 0 0 0 0 Res	
U1SLOW		0x014		
U2SLOW		0x024		
U3SLOW		0x034		
U4SLOW		0x044		
U5SLOW		0x054		
U6SLOW		0x064		
U7SLOW		0x074		
U8SLOW		0x084		
U0LVL	Universal Port Level Register	0x005	r/w A7 A6 A5 A4 A3 A2 A1 A0 0 0 0 0 0 0 0 0 Res	
U1LVL		0x015		
U2LVL		0x025		
U3LVL		0x035		
U4LVL		0x045		
U5LVL		0x055		
U6LVL		0x065		
U7LVL		0x075		
U8LVL		0x085		

Table 31–28: Universal Ports (Base addr. 0xF90400)

Mnemonic	Register Name	Offs.	Register Configuration 7 6 5 4 3 2 1 0	Section
U0PIN	Universal Port Pin Register	0x006		12.3.
U1PIN		0x016		
U2PIN		0x026		
U3PIN		0x036		
U4PIN		0x046		
U5PIN		0x056		
U6PIN		0x066		
U7PIN		0x076		
U8PIN		0x086		
U0MODE	Universal Port Mode Register	0x007		
U1MODE		0x017		
U2MODE		0x027		
U3MODE		0x037		
U4MODE		0x047		
U5MODE		0x057		
U6MODE		0x067		
U7MODE		0x077		
U8MODE		0x087		

32. Control Register and Memory Interface

32.1. Control Register CR

When exiting Reset, the device will start up in a configuration defined by the CR setting. For details on how to set the CR see chapter “Core Logic”.

A full description of the functionality of all CR bits is given below. Among others, the CR allows to configure the memory interface for connection to a variety of external memories.

CR Control Register

	7	6	5	4	3	2	1	0	Offs
r/w	x	x	x	x	x	x	x	x	3
r/w	STPCLK	RESLNG	x	x	x	TSTTOG	x	PSA	2
r/w	EB2	TFT	TETM	EB1	EBW	EASY	MFM		1
r/w	JTAG	ENDIAN	MAP		IBOOT	IROM	IRAM	ICPU	0
	Value of memory location 0x20 to 0x23								Res

The upper half word of register CR is loaded from location 0x22/0x23 only if flag EBW is at zero. If EBW is at one, the upper half word is initialized to 0xFFFB.

STPCLK **Stop Clock** (Emu parts only)
r/w1: Timers are stopped in debug mode.
r/w0: Timers are working during debug mode.
Timers are stopped with a resolution of $1/f_0$.

RESLNG **Reset Pulse Length**
r/w1: Pulse length is $8/F_{XTAL}$
r/w0: Pulse length is $2048/F_{XTAL}$
This bit specifies the length of the reset pulse which is output at pin RESETQ following an internal reset. If pin TEST is 1 the first reset after power on is short. The following resets are as programmed by RESLNG. If pin TEST is 0 all resets are long.

TSTTOG **TEST2 Pin Toggle** (Table 32–8)
This bit is used for test purposes only. If TSTTOG is true in IC active mode, pin TEST2 can toggle the Multi Function pins between Bus mode and normal mode.

PSA **Program Storage Access**
r/w1: 16bit access.
r/w0: 32bit access.
This bit allows, in EMU parts, to set the data bus access width to ROM, BootROM and Flash program storage.

EB2 **External Bus Flag 2** (Table 32–1)
r/w1: CE0Q and CE1Q select two external chips.
r/w0: OEQ and WEQ select one external chip connected to CE0Q (don’t use CE1Q).

TFT **Trace Bus Full Trace** (Emu parts only, Table 32–2)

TETM **Trace Bus ETM** (Emu parts only, Table 32–2)

EB1 **External Bus Flag 1** (Emu/MCM parts only, Table 32–1)
r/w1: Power saving mode of memory interface. Emu Bus configured for external Flash memory. Pin signals FBUSQ, BWQ0 to 3 and CE1Q are disabled and pulled low weakly. In CPU SLOW mode pin signal CE0Q activates flash memory only for 1/128th of access cycle.
r/w0: Emu Bus configured for standard external Memory. CE0Q always enables memory for full access cycle.

EBW **Emu Bus Width** (Emu/MCM parts only, Table 32–1)
r/w1: Emu Bus configured for 16bit wide external memory. Bits CR.PSA, CR.STPCLK and CR.RESLNG are forced to one and bit CR.TSTTOG is forced to zero.
r/w0: Emu Bus configured for 32bit wide external memory.

EASY **Emu Bus in Asynchronous Mode** (Table 32–1) (Emu/MCM parts only)
r/w1: Emu Bus configured for asynchronous external memory.
r/w0: Emu Bus configured for synchronous external memory.
In synchronous mode the address bus (A) and chip enable (CExQ) latches are transparent.

Table 32–1: Emu bus configuration for some commonly used external memories

EB2	EB1	EBW	EASY	External Memory Type	
				Program Memory (CE0Q)	Data or BOOT Memory (CE1Q)
1	0	0	0	32-Bit sync SRAM (e.g. MT55L256L32F)	
0	1	0	1	32-Bit async Flash (e.g. 2 x Am29F400BT)	
0	1	1	1	16-Bit async. Flash (e.g. Am29F400BT)	don’t use
0	0	0	1	32-Bit async Flash (e.g. 2 x Am29LV400BT)	
0	1	1	1	16-Bit async. Flash (e.g. Am29LV400BT)	don’t use

MFM **Multi Function pin Mode** (Tables 32–8)

JTAG **Application JTAG Interface**
r/w1: Enabled if TEST2 pin is high (Fig. 32–2)
r/w0 Disabled

ENDIAN **Endian setting ARM Core**
r/w1: Little endian.
r/w0: Big endian.
Don't change this flag dynamically

MAP **Mapping** (Table 32–3)

IBOOT **Internal Boot ROM** (Tables 32–4, 32–7)

IROM **Internal ROM** (Table 32–5)

IRAM **Internal RAM** (Tables 32–6, 32–7)

ICPU **Internal CPU**
r/w1: Enable internal CPU.
r/w0: Disable internal CPU

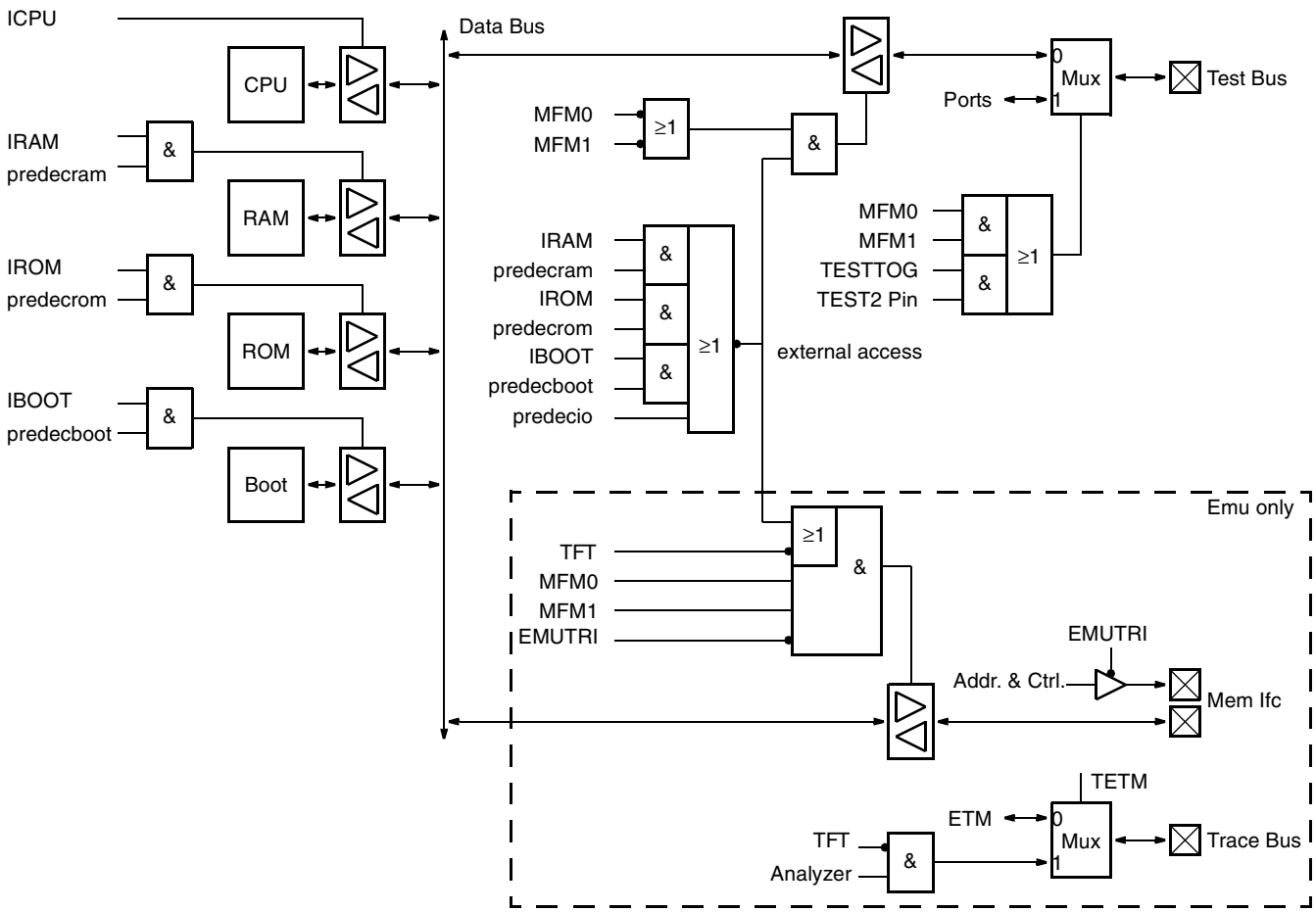


Fig. 32–1: Bus Interfaces

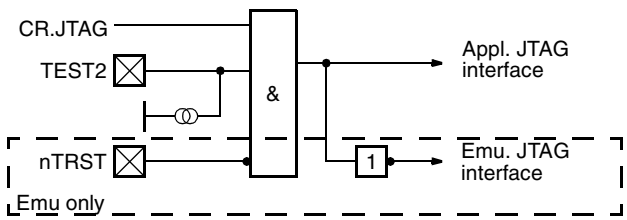


Fig. 32–2: Enabling JTAG Interfaces

Table 32–2: TETM and TFT Usage

TFT	TETM	Trace Bus Mode	D0 to D31 active	ETM
1	1	Disabled (Gnd) (Except for DBGACK, nRESET, FSYS)	for external memory access only	Off
0	1	Analyzer	always	Off
1	0	ETM	for external memory access only	On
0	0	ETM	always	On

Table 32–3: MAP usage

MAP		Mapping Effect
1	0	
0	0	mirrors RAM base offset 0xC0.0000 to 0
0	1	maps ROM/Flash base offset 0x20.0000 to 0
1	x	mirrors Boot ROM base offset 0xF0.0000 to 0

Table 32–4: IBOOT usage

IBOOT	MFM		selected Boot ROM source	
	1	0	QFP128	Emu
0	0	x	external via Multi Function pins in Bus mode	
	x	0		
	1	1	disable Boot ROM	ext. via Emu bus
1	x	x	internal Boot ROM	

Table 32–5: IROM usage

IROM	selected ROM/Flash source	
	QFP128	Emu
0	external via Multi Function pins in Bus mode	
1	internal ROM/Flash	external via Emu bus

Table 32–6: IRAM usage

IRAM	MFM		selected RAM source	
	1	0	QFP128	Emu
0	0	x	external via Multi Function pins in Bus mode	
	x	0		
	1	1	disable RAM	ext. via Emu bus
1	x	x	internal RAM	

Table 32–7: CE1Q Selections

IRAM	IBOOT	CE1Q selects	
		RAM	Boot ROM
0	x	external	internal
1	0	internal	external
1	1	No external access	

Table 32–8: TSTTOG and MFM usage in ROM/Flash parts

MFM		TSTTOG	TEST2 Pin	Multi Function Pins
1	0			
0	0	0	x	Bus mode 0
		1	0	Bus mode 0
			1	Port mode
0	1	0	x	Bus mode 1
		1	0	Bus mode 1
			1	Port mode
1	0	0	x	Bus mode 2
		1	0	Bus mode 2
			1	Port mode
1	1	x	x	Port mode

32.2. External Memory Interface

32.2.1. Interfacing examples

EVDD = 5V is required for the following interfacing examples.

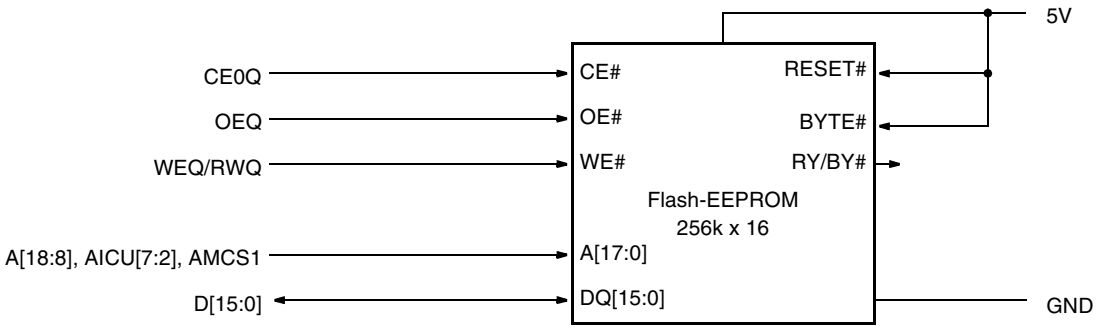


Fig. 32–3: Asynchronous Flash EEPROM (e.g. Am29F400B) as program memory

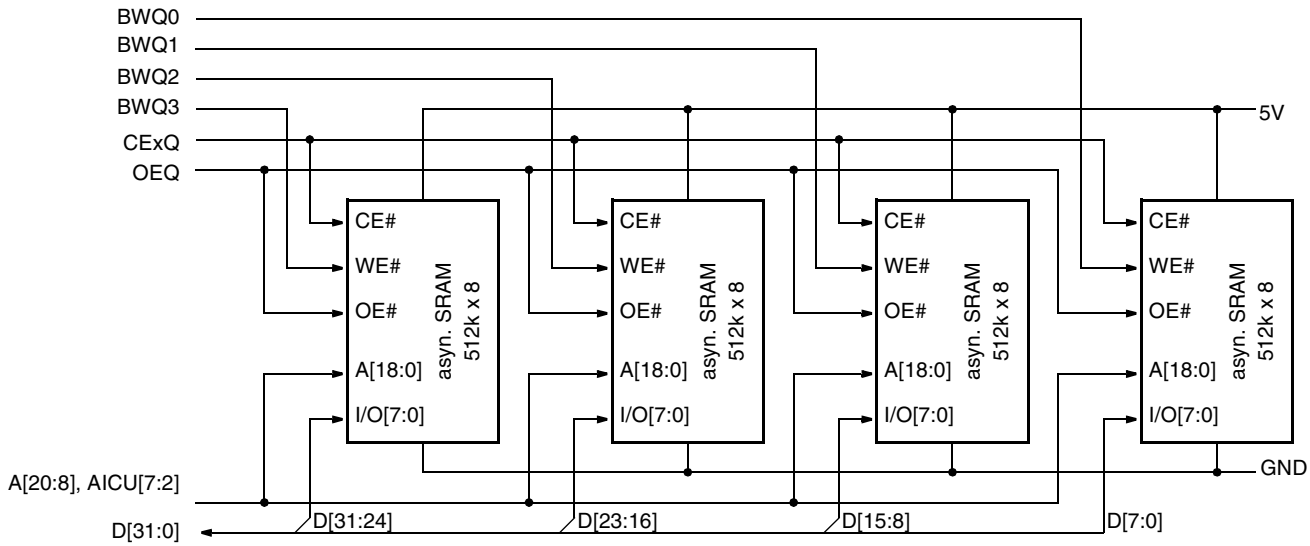


Fig. 32–4: Asynchronous SRAM (e.g. KM684002B) as emulation program memory

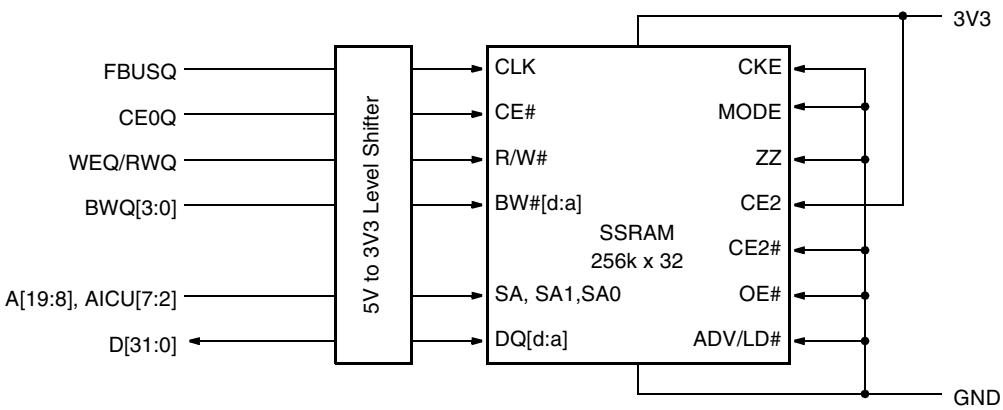


Fig. 32–5: Synchronous SRAM (e.g. MT55L256L32F) as emulation program memory

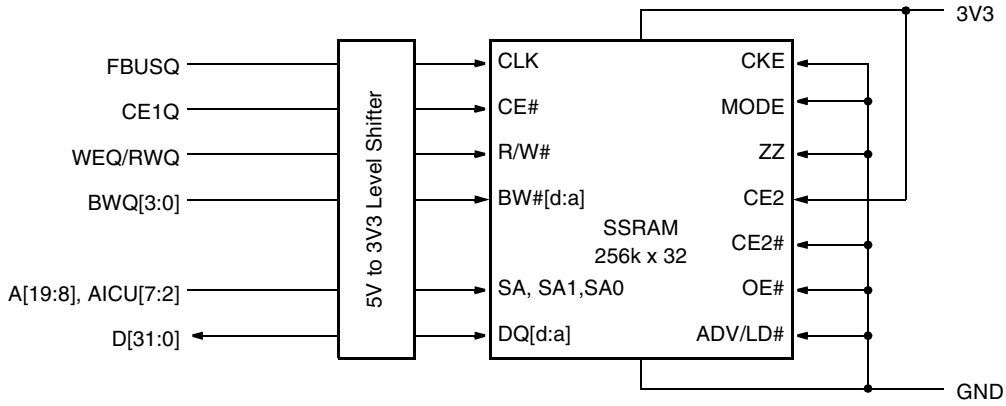


Fig. 32–6: Synchronous SRAM (e.g. MT55L256L32F) as emulation RAM or boot memory

32.2.2. External Trace Interfacing

For a mapping of the IC pins to external trace tools see the Specification of the Evaluation Board Kit (EVB).

32.2.3. Memory Interface Characteristics

Table 32–9: UVSS=UVSS1=FVSS=HVSSn=EVSSn=AVSS=0V, 3.5V<AVDD=UVDD=UVDD1<5.5V, 4.5V<EVDDn<5.5V, TCASE= 0 to 35°C, C_L = 70pF

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
DFBUSQ	FBUSQ High to Low Ratio	47.5		52.5	%	PLL mode
Synchronous SRAM						
t_{sAS}	sync Address Setup Time	0			ns	13ns ADB to Pad, 4ns Pad to DB
t_{sAH}	sync Address Hold Time		0		ns	
t_{sCES}	sync Chip Enable Setup	0		20	ns	
t_{sDSR}	sync Data Setup Read Time	25			ns	
t_{sDHR}	sync Data Hold Read Time		0		ns	
t_{sDSW}	sync Data Setup Write Time	0		15	ns	
t_{sDDT}	sync Data drive Tristate		0		ns	
Asynchronous SRAM						
t_{aAS}	async Address Setup Time	0		10	ns	
t_{aAH}	async Address Hold Time		0		ns	
t_{aCES}	async Chip Enable Setup	0		10	ns	
t_{aOES}	async Output Enable Setup		0		ns	
t_{aBWS}	async Byte Write Setup		0		ns	
t_{aDSR}	async Data Setup Read	25			ns	
t_{aDHR}	async Data Hold Read Time		0		ns	

Table 32–9: UVSS=UVSS1=FVSS=HVSSn=EVSSn=AVSS=0V, 3.5V<AVDD=UVDD=UVDD1<5.5V, 4.5V<EVDDn<5.5V, TCASE= 0 to 35°C, C_L = 70pF

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{aDSW}	async Data Setup Write	0		15	ns	
t_{aDDT}	async Data drive Tristate		0		ns	

Table 32–10: UVSS=UVSS1=FVSS=HVSSn=EVSSn=AVSS=0V, 3.5V<AVDD=UVDD=UVDD1<5.5V, 3V<EVDDn=FVDD<3.6V, TCASE= -40 to 85°C, C_L = 10pF

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Asynchronous Flash						
t_{aAS}	async Address Setup Time	0			ns	12ns ADB to Pad, 5ns Pad to DB

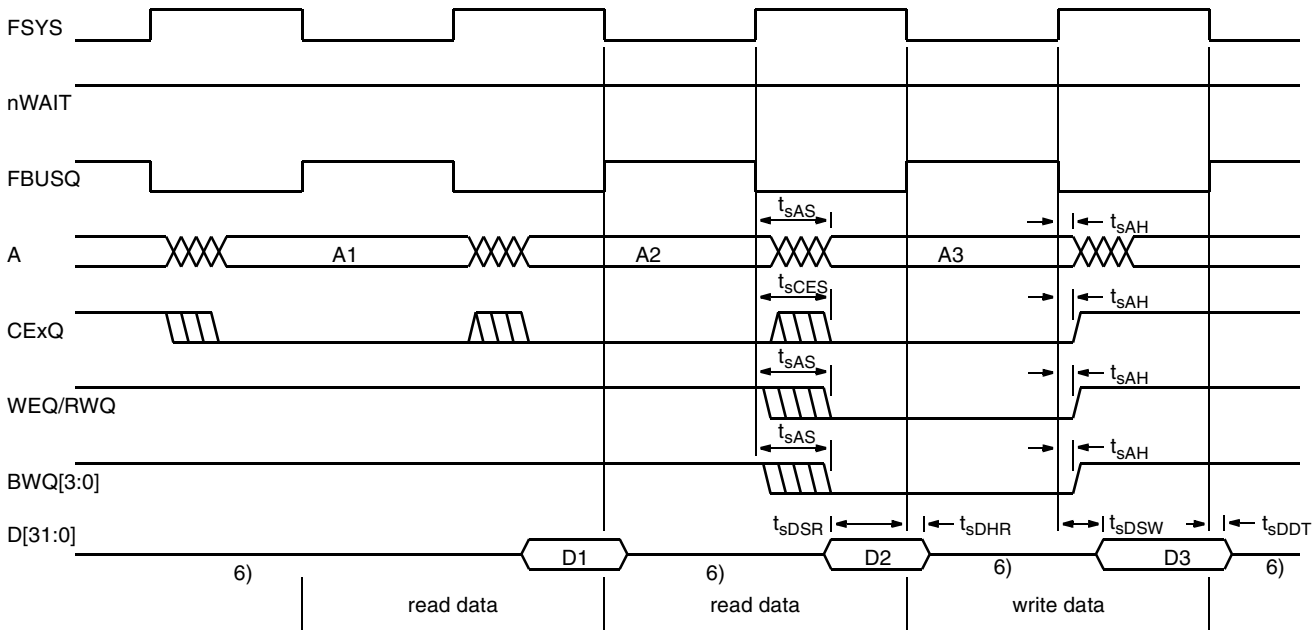


Fig. 32–7: Sync SRAM Timing, 0 Wait States

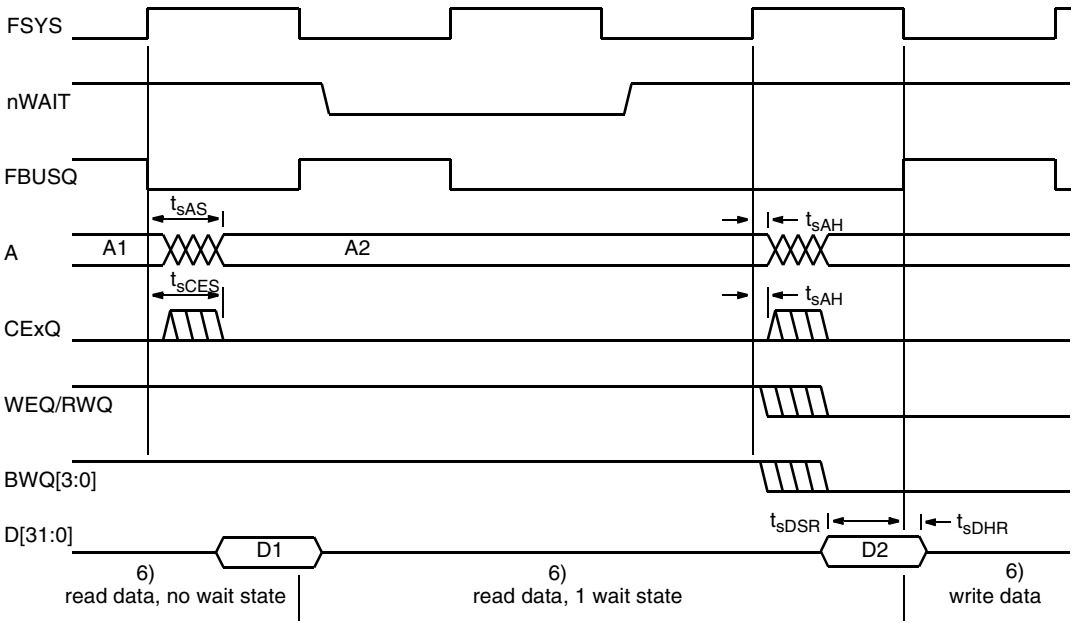


Fig. 32–8: Sync SRAM Timing, Read with Wait State, followed by a Write Cycle

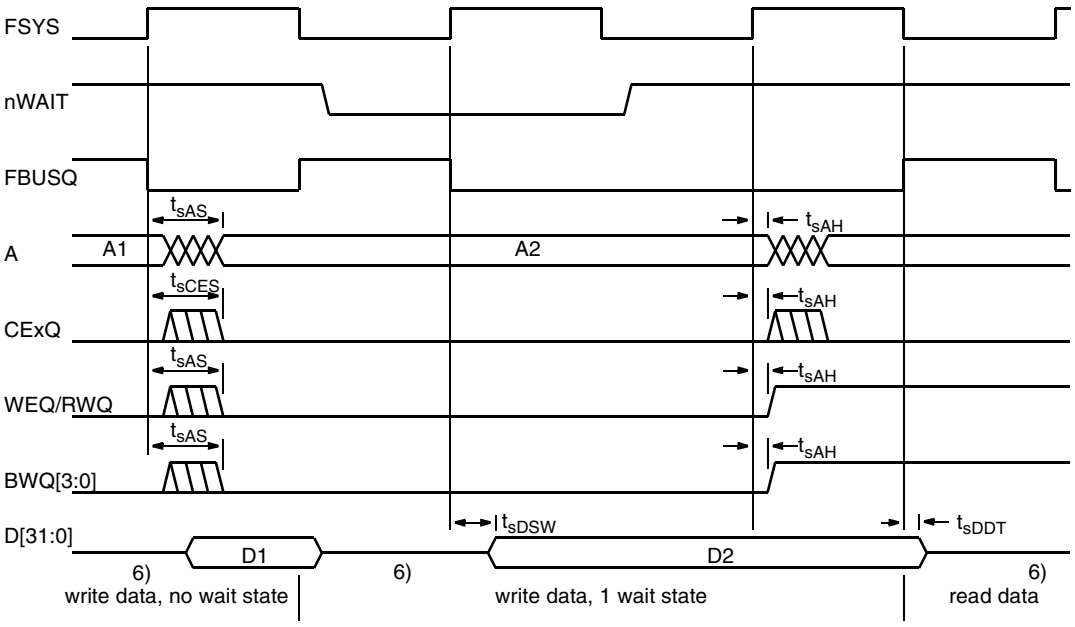


Fig. 32–9: Sync SRAM Timing, Write with Wait State, followed by a Read Cycle

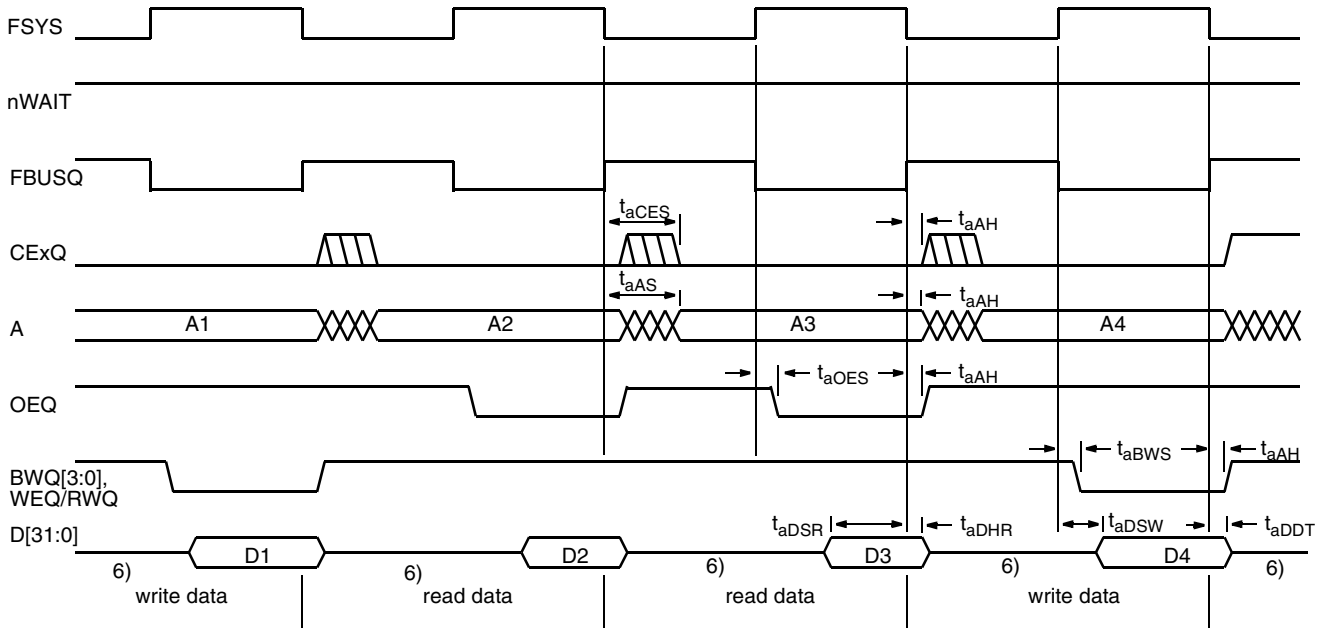


Fig. 32–10: Async SRAM/Flash Timing, 0 Wait States

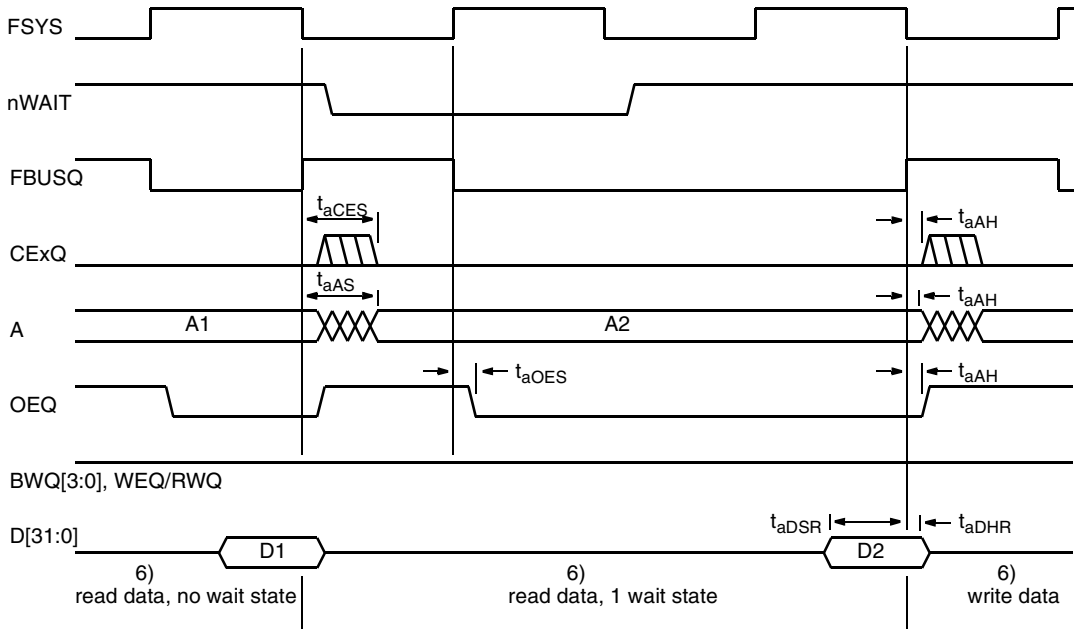


Fig. 32–11: Async SRAM/Flash Timing, Read with Wait State, followed by a Write Cycle

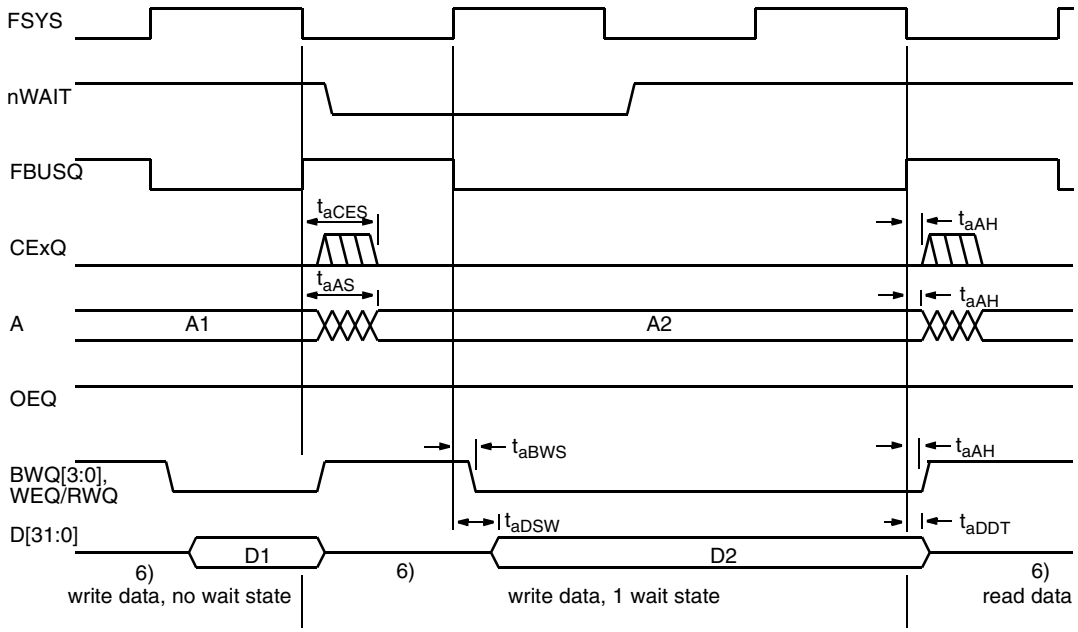


Fig. 32–12: Async SRAM/Flash Timing, Write with Wait State, followed by a Read Cycle

6) During the high level of FBUSQ the previous data bus levels are weakly held. Thus the data bus is defined when the bus drivers are tristate and FBUSQ is high. See section 'Electrical Characteristics' for the weak hold currents for pull-down (Ipd) and for pull-up (Ipu).

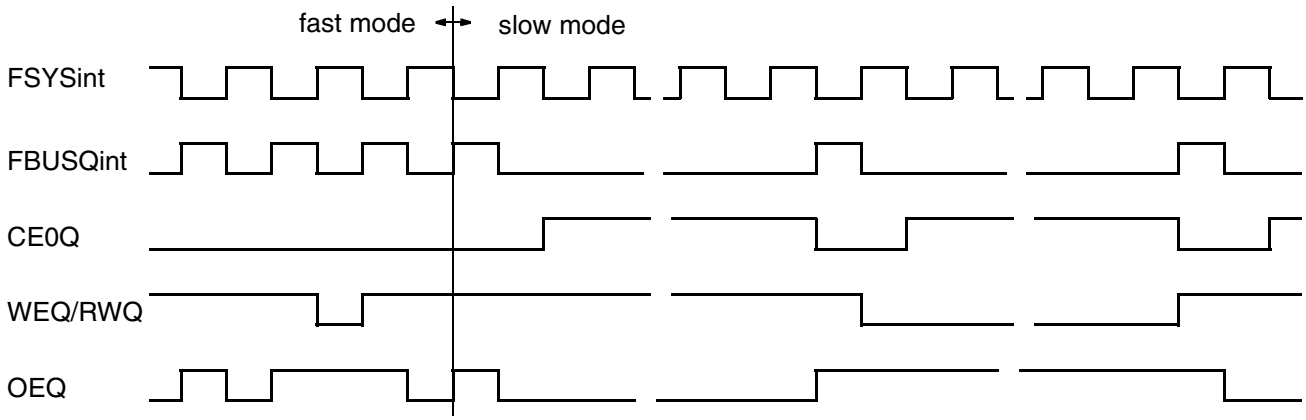


Fig. 32–13: CE0Q Timing in PLL/FAST and SLOW/DEEP SLOW modes (CR.EB2 set to 0, CR.EB1 and CR.EASY set to 1)

CE0Q is used for low power mode. Input data are latched with the rising edge of CE0Q and are weakly held as long as CE0Q stays high.

33. Differences

This chapter describes differences of this document to predecessor document “CDC32xxG-B V3.0 Automotive Controller Family Hardware Manual, CDC3205G-B Automotive Controller Specification“ (6251-546-4AI)

#	Section	Description
1	Introduction	Example Mask ROM Part replaced by CDC3272G-B, T_{CASE} extended.
2	Electrical Characteristics	Absolute Maximum Ratings: editorial corrections.
		Recommended Operating Conditions: editorial corrections.
		Characteristics: various editorial changes, changed definition: UI_{DDs}, UI_{DDd}, BV_{DD_ro}, BI_{DD_rlim}, t_{BVDD_su}, most ADC parameters, R_1 of quartz changed value: T_{CASE} range, UI_{DDs}, UI_{DDd}, HI_{DDq}, V_{ilhc}-V_{ihlc}, I_{pd}, I_{pu}, V_{ol} (H-Ports), V_{oh} (H-Ports), I_{shf}, I_{shs}, I_{shsd}, V_{REFINT}, t_{ACDEL}, AV_{lh}-AV_{hl}, t_{UCDEL}, C_i, dt_{PLL} added parameters: I_{DD_rlimr}
3	CPU and Clock System	CPU mode switching changed.
		PWM, PFM and CAPCOM: operability during CPU-Active modes corrected.
		ERM table replaced by version from Errata V3.6, F_{SYS} max. reduced. ERM deactivation procedure corrected.
4	Core Logic	Description of the Watchdog module clarified.
		Reset Logic Block Diagram clarified.
5	I2C	Block diagram corrected.
		Initialization corrected.
		Description of Write-FIFO half full interrupt corrected.
		Read-FIFO behavior clarified.
		Description of DACK flag clarified.
6	Control Register and Memory Interface	Table 32-1 corrected.
7	Differences	Chapter added.

34. Data Sheet History

1. Preliminary Data Sheet: “CDC 32xxG-B Automotive Controller Family User Manual, CDC 3205G-B Automotive Controller”, Nov. 28, 2002, 6251-546-1PD. First release of the preliminary data sheet.

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