



CD4089BM/CD4089BC Binary Rate Multiplier CD4527BM/CD4527BC BCD Rate Multiplier

General Description

The CD4089B is a 4-bit binary rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by $\frac{1}{16}$ times the binary input number. For example, if 5 is the binary input number, there will be 5 output pulses for every 16 clock pulses.

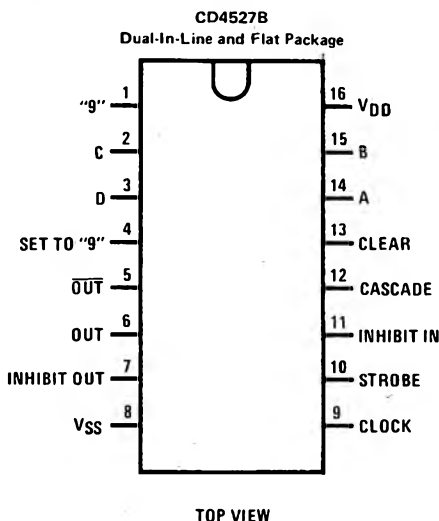
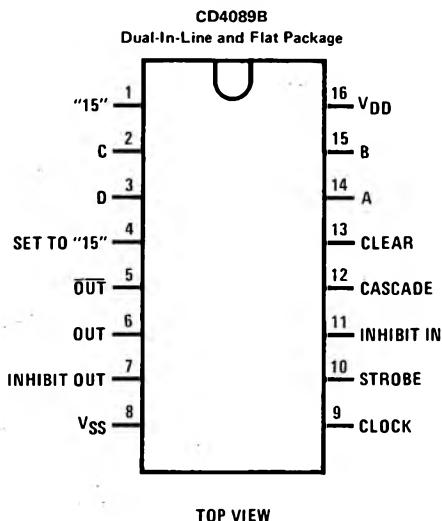
The CD4527B is a 4-bit BCD rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by $\frac{1}{10}$ times the BCD input number. For example, if 5 is the BCD input number, there will be 5 output pulses for every 10 clock pulses.

These devices may be used to perform arithmetic operations including multiplication and division, A/D and D/A conversion and frequency division.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45V_{DD} typ.
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Internally synchronous 4-bit counter
- Output clocked on the negative-going edge of clock
- STROBE for inhibiting and enabling outputs
- INHIBIT IN and CASCADE inputs for cascade operation
- Complementary output
- CLEAR and SET inputs
- "9" or "15" output and INHIBIT OUT output

Connection Diagrams



Absolute Maximum Ratings

(Notes 1 and 2)

V _{DD} Supply Voltage	−0.5 to +18V
V _{IN} Input Voltage	−0.5 to V _{DD} + 0.5V
T _S Storage Temperature Range	−65°C to +150°C
P _D Package Dissipation	500 mW
T _L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V _{DD} Supply Voltage	3 to 15 V
V _{IN} Input Voltage	0 to V _{DD} V
T _A Operating Temperature Range	−55°C to +125°C
CD4089BM, CD4527BM	−55°C to +125°C
CD4089BC, CD4527BC	−40°C to +85°C

DC Electrical Characteristics CD4089BM/CD4527BM (note 2)

PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I _{DD} Quiescent Device Current	V _{DD} = 5V		5			5		150	μA
	V _{DD} = 10V		10			10		300	μA
	V _{DD} = 15V		20			20		600	μA
V _{OL} Low Level Output Voltage	I _O ≤ 1 μA								
	V _{DD} = 5V		0.05		0	0.05		0.05	V
	V _{DD} = 10V		0.05		0	0.05		0.05	V
V _{OH} High Level Output Voltage	I _O ≤ 1 μA								
	V _{DD} = 5V	4.95		4.95	5		4.95		V
	V _{DD} = 10V	9.95		9.95	10		9.95		V
V _{IL} Low Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V		1.5			1.5		1.5	V
	V _{DD} = 10V, V _O = 1V or 9V		3.0			3.0		3.0	V
	V _{DD} = 15V, V _O = 1.5V or 13.5V		4.0			4.0		4.0	V
V _{IH} High Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5		3.5			3.5		V
	V _{DD} = 10V, V _O = 1V or 9V	7.0		7.0			7.0		V
	V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0		11.0			11.0		V
I _{OL} Low Level Output Current	V _{DD} = 5V, V _O = 0.4V	0.64		0.51	0.88		0.36		mA
	V _{DD} = 10V, V _O = 0.5V	1.6		1.3	2.25		0.9		mA
	V _{DD} = 15V, V _O = 1.5V	4.2		3.4	8.8		2.4		mA
I _{OH} High Level Output Current	V _{DD} = 5V, V _O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	V _{DD} = 10V, V _O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
	V _{DD} = 15V, V _O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I _{IN} Input Current	V _{DD} = 15V, V _{IN} = 0V		−0.1		−10 ^{−5}	−0.1		−1.0	μA
	V _{DD} = 15V, V _{IN} = 15V		0.1		10 ^{−5}	0.1		1.0	μA

DC Electrical Characteristics CD4089BC/CD4527BC (Note 2)

PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I _{DD} Quiescent Device Current	V _{DD} = 5V		20			20		150	μA
	V _{DD} = 10V		40			40		300	μA
	V _{DD} = 15V		80			80		600	μA
V _{OL} Low Level Output Voltage	I _O ≤ 1 μA								
	V _{DD} = 5V		0.05		0	0.05		0.05	V
	V _{DD} = 10V		0.05		0	0.05		0.05	V
V _{OH} High Level Output Voltage	I _O ≤ 1 μA								
	V _{DD} = 5V	4.95		4.95	5		4.95		V
	V _{DD} = 10V	9.95		9.95	10		9.95		V
V _{IL} Low Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V		1.5			1.5		1.5	V
	V _{DD} = 10V, V _O = 1V or 9V		3.0			3.0		3.0	V
	V _{DD} = 15V, V _O = 1.5V or 13.5V		4.0			4.0		4.0	V
V _{IH} High Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5		3.5			3.5		V
	V _{DD} = 10V, V _O = 1V or 9V	7.0		7.0			7.0		V
	V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0		11.0			11.0		V
I _{OL} Low Level Output Current	V _{DD} = 5V, V _O = 0.4V	0.52		0.44	0.88		0.36		mA
	V _{DD} = 10V, V _O = 0.5V	1.3		1.1	2.25		0.9		mA
	V _{DD} = 15V, V _O = 1.5V	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics (Cont'd.) CD4089BC/CD4527BC (Note 2)

PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH} High Level Output Current	$V_{DD} = 5V, V_O = 4.6V$	-0.52		-0.44	-0.88		-0.36		mA
	$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-2.25		-0.9		mA
	$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	-8.8		-2.4		mA
I_{IN} Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		-10^{-5}	-0.3		-1.0	μA
	$V_{DD} = 15V, V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL} Propagation Delay Time, Clock to Out or $\overline{Out}$	$V_{DD} = 5V$		175	350	ns
	$V_{DD} = 10V$		85	170	ns
	$V_{DD} = 15V$		60	120	ns
t_{PLH}, t_{PHL} Propagation Delay Time, Clock to E_{OUT}	$V_{DD} = 5V$		300	600	ns
	$V_{DD} = 10V$		120	240	ns
	$V_{DD} = 15V$		75	150	ns
t_{PLH}, t_{PHL} Propagation Delay Time, Clock to "9" or "15"	$V_{DD} = 5V$		280	560	ns
	$V_{DD} = 10V$		100	200	ns
	$V_{DD} = 15V$		70	140	ns
t_{PLH}, t_{PHL} Propagation Delay Time, Set or Clear to Out or $\overline{Out}$	$V_{DD} = 5V$		500	1100	ns
	$V_{DD} = 10V$		200	400	ns
	$V_{DD} = 15V$		150	300	ns
t_{PLH}, t_{PHL} Propagation Delay Time, Cascade to Out	$V_{DD} = 5V$		100	200	ns
	$V_{DD} = 10V$		50	100	ns
	$V_{DD} = 15V$		35	70	ns
t_{PLH}, t_{PHL} Propagation Delay Time, Strobe to Out	$V_{DD} = 5V$		220	440	ns
	$V_{DD} = 10V$		85	170	ns
	$V_{DD} = 15V$		65	130	ns
t_{TLH}, t_{THL} Transition Time, All Outputs	$V_{DD} = 5V$		100	200	ns
	$V_{DD} = 10V$		50	100	ns
	$V_{DD} = 15V$		40	80	ns
$t_W(CL)$ Minimum Clock Pulse Width	$V_{DD} = 5V$		250	500	ns
	$V_{DD} = 10V$		100	200	ns
	$V_{DD} = 15V$		70	140	ns
f_{CL} Maximum Clock Frequency	$V_{DD} = 5V$	1	2		MHz
	$V_{DD} = 10V$	2.5	5		MHz
	$V_{DD} = 15V$	3.5	7		MHz
t_r Maximum Clock Rise Time	$V_{DD} = 5V$			5	μs
	$V_{DD} = 10V$			1.5	μs
	$V_{DD} = 15V$			1.0	μs
t_f Maximum Clock Fall Time	$V_{DD} = 5V$			15	μs
	$V_{DD} = 10V$			15	μs
	$V_{DD} = 15V$			15	μs
$t_W(S,R)$ Minimum Set or Clear Pulse Width	$V_{DD} = 5V$		125	250	ns
	$V_{DD} = 10V$		50	100	ns
	$V_{DD} = 15V$		25	55	ns
t_{REM} Set Removal Time	$V_{DD} = 5V$		-45	0	ns
	$V_{DD} = 10V$		-20	0	ns
	$V_{DD} = 15V$		-10	0	ns
t_{SET-UP} Inhibit In Set-Up Time	$V_{DD} = 5V$		175	350	ns
	$V_{DD} = 10V$		60	120	ns
	$V_{DD} = 15V$		45	90	ns
C_i Average Input Capacitance	Any Input		5	7.5	pF
C_{PD} Power Dissipation Capacitance	Per Package, (Note 3)		80		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Truth Tables

CD4089B
Binary Rate Multiplier

INPUTS										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (H OR L)			
D	C	B	A	No. of Clock Pulses	Inh In	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 Out	Pin 7 Inh Out	Pin 1 "15"
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	16	0	1	0	0	0				
X	X	X	X	16	0	0	1	0	0				
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	0	1	L	H	L	H

*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

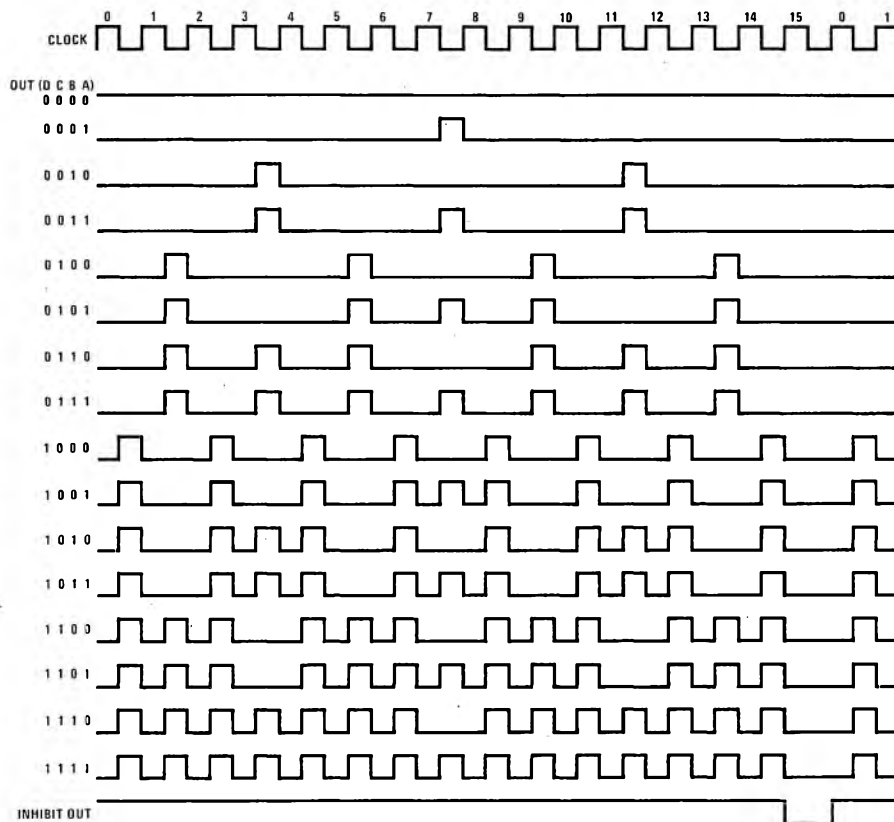
CD4527B
BCD Rate Multiplier

INPUTS										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (H OR L)			
D	C	B	A	No. of Clock Pulses	Inh In	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 Out	Pin 7 Inh Out	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
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1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0				
X	X	X	X	10	0	0	1	0	0				
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

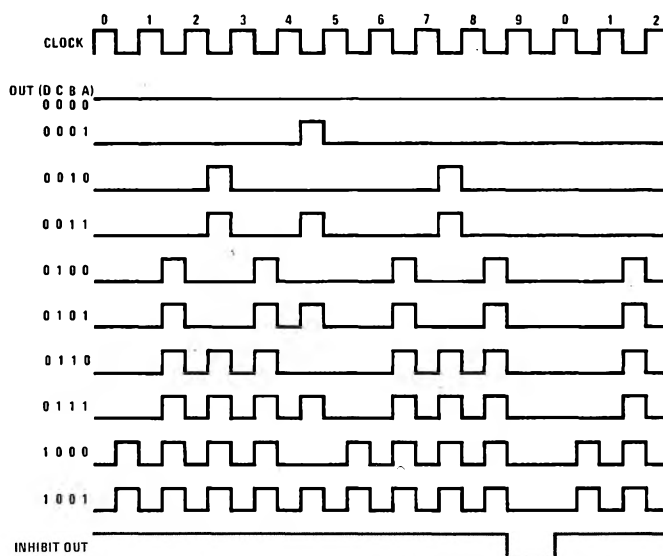
*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

Logic Waveforms

CD4089B
Binary Rate Multiplier

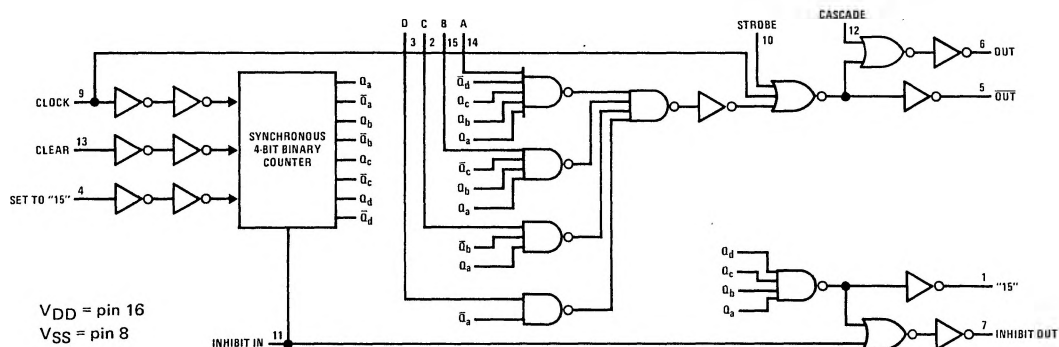


CD4527B
BCD Rate Multiplier



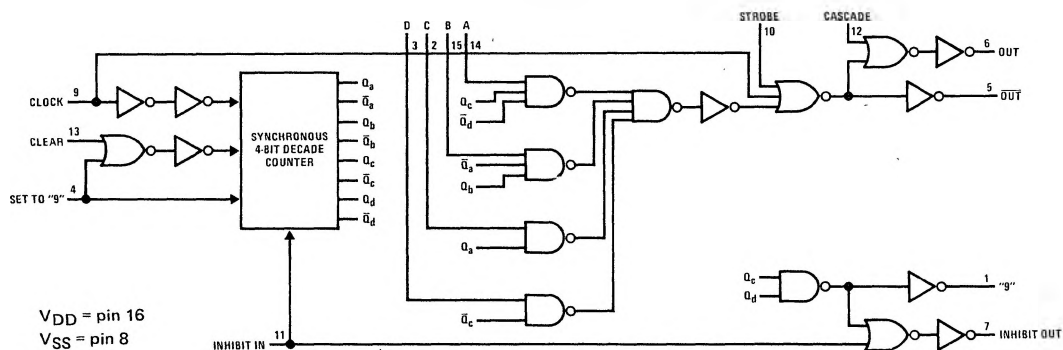
CD4089B

Binary Rate Multiplier

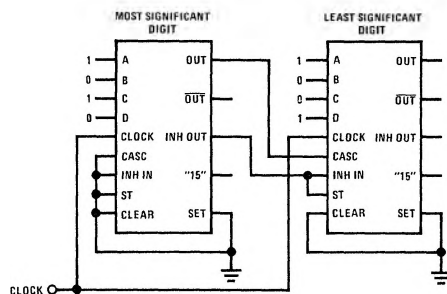


CD4527B

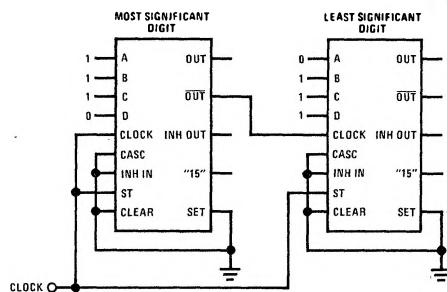
BCD Rate Multiplier



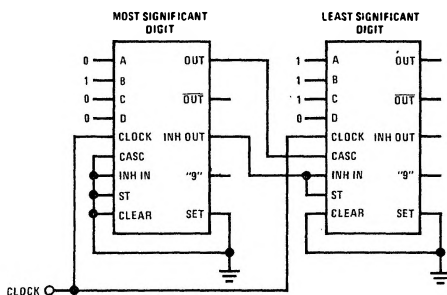
Cascading Packages



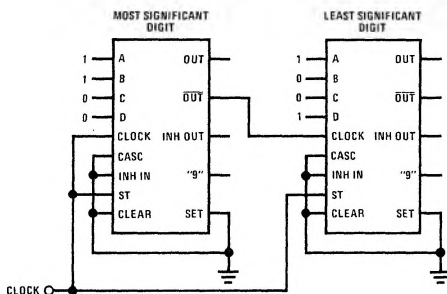
Two CD4089B's cascaded in the "add" mode with a preset number of 89 $\left(\frac{5}{16} + \frac{9}{256} = \frac{89}{256} \right)$



Two CD4089B's cascaded in the "multiply" mode with a preset number of 98 $\left(\frac{7}{16} \times \frac{14}{16} = \frac{98}{256} \right)$



Two CD4527B's cascaded in the "add" mode with a preset number of 27 $\left(\frac{2}{10} + \frac{7}{100} = \frac{27}{100} \right)$



Two CD4527B's cascaded in the "multiply" mode with a preset number of 27 $\left(\frac{3}{10} \times \frac{9}{10} = \frac{27}{100} \right)$