National Semiconductor

CD4048BM/CD4048BC TRI-STATE® Expandable 8-Function 8-Input Gate

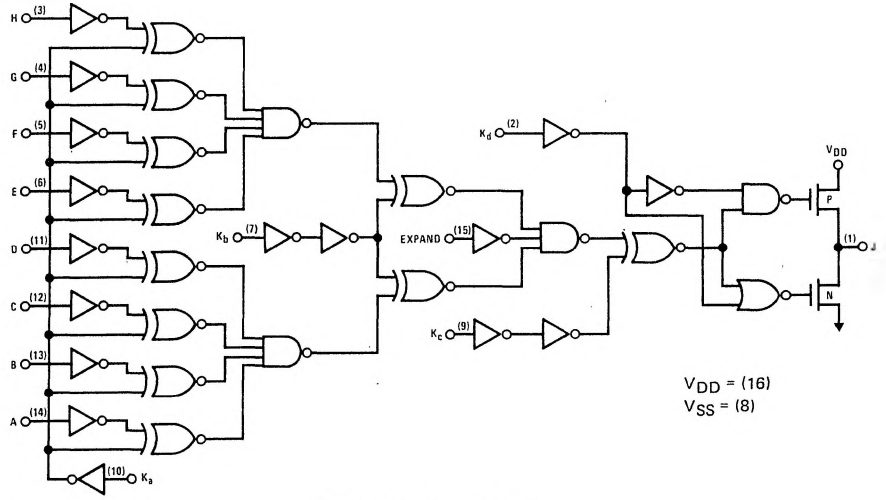
General Description

The CD4048BM/CD4048BC is a progammable 8-input gate. Three binary control lines K_a, K_b, and K_c determine the 8 different logic functions of the gate. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR. A fourth input, K_d, is a TRI-STATE control. When K_d is high, the output is enabled; when K_d is low, the output is a high impedance. This feature enables the user to connect the device to a common bus line. The Expand input permits the user to increase the number of gate inputs. For example, two 8-input CD4048's can be cascaded into a 16-input multifunction gate. When the Expand input is not used, it should be connected to V_{SS}. All inputs are buffered and protected against electrostatic effects.

Features

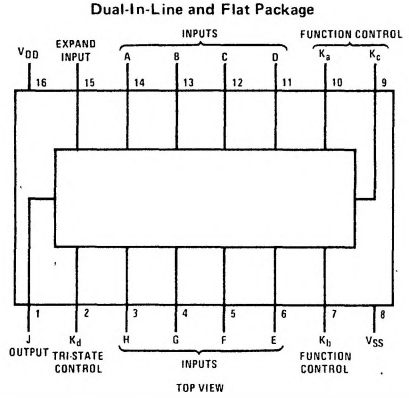
- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- High sink and source current capability
- TTL compatibility — drives 1 standard TTL load at $V_{CC} = 5$ V, over full temperature range
- Many logic functions in one package

Logic Diagram



Connection Diagram

Dual-In-Line and Flat Package



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4048BM	−55°C to +125°C
CD4048BC	−40°C to +85°C

DC Electrical Characteristics CD4048BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.01	5.0		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	2.8		2.3	4.0		1.6		mA
		V_{DD} = 10V, V_O = 0.5V	6.4		5.2	11		3.6		mA
		V_{DD} = 15V, V_O = 1.5V	14		11.5	23		8.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−2.8		−2.3	−4.0		−1.6		mA
		V_{DD} = 10V, V_O = 9.5V	−6.4		−5.2	−11		−3.6		mA
		V_{DD} = 15V, V_O = 13.5V	−14		−11.5	−23		−8.0		mA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15V, V_O = 0V		−0.2		−0.002	−0.2		−2	μA
		V_{DD} = 15V, V_O = 15V		0.2		0.002	0.2		2	μA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4048BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

DC Electrical Characteristics (Cont'd.) CD4048BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	2.3		2.0	4.0			1.6	mA
		$V_{DD} = 10V$, $V_O = 0.5V$	5.2		4.5	11			3.6	mA
		$V_{DD} = 15V$, $V_O = 1.5V$	11.5		9.8	23			8.0	mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−2.3		−2.0	−4.0			−1.6	mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−5.2		−4.5	−11			−3.6	mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−11.5		−9.8	−23			−8.0	mA
I_{TL}	TRI-STATE Leakage Current	$V_{DD} = 15V$, $V_O = 0V$		−0.6		−0.005	−0.6		−2	μA
		$V_{DD} = 15V$, $V_O = 15V$		0.6		0.005	0.6		2	μA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, and $t_r = t_f = 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		425	850	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{PLZ}, t_{PHZ}	Propagation Delay Time, K_d to	$R_L = 1.0k\Omega$				
	High Impedance (From Active	$V_{DD} = 5V$		175	350	ns
	Low or High Level)	$V_{DD} = 10V$		125	250	ns
		$V_{DD} = 15V$		100	200	ns
t_{PZL}, t_{PZH}	Propagation Delay Time, K_d to	$R_L = 1.0k\Omega$				
	Active High or Low Level	$V_{DD} = 5V$		225	450	ns
	(From High Impedance)	$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		70	140	ns
t_{THL}, t_{TLH}	Output Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{OUT}	Tristate output Capacitance				22.5	pF

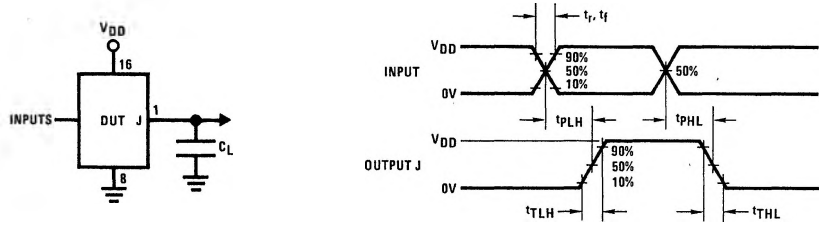
Truth Table

OUTPUT FUNCTION	BOOLEAN EXPRESSION	CONTROL INPUTS				UNUSED INPUTS
		K_a	K_b	K_c	K_d	
NOR	$J = \overline{A + B + C + D + E + F + G + H}$	0	0	0	1	V_{SS}
OR	$J = A + B + C + D + E + F + G + H$	0	0	1	1	V_{SS}
OR/AND	$J = (A + B + C + D) \cdot (E + F + G + H)$	0	1	0	1	V_{SS}
OR/NAND	$J = \overline{(A + B + C + D) \cdot (E + F + G + H)}$	0	1	1	1	V_{SS}
AND	$J = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$	1	0	0	1	V_{DD}
NAND	$J = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$	1	0	1	1	V_{DD}
AND/NOR	$J = \overline{(A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)}$	1	1	0	1	V_{DD}
AND/OR	$J = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$	1	1	1	1	V_{DD}
Hi-Z		X	X	X	0	X

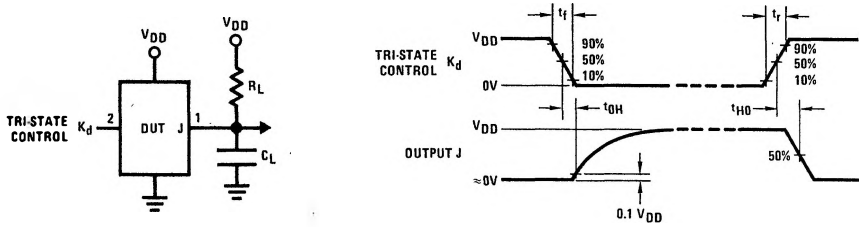
Positive logic: 0 = low level, 1 = high level, X = irrelevant, EXPAND input tied to V_{SS}.

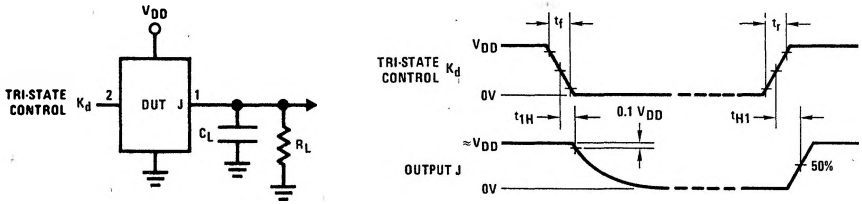
AC Test Circuits and Switching Time Waveforms

Logic Propagation Delay Time Tests



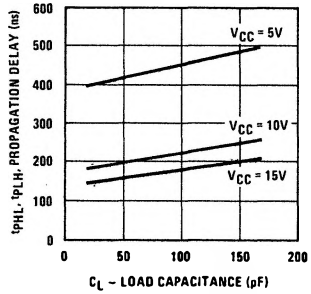
TRI-STATE Propagation Delay Time Tests



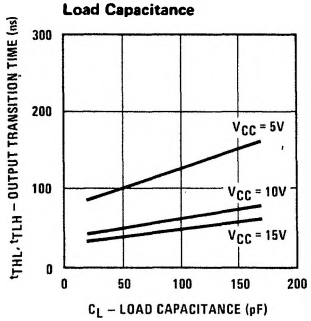


Typical Performance Characteristics

Propagation Delay vs Load Capacitance

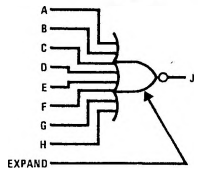


Output Transition Time vs Load Capacitance



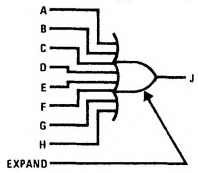
Basic Logic Configurations

NOR



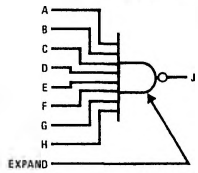
$K_aK_bK_c = 000$

OR



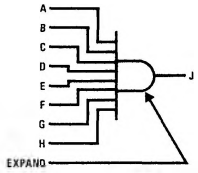
= 001

NAND



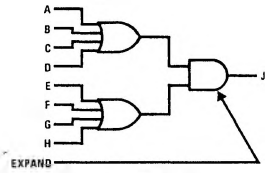
= 101

AND



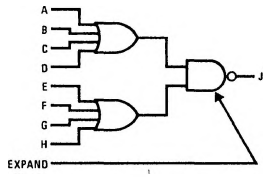
= 100

OR/AND



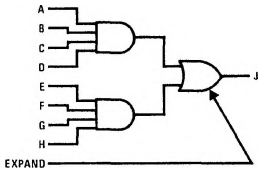
= 010

OR/NAND



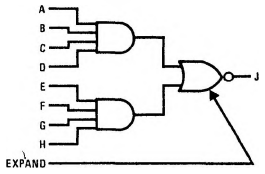
= 011

AND/OR



= 111

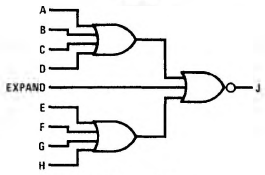
AND/NOR



= 110

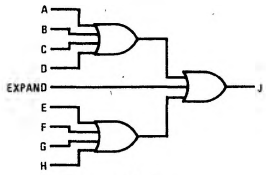
Actual Circuit Configurations

NOR



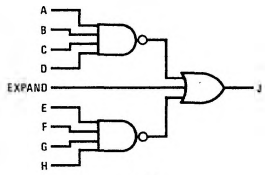
$K_aK_bK_c = 000$

OR



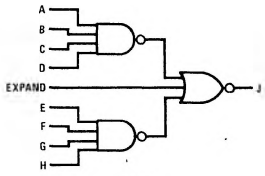
= 001

NAND



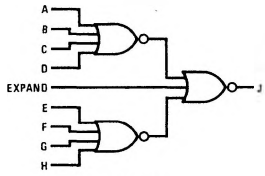
= 101

AND



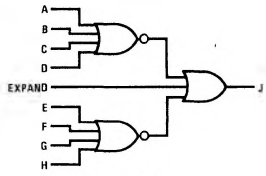
= 100

OR/AND



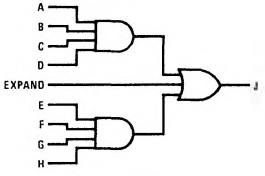
= 010

OR/NAND



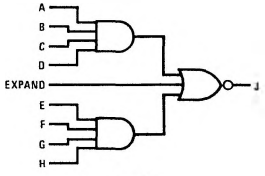
= 011

AND/OR



= 111

AND/NOR



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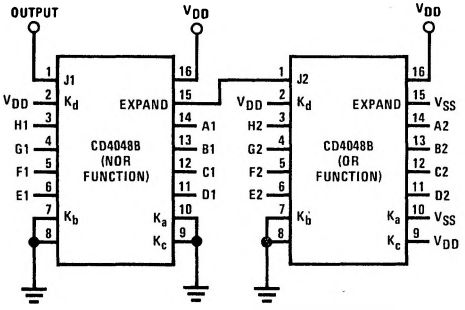
Truth Table for EXPAND Feature

COMBINED OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J = \overline{(A + B + C + D + E + F + G + H) + (EXP)}$
OR	OR	$J = (A + B + C + D + E + F + G + H) + (EXP)$
AND	NAND	$J = \overline{(ABCDEFGH) \cdot (EXP)}$
NAND	NAND	$J = \overline{(ABCDEFGH) \cdot (EXP)}$
OR/AND	NOR	$J = \overline{(A + B + C + D) \cdot (E + F + G + H) \cdot (EXP)}$
OR/NAND	NOR	$J = \overline{(A + B + C + D) \cdot (E + F + G + H) \cdot (EXP)}$
AND/NOR	AND	$J = \overline{(ABCD) + (EFGH) + (EXP)}$
AND/OR	AND	$J = (ABCD) + (EFGH) + (EXP)$

Note. Positive logic is assumed. (EXP) represents the logic level present at the EXPAND input.

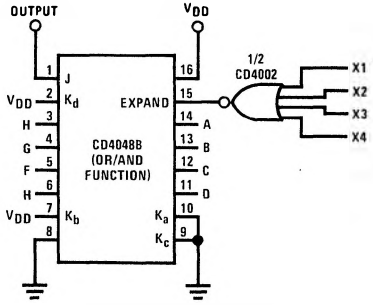
Typical Applications of EXPAND Feature

16-Input NOR Gate



$$\text{Output} = \overline{A1 + B1 + C1 + D1 + E1 + F1 + G1 + H1 + A2 + B2 + C2 + D2 + E2 + F2 + G2 + H2}$$

12-Input OR/AND Gate



Output = (A + B + C + D) • (E + G + H) • (X1 + X2 + X3 + X4) F +