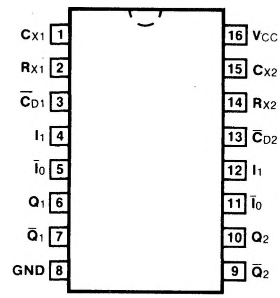
96S02
96LS02

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

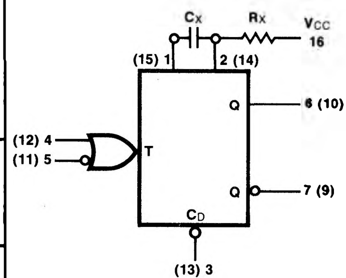
DESCRIPTION — The 96S02 and 96LS02 are dual retriggerable and resettable monostable multivibrators. These one-shots provide exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 1.0 MΩ for the 96LS02 and 2.0 MΩ for the 96S02 reduce required capacitor values. Hysteresis is provided on both trigger inputs of the 96LS02 and on the positive trigger input of the 96S02 for increased noise immunity.

- **REQUIRED TIMING CAPACITANCE REDUCED BY FACTORS OF 10 TO 100 OVER CONVENTIONAL DESIGNS**
- **BROAD TIMING RESISTOR RANGE — 1.0 kΩ to 2.0 MΩ**
- **OUTPUT PULSE WIDTH IS VARIABLE OVER A 2000:1 RANGE BY RESISTOR CONTROL**
- **PROPAGATION DELAY OF 35 ns 96LS02, 12 ns 96S02**
- **0.3 V HYSTERESIS ON TRIGGER INPUTS**
- **OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE**
- **35 ns TO ∞ OUTPUT PULSE WIDTH RANGE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

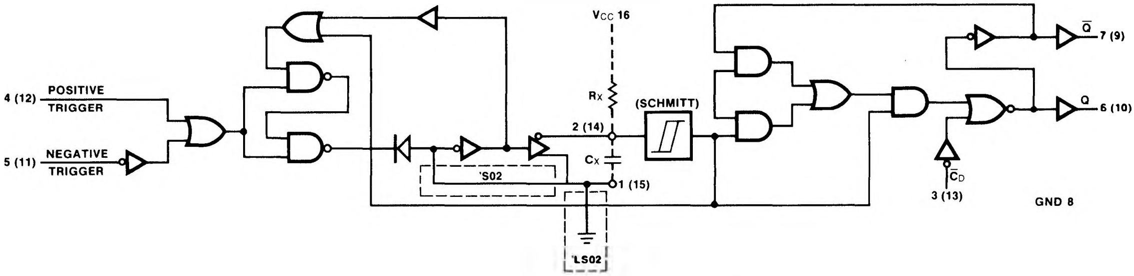
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	96S02PC, 96LS02PC		9B
Ceramic DIP (D)	A	96S02DC, 96LS02DC	96S02DM, 96LS02DM	6B
Flatpak (F)	A	96S02FC, 96LS02FC	96S02FM, 96LS02FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96S (U.L.) HIGH/LOW	96LS (U.L.) HIGH/LOW
$\overline{I}_0$	Trigger Input (Active Falling Edge)	0.5/0.625	
$\overline{I}_0$	Schmitt Trigger Input (Active Falling Edge)		0.5/0.25
I_1	Schmitt Trigger Input (Active Rising Edge)	0.5/0.625	0.5/0.25
$\overline{C}_D$	Direct Clear Input (Active LOW)	0.5/0.625	0.5/0.25
Q	True Pulse Output	25/12.5	10/5.0 (2.5)
$\overline{Q}$	Complementary Pulse Output	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM

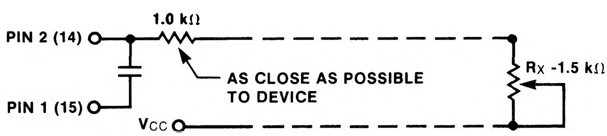


FUNCTIONAL DESCRIPTION — The 96S02 and 96LS02 dual retriggerable resettable monostable multivibrators have two dc coupled trigger inputs per function, one active LOW ($\overline{I}_0$) and one active HIGH (I_1). The I_1 input of both circuit types and the $\overline{I}_0$ input of the 96LS02 utilize an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are dc coupled making triggering independent of input transition times. When input conditions for triggering are met the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\overline{Q}$ output to $\overline{I}_0$ or the Q output to I_1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

Operation Notes

TIMING

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.0 kΩ to 1.0 MΩ (96LS02) or 2.0 MΩ (96S02).
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1 (15), the (-) terminal to pin 2 (14) and R_X. Pin 1 (15) will remain positive with respect to pin 2 (14) during the timing cycle. In the 96S02, however, during quiescent (non-triggered) conditions, pin 1 (15) may go negative with respect to pin 2 (14) depending on values of R_X and V_{CC}. For values of $R_X \geq 10$ kΩ the maximum amount of capacitor reverse polarity, pin 1 (15) negative with respect to pin 2 (14) is 500 mV. Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to 5% of their working forward voltage rating; therefore, capacitors having a rating of 10 WVdc or higher should be used with the 96S02 when $R_X \geq 10$ kΩ.
4. The output pulse width t_w for $R_X \geq 10$ kΩ and $C_X \geq 1000$ pF is determined as follows:
   (96S02) $t_w = 0.55\ R_X C_X$
   (96LS02) $t_w = 0.43\ R_X C_X$
   Where R_X is in kΩ, C_X is in pF, t is in ns *or* R_X is in kΩ, C_X is in μF, t is in ms.
5. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

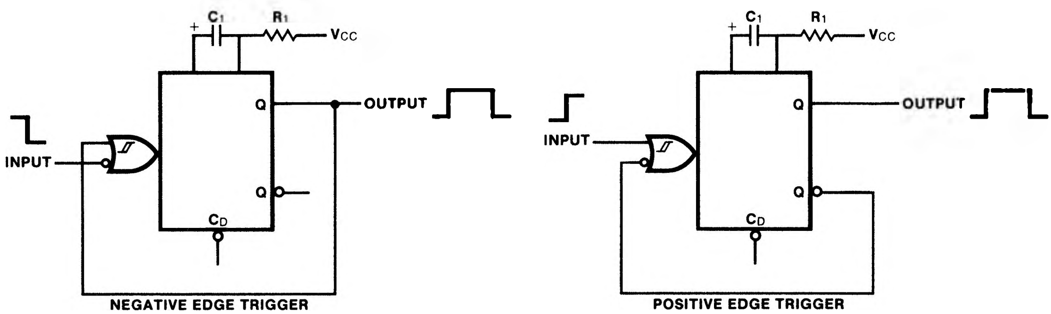


Operation Notes (Cont'd)

7. Under any operating condition, C_X and R_X (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 μF to 0.1 μF bypass capacitor between V_{CC} and ground located near the circuit is recommended.

TRIGGERING

1. The minimum negative pulse width into $\bar{I}_0$ is 8.0 ns; the minimum positive pulse width into I_1 is 12 ns.
2. Input signals to the 96S02 exhibiting slow or noisy transitions should use the positive trigger input I_1 which contains a Schmitt trigger. Input signals to the 96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.
3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.



4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on $\bar{C}_D$ will not trigger the 96S02 or 96LS02. If the $\bar{C}_D$ input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

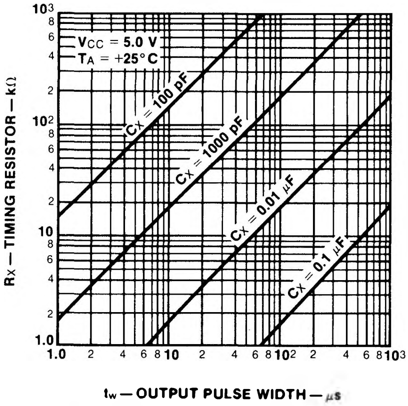
TRIGGERING TRUTH TABLE

PIN NO'S. 5 (11)	4 (12)	3 (13)	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

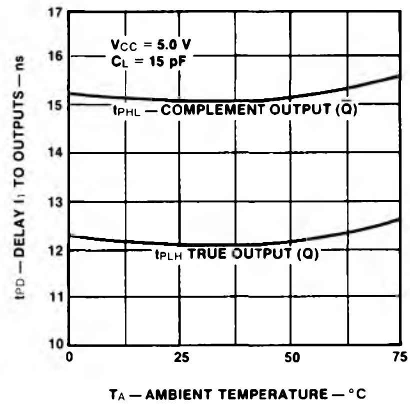
H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Immaterial (either H or L)
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

TYPICAL CHARACTERISTICS
96S02

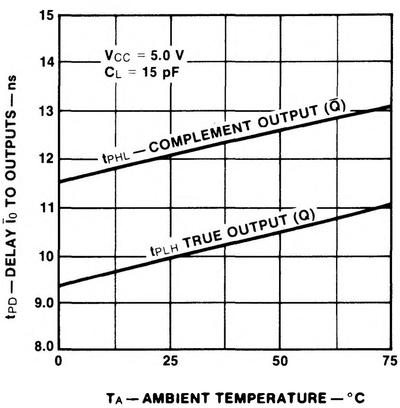
OUTPUT t_W vs R_X and C_X



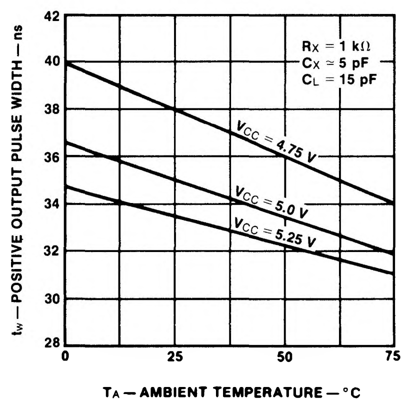
$\bar{I}_1$ DELAY TIME vs T_A



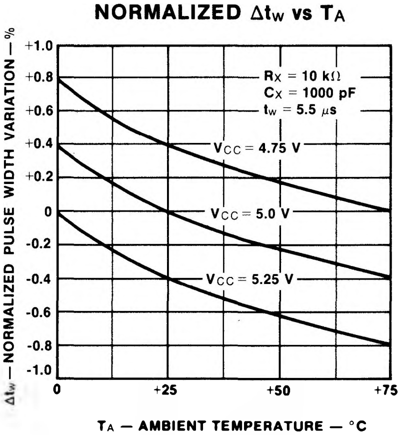
$\bar{I}_0$ DELAY TIME vs T_A



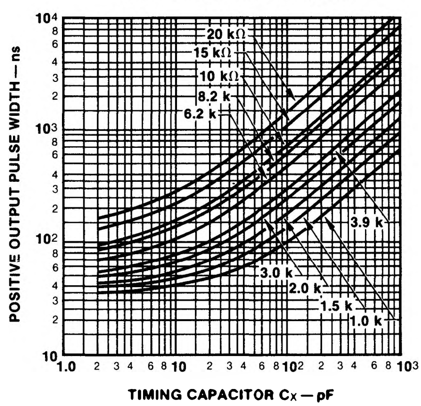
OUTPUT t_W vs T_A



NORMALIZED Δt_W vs T_A

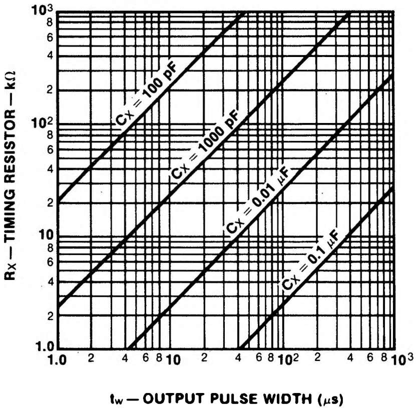


PULSE WIDTH vs $R_X C_X$

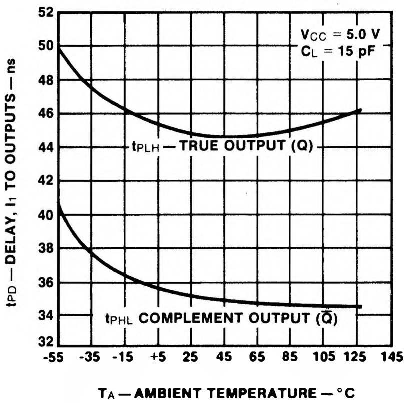


TYPICAL CHARACTERISTICS
96LS02

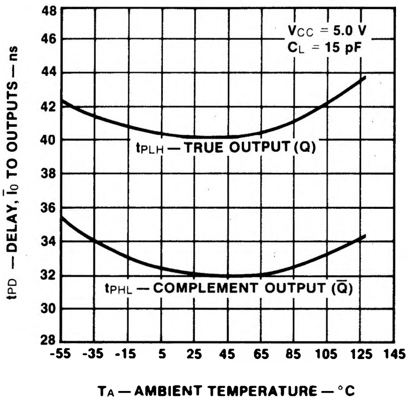
OUTPUT t_w vs R_X and C_X



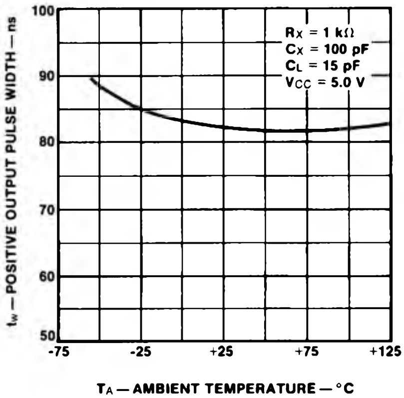
I_1 DELAY TIME vs T_A



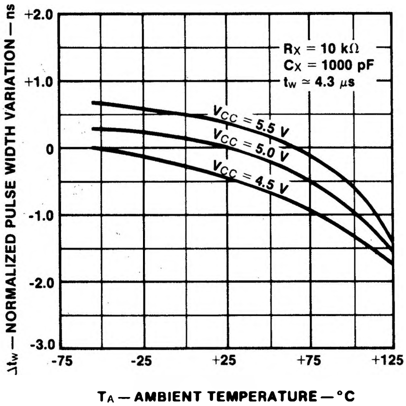
$\bar{I}_0$ DELAY TIME vs T_A



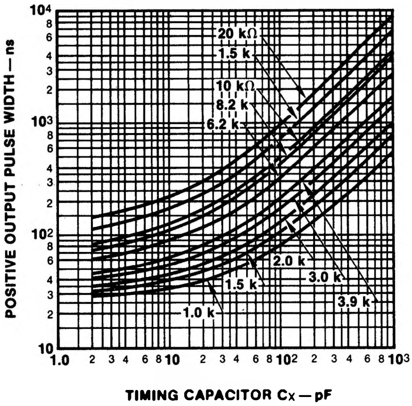
OUTPUT t_w vs T_A



NORMALIZED Δt_w vs T_A

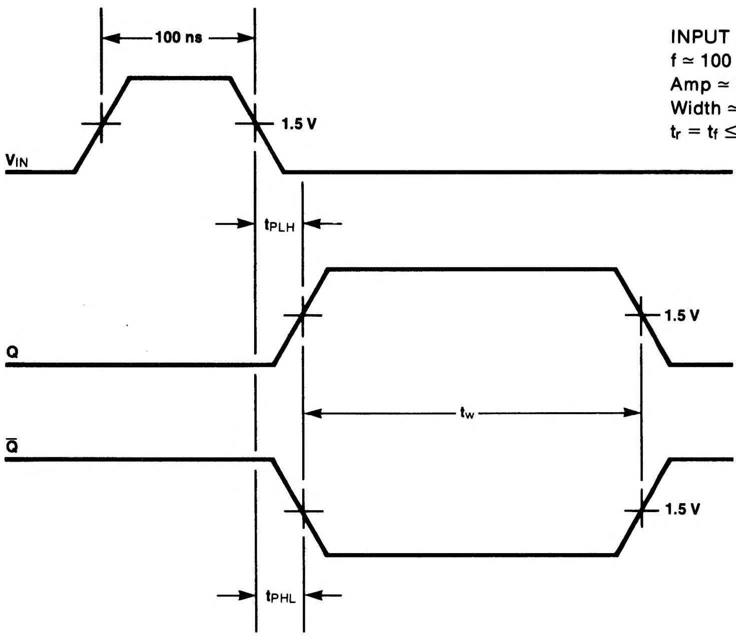


PULSE WIDTH vs R_XC_X



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		96S Min	96S Max	96LS Min	96LS Max	UNITS	CONDITIONS
V_{T+}	Positive-going Threshold Voltage, $\bar{I}_0$, I_1 (96LS02) I_1 (96S02)			2.0		2.0	V	V_{CC} = 5.0 V
V_{T-}	Negative-going Threshold Voltage $\bar{I}_0$, I_1 (96LS02) I_1 (96S02)	XM	0.8		0.7		V	V_{CC} = 5.0 V
		XC	0.8		0.8			
V_{OH}	Output HIGH Voltage	XM	2.7		2.5		V	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} I_{OH} = -400 μA ('LS02) I_{OH} = -1.0 mA ('S02)
		XC	2.7		2.7			
V_{OL}	Output LOW Voltage	XM		0.5		0.5	V	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}
		XC		0.5		0.4		
V_{CX}	Capacitor Voltage Pin 1 (15) Referenced to Pin 2 (14)		-0.85	3.0	0	3.0	V	R_X = 1.0 kΩ, V_{CC} = 4.75 V to 5.25 V
			-0.5	3.0	0	3.0		R_X = > 10 kΩ
			-0.4	3.0	0	3.0		R_X > 1.0 MΩ
I_{IH}	Input HIGH Current			20		20	μA	V_{IN} = 2.7 V, V_{CC} = Max
				0.1		0.1	mA	V_{IN} = 5.5 V ('S02) V_{IN} = 10 V ('LS02)
I_{IL}	Input LOW Current			-1.0		-0.4	mA	V_{IN} = 0.4 V, V_{CC} = Max
I_{OS}	Output Short Circuit Current		-40	-100	-20	-100	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current			75		36	mA	V_{IN} = Open, V_{CC} = Max



INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leq 5$ ns

Fig. a

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	96S C_L = 15 pF Min	96S C_L = 15 pF Max	96LS C_L = 15 pF Min	96LS C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay $\overline{I}_0$ to Q		15		55	ns	Fig. a
t_{PHL}	Propagation Delay $\overline{I}_0$ to $\overline{Q}$		19		50	ns	Fig. a
t_{PLH}	Propagation Delay I_1 to Q		19		60	ns	Fig. a
t_{PHL}	Propagation Delay I_1 to $\overline{Q}$		20		55	ns	Fig. a
t_{PHL}	Propagation Delay $\overline{C}_D$ to Q		20		30	ns	Fig. a
t_{PLH}	Propagation Delay $\overline{C}_D$ to $\overline{Q}$		14		35	ns	Fig. a
t_w (L)	$\overline{I}_0$ Pulse Width LOW	8.0		15		ns	Fig. a
t_w (H)	I_1 Pulse Width HIGH	12		30		ns	Fig. a
t_w (L)	$\overline{C}_D$ Pulse Width LOW	7.0		22		ns	Fig. a
t_w (H)	Minimum Q Pulse Width HIGH	30	45	25	55	ns	R_X = 1.0 kΩ, C_X = 10 pF including jig and stray
t_w	Q Pulse Width	5.2	5.8	4.1	4.5	µs	R_X = 10 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range*	1.0	2000	1.0	1000	kΩ	T_A = -55° C to +125° C, V_{CC} = 4.5 V to 5.5 V
t	Change in Q Pulse Width over Temperature — XM				3.0	%	R_X = 10 kΩ, C_X = 1000 pF
	Change in Q Pulse Width over Temperature — XC		1.0		1.0	%	R_X = 10 kΩ, C_X = 1000 pF
t	Change in Q Pulse Width over V_{CC} Range		1.0		0.8	%	T_A = 25° C, V_{CC} = 4.75 V to 5.25 V, R_X = 10 kΩ, C_X = 1000 pF
					1.5	%	T_A = 25° C, V_{CC} = 4.5 V to 5.5 V, R_X = 10 kΩ, C_X = 1000 pF

*Applies only over commercial V_{CC} and T_A range for 96S02.