CRC GENERATOR/CHECKER — 8X01A/9401

PRELIMINARY

DESIGN FEATURES

- **TTL inputs/outputs**
- **12MHz (Max) data rate**
- **Separate preset/reset controls**
- **SDLC specified pattern match (8X01A only)**
- **Automatic right justification**
- **Pin-for-pin compatibility and functionally identical with 8X01 (8X01A only)**
- **V_{CC} = 5V**
- **14-Pin DIP**

USE AND APPLICATION

- **Floppy and other disk systems**
- **Digital cassette and cartridge systems**
- **Data communication systems**

PRODUCT DESCRIPTION

The CRC Generator/Checker (8X01A or 9401) provides error-correction capabilities for digital systems that handle serial data. The two parts differ in that the 8X01A provides Synchronous Data Link Control (SDLC).

The serial data stream is divided by a selected polynomial; the remainder resulting from this algebraic process is transmitted at the end of the data stream as a Cyclic Redundancy Check Character (CRCC). At the receiving end, the same calculation is performed on the data. If the received message is error-free, the calculated remainder should satisfy a predetermined pattern. In most cases, the remainder is zero; however, where SDLC protocols (8X01A only) are used, the correct remainder is 1111000010111000 (X^0–X^{15}).

Eight polynomials are provided and any of these can be selected via a 3-bit control bus. Popular polynomials, such as CRC-16 and CCITT are implemented and the one selected can be programmed to start with all zeroes or all ones. Right justification for polynomials of degree less than 16 is automatic.

FUNCTIONAL OPERATION

8X01A and 9401

The CRC Generator/Checker circuit provides a means of detecting errors in a serial data communications environment. A binary message can be interpreted as a binary polynomial H(x). This polynomial can be divided by a generator polynomial P(x) such that H(x) = P(x) Q(x) + R(x) whereby Q(x) is the quotient and R(x) is the remainder. During transmission, the remainder is appended to the end of the message as check bits. For a given message, a unique remainder is generated. Hardware implementation of division is simply a feedback shift register with Exclusive-OR gating. Subtraction and addition in modulo 2 is implemented by the Exclusive-OR function. The number of shift register stages is equal to the degree of the divisor polynomial.

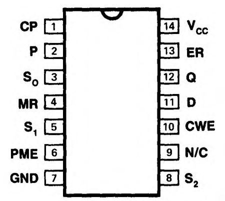
The accompanying truth table defines the polynomials implemented in the CRC circuit. Each polynomial can be selected via control inputs S_0, S_1 and S_2. To generate the check bits, the data stream is entered via the Data (D) input, using the high to low transition of the Clock ($\overline{CP}$) input. This data is gated with the most significant output (Q) of the shift register which, in turn, controls the exclusive OR gates. The Check Word Enable (CWE) must be held high while the data is being entered. After the last data bit is entered, the CWE is brought low and the check bits are shifted out of the register and appended to the data bits using external gating—see Check Word Generation diagram.

To check an incoming message for errors, both the data and check bits are entered through the "D" input with the CWE input held high. The 8X01A while not in the data path, monitors the message. After the last check bit is entered, in the 8X01A, the ERror output is made valid by a high-to-low transition of $\overline{CP}$. If no error is detected during the data transmission, all bits of the internal register are low and the ERror output is also low; if an error is detected, it is reflected by the bit pattern and the ERror output is high. The ERror output status remains valid until the next high-to-low transition of $\overline{CP}$ or until initialized by the preset ($\overline{P}$) or reset (MR) functions. The $\overline{PME}$ line must be high if the ERror output is used to indicate an all-zero result.

A high level applied to the Master Reset (MR) input asynchronously clears the shift register. A low level applied to the Preset (P) input asynchronously sets all bits to the appropriate state if the control-code inputs (S_0, S_1, and S_2) specify a 16-bit polynomial. In the

8X01A & 9401 PACKAGE/PIN DESIGNATOR

N, F PACKAGE



TOP VIEW

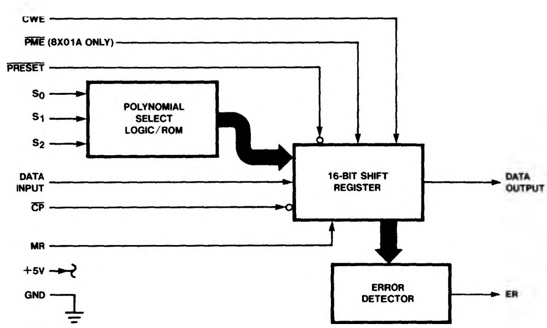
S_0, S_1, S_2	— POLYNOMIAL SELECT INPUTS
D	— DATA INPUTS
$\overline{CP}$	— CLOCK INPUT (ACTIVE ON HIGH-TO-LOW TRANSITION)
CWE	— CHECK WORD ENABLE
$\overline{P}$	— PRESET INPUT (ACTIVE LOW)
MR	— MASTER RESET INPUT (ACTIVE HIGH)
Q	— DATA OUTPUT
ER	— ERROR OUTPUT (ACTIVE HIGH)
$\overline{PME}$ (8X01A ONLY)	— PATTERN MATCH ENABLE (ACTIVE LOW)
N/C	— NO CONNECTION

ORDER NUMBERS

N8X01A, N941N, S801AF, S9041F

* 8X01A only; for 9401, pin 6 is not connected (N/C)

BLOCK DIAGRAM OF 8X01A & 9401



NOTE
Refer to Truth Table on next page for selection of polynomials.

CRC GENERATOR/CHECKER 8X01A/9401

PRELIMINARY

FUNCTIONAL OPERATION (cont'd)

case of check polynomials that are 8-or-12 bits in length, only the most significant 8-or-12 bits of the shift register are set; all remaining bits are cleared.

8X01A ONLY

For data communications using the Synchronous Data Link Control (SDLC) protocol, the 8X01A is preset to an all-ones configuration before any accumulation is done; this applies to both transmitting and receiving modes of operation. Using SDLC, the check sum shifted out of the 8X01A must be inverted.

During the receiving mode, a special pattern of 1111000010111000 (X^0-X^{15}) is used in place of all-zeroes to check for a valid message. The Pattern Match Enable pin allows the user to select this option. If $\overline{PME}$ is low during the last bit time of the message, the ERror output is low providing the result matches the special pattern; if an error occurs, ER is high.

TRUTH TABLE

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$x^{16}+x^{15}+x^2+1$	CRC-16
L	L	H	$x^{16}+x^{14}+x+1$	CRC-16 REVERSE
L	H	L	$x^{16}+x^{15}+x^{13}+x^7+x^4+x^2+x^1+1$	
L	H	H	$x^{12}+x^{11}+x^3+x^2+x+1$	CRC-12
H	L	L	$x^8+x^7+x^5+x^4+x+1$	
H	L	H	x^8+1	LRC-8
H	H	L	$x^{16}+x^{12}+x^5+1$	CRC-CCITT
H	H	H	$x^{16}+x^{11}+x^4+1$	CRC-CCITT REVERSE

RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
$\overline{CP}$	Clock input	0		12	MHz

DC ELECTRICAL CHARACTERISTICS FOR 8X01A

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input high voltage		2.0			2 0			V
V_{IL}	Input low voltage				0.8			0.7	V
V_{IC}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = −18mA		−0.9	−1.5		−0.9	−1.5	V
V_{OH}	Output high voltage	V_{CC} = Min, I_{OH} = −400μA	2.7	3 4		2.4	3.4		V
V_{OL}	Output low voltage	V_{CC} = Min, I_{OL} = 4.0mA		0.35	0.4		0.35	0.4	V
		V_{CC} = Min, I_{OL} = 8.0mA		0 45	0.5		—	—	V
I_{IL}	Input low current	V_{CC} = Max, V_{IN} = 0.4V		−0.22	−0.36		−0.22	−0.36	mA
I_{IH}	Input high current	V_{CC} = Max, V_{IN} = 2.7V			20			20	μA
I_{IH}	Max input current	V_{CC} = Max, V_{IN} = 7V			0.1			0.1	mA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V[2]	−10		−42	−10		−42	mA
I_{CC}	Supply current	V_{CC} = Max, inputs open		60	110		60	110	mA

DC ELECTRICAL CHARACTERISTICS FOR 9401

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input high voltage	Guar. input high voltage	2.0			2.0			V
V_{IL}	Input low voltage	Guar. input low voltage			0 8			0.7	V
V_{IC}	Input clamp diode voltage	V_{CC} = Min I_{IN} = −18mA		−0.9	−1.5		−0.9	−1.5	V
V_{OH}	Output high voltage	V_{CC} = Min, I_{OH} = −400μA	2.4	3.4		2.4	3.4		V
V_{OL}	Output low voltage	V_{CC} = Min, I_{OL} = 4.0mA		0.35	0.4		0.35	0.4	V
		V_{CC} = Min, I_{OL} = 8.0mA		0 45	0.5		—	—	V
I_{IL}	Input low current	V_{CC} = Max, V_{IN} = 0.4V		−0.22	−0.36		−0.22	−0 36	mA
I_{IH}	Input high current	V_{CC} = Max, V_{IN} = 2.7V		1 0	40		1 0	40	μA
		V_{CC} = Max, V_{IN} = 5 5V			1.0			1.0	mA
I_{OS}	Output short circuit current[2]	V_{CC} = Max, V_{OUT} = 0V	−15		−100	−15		−100	mA
I_{CC}	Supply current	V_{CC} = Max, inputs open		70	110		70	110	mA

NOTES 1 Commercial—V_{CC}(min) = 4 75V, V_{CC}(max) = 5 25V Military—V_{CC}(min) = 4 50V, V_{CC}(max) = 5 50V 2 No more than one output should be shorted at a time

AC ELECTRICAL CHARACTERISTICS FOR 8X01A $V_{CC} = 5V, T_A = +25°C$

PARAMETER	DESCRIPTION	FROM	TO	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
					Min	Typ	Max	Min	Typ	Max	
f_{max}	Max clock freq				12			12			MHz
PULSE WIDTHS:											
t_w-$\overline{CP}$(L)	Clock low			See figure 2	35			35			ns
t_w-$\overline{P}$(L)	Preset low			See figure 3	35			35			ns
t_w-MR(H)	Master reset high			See figure 4	35			35			ns
SETUP/HOLD TIMES:											
t_s-D	Setup time	Data	Clock		55			55			ns
t_s-CWE	Setup time	CWE	Clock	See figure 5	55			55			ns
t_h-D & CWE	Hold time	Data & CWE	Clock		0			0			ns
PROPAGATION DELAY:											
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{PRESET}$	Data output	See figures 1, 2, & 3			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Data output	See figure 4			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{PRESET}$	Error output	See figure 3			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Error output	See figure 4			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{CP}$	Data output	See figure 2			55			55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{CP}$	Error output	See figure 2			55			55	ns
t_{REC}	Recovery time	Preset, MR	Clock	See fig. 3 & 4	35			35			ns

AC ELECTRICAL CHARACTERISTICS FOR 9401 $V_{CC} = 5V, T_A = +25°C$

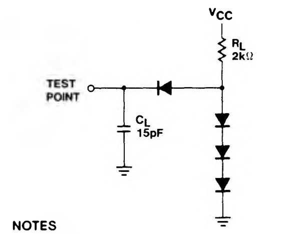
PARAMETER	DESCRIPTION	FROM	TO	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
					Min	Typ	Max	Min	Typ	Max	
f_{max}	Max clock freq				12	20		12	20		MHz
PULSE WIDTHS:											
t_w-$\overline{CP}$(L)	Clock low			See figure 2	35			35			ns
t_w-$\overline{P}$(L)	Preset low			See figure 3	40	30		40	30		ns
t_w-MR(H)	Master reset high			See figure 4	35	25		35	25		ns
SETUP/HOLD TIMES:											
t_s-D	Setup time	Data	Clock		55	35		55	35		ns
t_s-CWE	Setup time	CWE	Clock	See figure 5	55	35		55	35		ns
t_h-D & CWE	Hold time	Data & CWE	Clock		0	−8		0	−8		ns
PROPAGATION DELAY:											
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{PRESET}$	Data output	See figures 1, 2, & 3		40	60		40	60	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Data output	See figure 4		30	55		30	55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{PRESET}$	Error output	See figure 3		40	60		40	60	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	Master reset	Error output	See figure 4		40	60		40	60	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{CP}$	Data output	See figure 2		30	55		30	55	ns
$t_{PLH,PHL}$	Low-to-High and High-to-Low	$\overline{CP}$	Error output	See figure 2		40	60		40	60	ns
t_{REC}	Recovery time	Preset, MR	Clock	See fig. 3 & 4	35	25		35	25		ns

CRC GENERATOR/CHECKER

8X01A/9401

PRELIMINARY

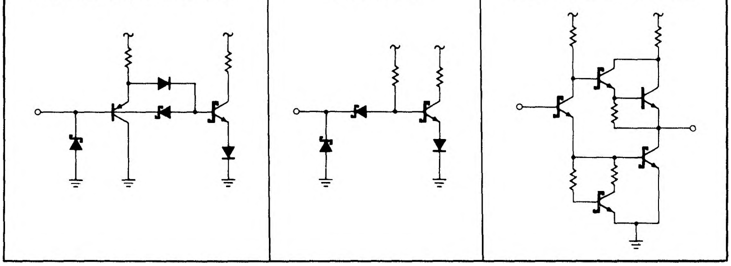
TEST CIRCUIT

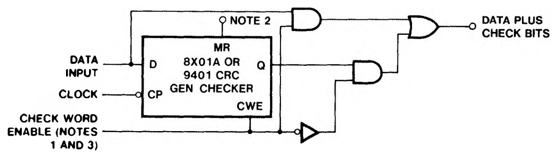


NOTES
1 Diodes are 1N3064 or equivalent
2 C_L includes jig and probe capacitance

INPUT/OUTPUT STRUCTURES

ALL INPUTS, EXCEPT $\overline{CP}$ | $\overline{CP}$ INPUT | OUTPUT STRUCTURE





NOTES
1 Check Word Enable is HIGH while data is being clocked, it is LOW during transmission of check bits
2 The 8X01A (or 9401) must be RESET or PRESET before each computation
3 CRC check bits are generated and appended to data bits

Figure 1. Check Word Generation

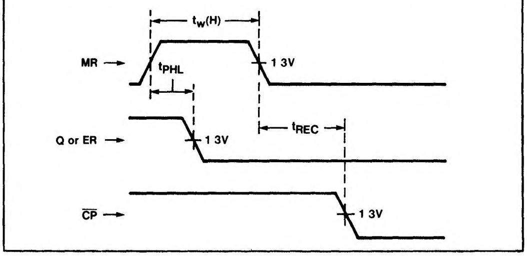


Figure 4. Propagation Delay—MR to Q and ER; Recovery Time—MR to $\overline{CP}$

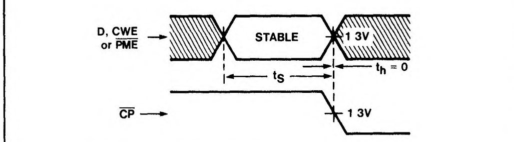


Figure 5. Setup and Hold Times—D to $\overline{CP}$, CWE to $\overline{CP}$, and $\overline{PME}$ to $\overline{CP}$

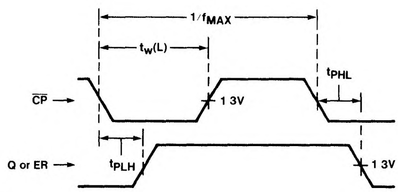


Figure 2. Propagation Delay—$\overline{CP}$ to Q and $\overline{CP}$ to ER

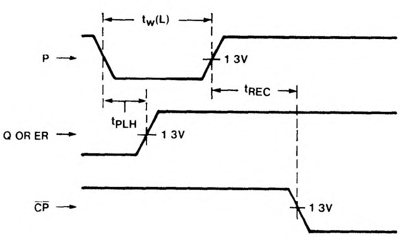


Figure 3. Propagation Delay—$\overline{P}$ to Q and ER; Recovery Time—$\overline{P}$ to $\overline{CP}$.