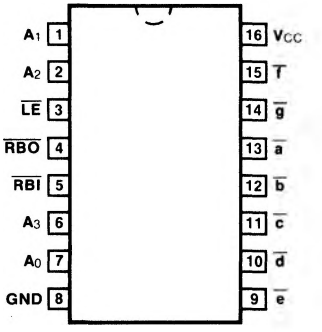
9374

7-SEGMENT DECODER/DRIVER/LATCH

(With Constant Current Sink Outputs)

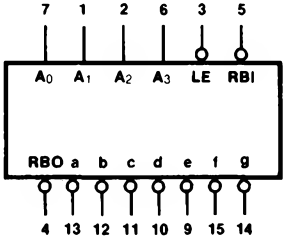
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '74 is a 7-segment decoder driver incorporating input latches and output circuits to directly drive common anode LED displays.

- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **15 mA CONSTANT CURRENT SINK CAPABILITY TO DIRECTLY DRIVE COMMON ANODE LED DISPLAYS**
- **INCREASES INCANDESCENT DISPLAY LIFE**
- **ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS**
- **DATA INPUT LOADING ESSENTIALLY ZERO WHEN LATCH DISABLED**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING AND/OR TRAILING-EDGE ZEROES**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	PKG TYPE
Plastic DIP (P)	A	9374PC	9B
Ceramic DIP (D)	A	9374DC	6B

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$A_0 - A_3$	Address (Data) Inputs	1.0/0.25**
$\overline{LE}$	Latch Enable Input (Active LOW)	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	0.5/0.25
$\overline{RBO}$	Ripple Blanking as Output (Active LOW)	1.0/0.5
	as Input (Active LOW)	-/0.75
$\overline{a} - \overline{g}$	Constant Current Outputs (Active LOW)	OC*/15 mA

*OC — Open Collector
**Except Loading is 10 μA @ 0.4 V when $\overline{LE}$ is HIGH.

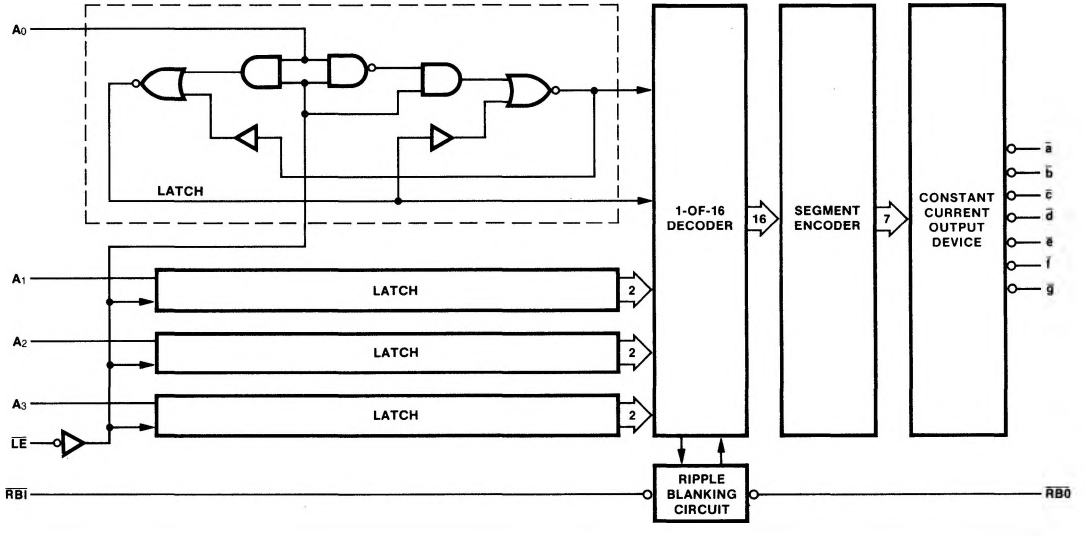
FUNCTIONAL DESCRIPTION—The '74 is a 7-segment deconder/driver with latches on the address inputs and active LOW constant current outputs to drive LEDs directly. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a decode format which produces numeric codes "0" through "9" and other codes.

Latches on the four data inputs are controlled by an active LOW Latch Enable, $\overline{LE}$. When $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 50 ns, which allows data to be strobed into the '74 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

The latch/decoder combination is a simple system which drives LED displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs, since several circuits — seven resistors per display, strobe drivers, a separate display voltage source, and clock failure detect circuits — traditionally found in multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.

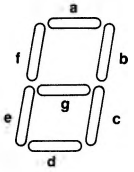
Another '74 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only 10 μA typ). This allows many '74s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The '74 also provides automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar precedure for the fractional part of a display will provide automatic suppression of trailing-edge zeros. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

LOGIC DIAGRAM



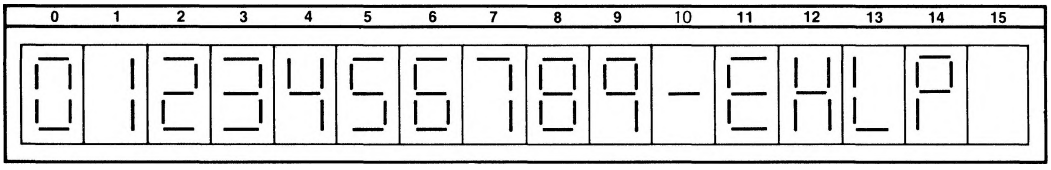
TRUTH TABLE

BINARY STATE	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	
—	H	*	X	X	X	X	←			STABLE			→	H	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	BLANK
X	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	BLANK



*The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
**$\overline{RBO}$ used as an input overrrides all other input conditions.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NUMERICAL DESIGNATIONS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	UNITS	CONDITIONS
V_{OUT}	Output Voltage, Applied	OFF		10 (Fig. a)	V	Separate LED Supply
		ON				
I_{OL}	Output LOW Current, $\overline{a}$—$\overline{g}$		12	18	mA	V_{CC} = 5.0 V, V_{OL} = 3.0 V T_A = 25°C
I_{OH}	Output HIGH Current $\overline{a}$—$\overline{g}$			250	μA	V_{CC} = Max, V_{OUT} = 5.5 V
I_{CC}	Power Supply Current			50	mA	V_{CC} = Max, V_{IN} = Gnd V_{OUT} = 3.0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF R_L = 1 kΩ Min	93XX C_L = 15 pF R_L = 1 kΩ Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{a}$—$\overline{g}$		140 140	ns	Figs. 3-2, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to $\overline{a}$—$\overline{g}$		140 140	ns	Figs. 3-2, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	93XX Min	93XX Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{LE}$	75 30		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to $\overline{LE}$	0 0		ns	
t_w (L)	$\overline{LE}$ Pulse Width LOW	85		ns	Fig. 3-9

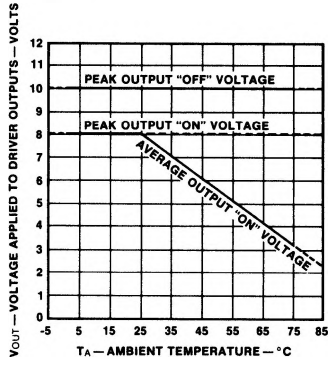


Fig. a Output Voltage Safe Operating Area

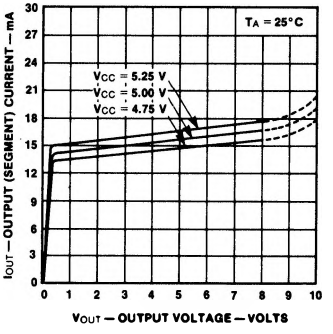


Fig. b Typical Constant Segment Current Versus Output Voltage

APPLICATIONS — It is possible with common anode 7-segment LED displays and constant current sink decoder drivers to save substantial amounts of power by carefully choosing operating points on display supply voltage. First, examine the power used in the normal display driving method where the display and decoder driver are both operated from a +5.0 V regulated supply ($V_{CC} = V_S$).

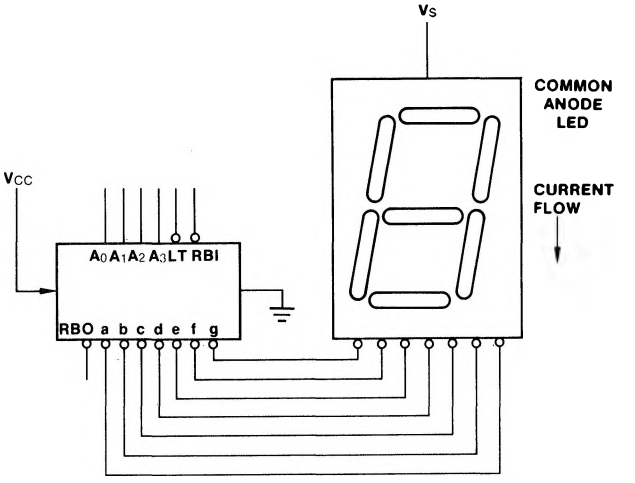


Fig. c Separate Supply for LED Displays

The power dissipated by the LED and the driver outputs is (V_{CC} x I_{seg} x n Segments). The total power dissipated with a 15 mA LED displaying an eight (8) would be:

$$P_{TOT} = 5.0\ V \times 15\ mA \times 7$$
$$= 525\ mW$$

Of this 525 mW, the power actually required to drive the LED is dependent on the V_F drop of each segment. Most GaAsP LEDs exhibit either a 1.7 V or a 3.4 V forward voltage drop. Therefore, the required total power for seven segments would be:

$$P_{(1.7)} = 1.7\ V \times 15\ mA \times 7$$
$$= 178.5\ mW$$
$$P_{(3.4)} = 3.4\ V \times 15\ mA \times 7$$
$$= 357\ mW$$

The remaining power is dissipated by the driver outputs which are maintaining the 15 mA constant current required by the LEDs. Most of this power is wasted, since the driver can maintain approximately 15 mA with as little as 0.5 V across the output device. By using a separate power source (V_S, *Figure c*) for the LEDs, which is set to the LED V_F plus the offset voltage of the driver, as much as 280 mW can be saved per digit. i.e.,

$$V_S = V_F\ (Max) + V_{offset}$$
$$= 2.0\ V + 0.5\ V$$
$$= 2.5\ V$$
$$P_T = 2.5\ V \times 14\ mA\ (from\ \textit{Figure b}) \times 7$$
$$= 245\ mW$$

These figures show that using a separate supply to drive the LEDs can offer significant display power savings. In battery powered equipment, two rechargeable nickle-cadmium cells in series would be sufficient to drive the display, while four such cells would be needed to operate the logic units.

APPLICATIONS (Cont'd) — Another method to save power is to apply intensity modulation to the displays *(Figure d)*. It is well known that LED displays are more efficient when operated in pulse mode. There are two reasons: one, the quantum efficiency of the LED material is better; secondly the eye tends to peak detect. Typically a 20% off duty cycle to displays (GaAsP) will produce the same brightness as operating under dc conditions.

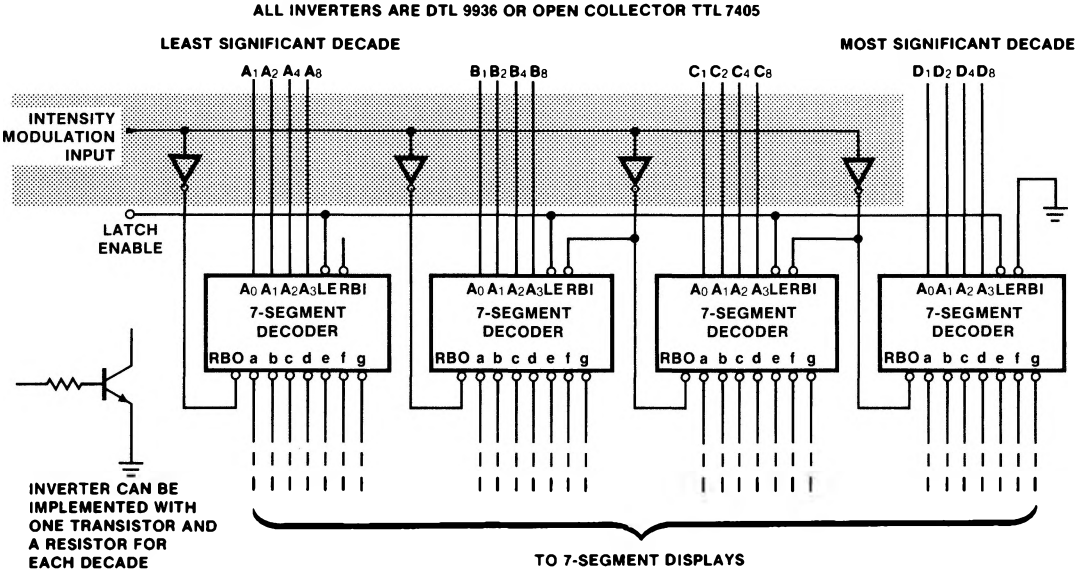


Fig. d Intensity Control by $\overline{\text{RBO}}$ Pulse Duty Cycle

Low Power, Low cost Display Power Sources — In small line operated systems using TTL/MSI and LED or incandescent displays, a significant portion of the total dc power is consumed to drive the displays. Since it is irrelevant whether displays are driven from unfiltered dc or pulsed dc (at fast rates), a dual power system can be used that makes better utilization of transformer rms ratings. The system utilizes a full wave rectified but unsmoothed dc voltage to provide the displays with 120 Hz pulsed power while the rest of the system is driven by a conventional dc power circuit. The frequency of 120 Hz is high enough to avoid display flicker problems. The main advantages of this system are:

- Reduced transformer rating
- Much smaller smoothing capacitor
- Increased LED light output due to pulsed operation

With the standard capacitor filter circuit, the rms current (full wave) loading of the tranformer is approximately twice the dc output. Most commercial transformer manufacturers rate tranformers with capacitive input filters as follows:

Full Wave Bridge Rectifier Circuit
Transformer rms current = 1.8 x dc current required

Full Wave Center Tapped Rectifier Circuit
Transformer rms current = 1.2 x dc current required

Therefore, the removal of a large portion of the filtered dc current requirement (display power) substantially reduces the transformer loading.

APPLICATIONS (Cont'd) — There are two basic approaches. First *(Figure e)* is the direct full wave rectified unregulated supply to power the displays. The '74 decoder driver constant current feature maintains the specified segment current after the LED diode drop and 0.5 V saturation voltage has been reached (≅2.2 V). Care must be exercised not to exceed the '74 power ratings and the maximum voltage that the decoder driver sees in both the "on" and "off" modes.

The second approach *(Figure f)* uses a 3-terminal voltage regulator such as the 7805 to provide dc pulsed power to the display with the peak dc voltage limited to +5.0 V. This approach allows easier system thermal management by heat sinking the regulator rather than the display or display drivers. When this power source is used with an intensity modulation scheme or with a multiplexed display system, the frequencies must be chosen such that they do not beat with the 120 Hz full wave rectified power frequency.

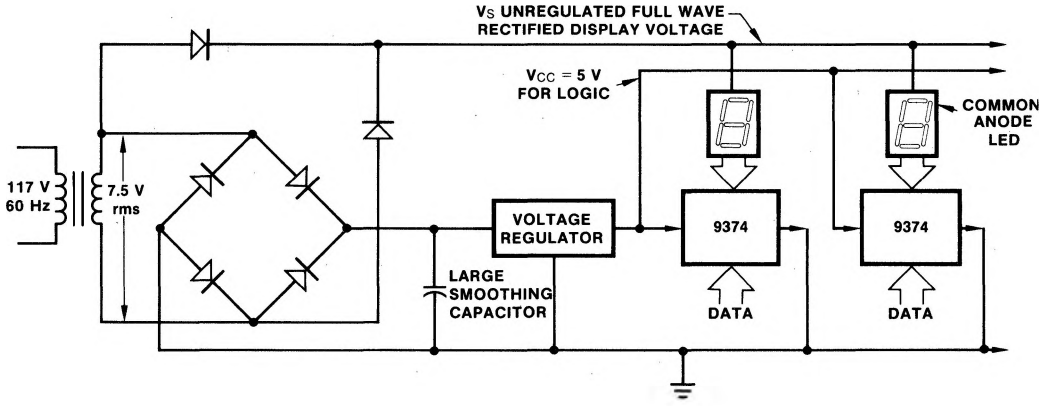


Fig. e Direct Unregulated Display Supply

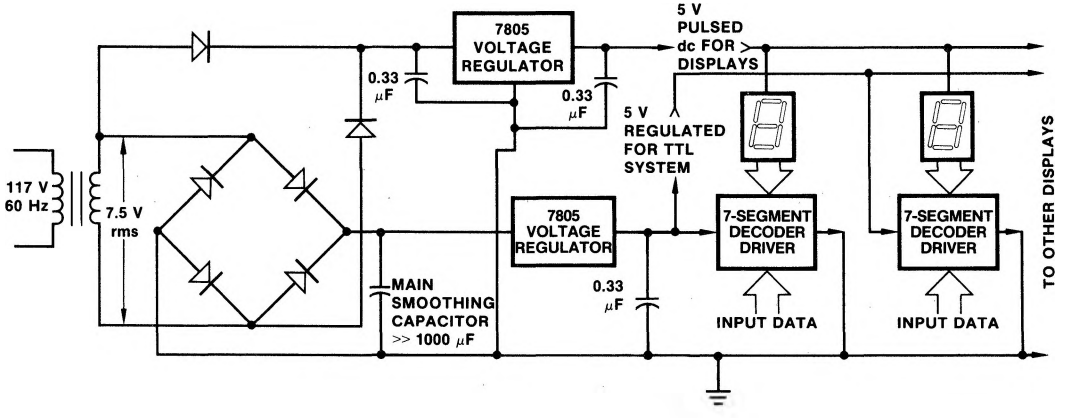


Fig. f Pulsed Regulated Display Supply

PARALLEL DATA SUPPLY SYSTEM WITH RIPPLE BLANKING