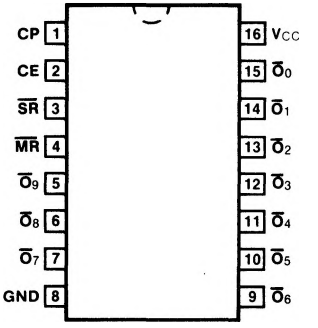
9319 • 9320

DECADE SEQUENCERS

DESCRIPTION — The '19 and '20 are high speed counters with ten decoded active LOW outputs. The '19 has standard TTL totem pole outputs, and the '20 has resistor pull-up outputs for wired-AND applications. The devices provide a 1-of-10 sequential output pattern by the application of ten pulses to the Clock input. Shorter sequences can be obtained by using external feedback, either hard-wired or programmable via multiplexing.

- **COMBINATION DECADE COUNTER AND 1-OF-10 DECODER**
- **GLITCHLESS, SEQUENTIAL 1-OF-10 OUTPUT PATTERN**
- **IDEAL FOR MULTIPHASE CLOCK GENERATION**
- **ANY SEQUENCE BETWEEN TWO AND TEN OBTAINABLE**
- **HIGH SPEED CLOCK INPUTS — TYPICALLY 50 MHz**
- **WIRED-AND CAPABILITY (9320 ONLY)**

CONNECTION DIAGRAM
PINOUT A



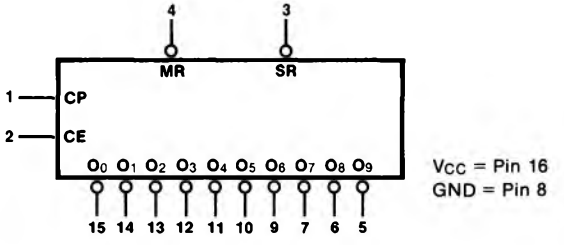
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9319PC, 9320PC		9B
Ceramic DIP (D)	A	9319DC, 9320DC	9319DM, 9320DM	6B
Flatpak (F)	A	9319FC, 9320FC	9319FM, 9320FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

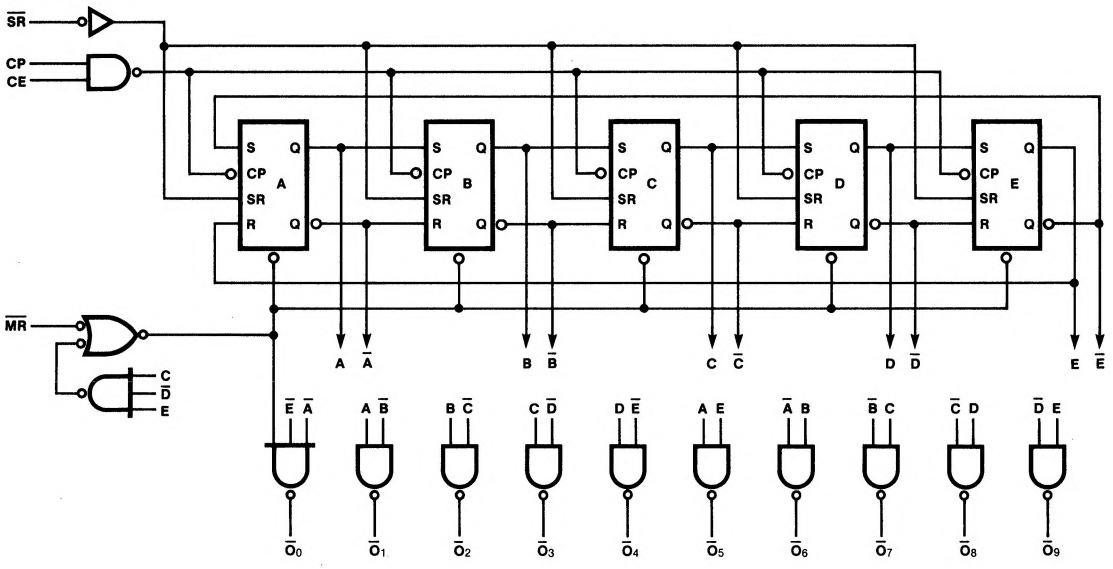
PIN NAMES	DESCRIPTION	9319 (U.L.) HIGH/LOW	9320 (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	1.0/1.0
$\overline{CE}$	Clock Enable Input	1.0/1.0	1.0/1.0
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/1.0	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	1.0/1.0
$\overline{O}_0 - \overline{O}_9$	Decoded Outputs (Active LOW)	20/10	3.0/10

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS									
	$\overline{MR}$	$\overline{SR}$	CE	CP	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	•	•	•	•	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$
Initialize, Asynchronous Reset	L	X	X	X	H	H	H					H	H	H
	L→H	X	(quiescent)		L	H	H					H	H	H
Synchronous Reset	H	L	H	⌐	L	H	H					H	H	H
Hold	H	X	L	X	(No Change)									
Sequence/Count	H	H	H	⌐	L	H	H	•	•	•	•	H	H	H
	H	H	H	⌐	H	L	H	•	•	•	•	H	H	H
	H	H	H	⌐	H	H	L	•	•	•	•	H	H	H
	•	•	•	•	•	•	•					•	•	•
	•	•	•	•	•	•	•					•	•	•
	•	•	•	•	•	•	•					•	•	•
	•	•	•	•	•	•	•					•	•	•
	H	H	H	⌐	H	H	H	•	•	•	•	L	H	H
	H	H	H	⌐	H	H	H	•	•	•	•	H	L	H
	H	H	H	⌐	H	H	H	•	•	•	•	H	H	L
	H	H	H	⌐	L	H	H	•	•	•	•	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

FUNCTIONAL DESCRIPTION — The '19 and '20 are decade shift counters with active LOW 1-of-10 decoded outputs. The decoded shift counter technique provides ten mutually exclusive, glitchless outputs. The edge-triggered counter is advanced on each LOW-to-HIGH transition of the Clock input (CP). When the Clock Enable ($\overline{CE}$), Synchronous Reset ($\overline{SR}$), Master Reset ($\overline{MR}$) are HIGH, the device is sequenced via the Clock thru output states $\overline{O}_0 - \overline{O}_9$, successively.

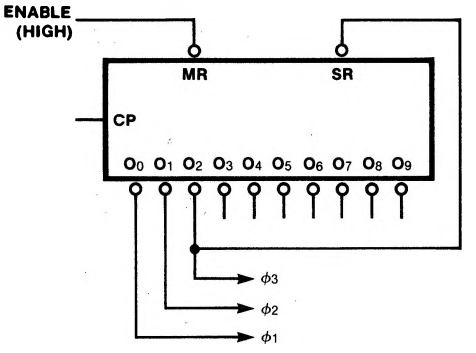
The active HIGH Count Enable ($\overline{CE}$) input is gated with the Clock and can be interchanged with Clock for layout convenience. A LOW on the $\overline{CE}$ input inhibits the Clock and stops the counter. By returning one of the outputs to the $\overline{CE}$ input, the device will sequence up to that output state and stop until reset with the Master Reset. Because the $\overline{CE}$ input is gated with the CP input, it cannot be changed from LOW to HIGH while the CP is HIGH.

The active LOW Synchronous Reset ($\overline{SR}$) is used to reset the counter to zero (returning the output to the $\overline{O}_0$ state) in response to the LOW-to-HIGH transition of the Clock. Any sequence between "two" and "ten" can be obtained by connecting the last desired output to the $\overline{SR}$ input. This method of truncating the sequence produces a series of pulses of equal duration as long as the clock frequency remains constant.

A LOW on the Master Reset ($\overline{MR}$) overrides all other input conditions and resets the counter to zero. As long as the $\overline{MR}$ is LOW, all of the outputs are HIGH. When the $\overline{MR}$ goes from LOW to HIGH, the zero output ($\overline{O}_0$) goes LOW. This $\overline{MR}$ gating with the $\overline{O}_0$ output insures complete system resetting or initialization before the first output in the sequencer is activated. For low frequency applications (below 1.0 MHz) the $\overline{MR}$ can be used in lieu of the $\overline{SR}$ for truncating the count sequence. If the input CP rise time is very slow (over 100 ns), the $\overline{MR}$ input should be used to reset the counter to avoid mis-triggering. This is accomplished by returning the next higher output to the $\overline{MR}$ pin. After the desired sequence is completed, the next clock pulse will reset the counter and enable the first output within 50 ns.

The outputs of the '19 are standard TTL totem pole type which can drive up to ten standard TTL unit loads. The outputs of the '20 are DTL resistor pull-up type for applications requiring wired-AND connections. The on-chip pull-up resistors, (about 3 kΩ) of the '20 eliminate the need for external resistors normally required by open-collector outputs. Up to eight '20 outputs can be tied together with enough sink current capability left to drive one standard TTL input or five 93L or 54LS/74LS inputs.

The '19 and '20 will normally require initialization after power is first applied. A LOW pulse on the Master Reset (or a LOW on the Synchronous Reset in conjunction with a clock pulse) will reset the 5-bit register and activate output $\overline{O}_0$. If initialization is not possible or not required, an error correction circuit is provided to detect some of the 22 unused states and return the counter to the proper sequence within ten clock cycles.



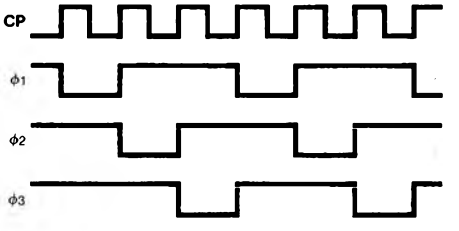
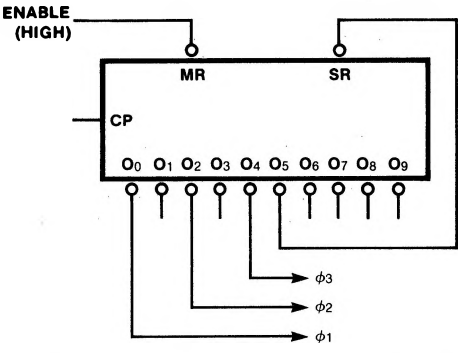


Fig. a Three-Phase Generator Operating at One-Third the Clock Frequency



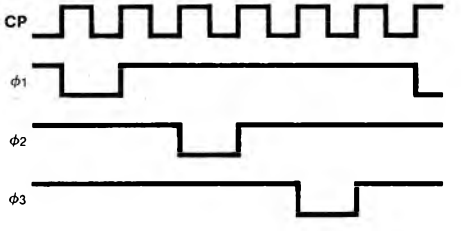


Fig. b Three-Phase Generator Operating at One-Sixth the Clock Frequency

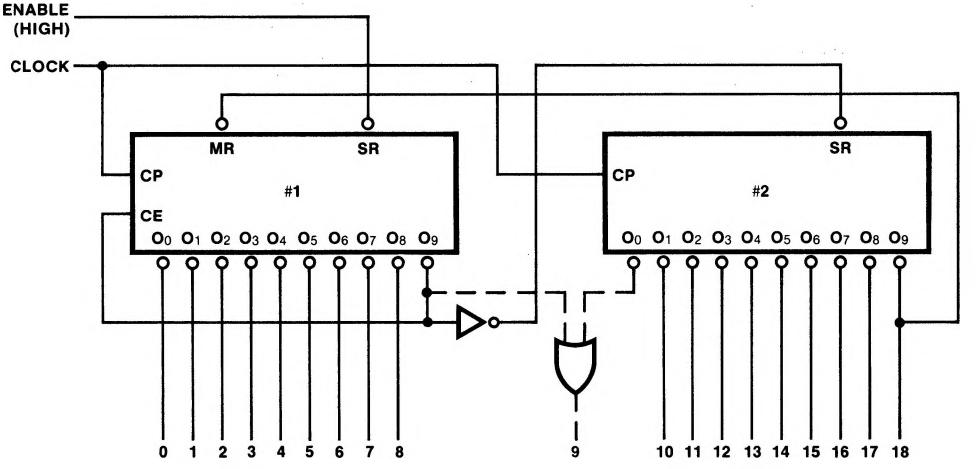


Fig. c Expansion for longer sequences. The first sequencer locks up after $\overline{O}_9$ goes LOW because of the feedback to CE. Simultaneously, $\overline{SR}$ of the second sequencer is released and it starts counting on the next clock. When $\overline{O}_9$ of the second sequencer goes LOW, the feedback to $\overline{MR}$ causes $\overline{O}_9$ of the first sequencer to go HIGH, which then makes $\overline{SR}$ of the second sequencer go HIGH. On the next clock the second sequencer goes to the $\overline{O}_0$ state, releasing $\overline{MR}$ of the first sequencer, making its $\overline{O}_0$ go LOW. On the next clock the first sequencer starts its counting sequence again.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	9319		9320		UNITS	CONDITIONS
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage			2.4		V	I_{OH} = -120 μA
I_{OS}	Output Short Circuit Current			-1.3	-3.7	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		60		60	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	9319		9320		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF, R_L = 400 Ω			
		Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	35		35		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$		40 30		40 30	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to $\overline{O}_n$		50 33		50 33	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	9319		9320		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SR}$ to CP	10 10		10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SR}$ to CP	5.0 5.0		5.0 5.0		ns	
t_w	CP Pulse Width	15		15		ns	Fig. 3-16
t_w (L)	$\overline{MR}$ or $\overline{SR}$ Pulse Width LOW	9.0		9.0		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	35		35		ns	Fig. 3-16