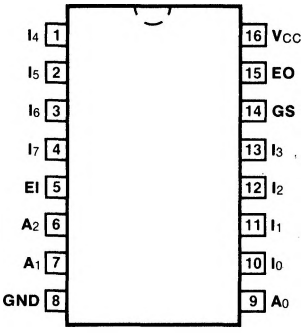
9318
93L18
8-INPUT PRIORITY ENCODER

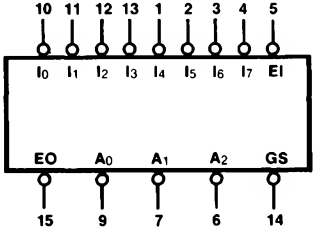
DESCRIPTION — The '18 multipurpose encoders are designed to accept eight inputs and produce a binary weighted code of the highest order input.

- **MULTIFUNCTION CAPABILITY**
  - **CODE CONVERSIONS**
  - **MULTI-CHANNEL D/A CONVERTER**
  - **DECIMAL TO BCD CONVERTER**
- **CASCADING FOR PRIORITY ENCODING OF N BITS**
- **INPUT ENABLE CAPABILITY**
- **PRIORITY ENCODING — AUTOMATIC SELECTION OF HIGHEST PRIORITY INPUT LINE**
- **OUTPUT ENABLE — ACTIVE LOW WHEN ALL INPUTS HIGH**
- **GROUP SIGNAL OUTPUT — ACTIVE WHEN ANY INPUT IS LOW**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

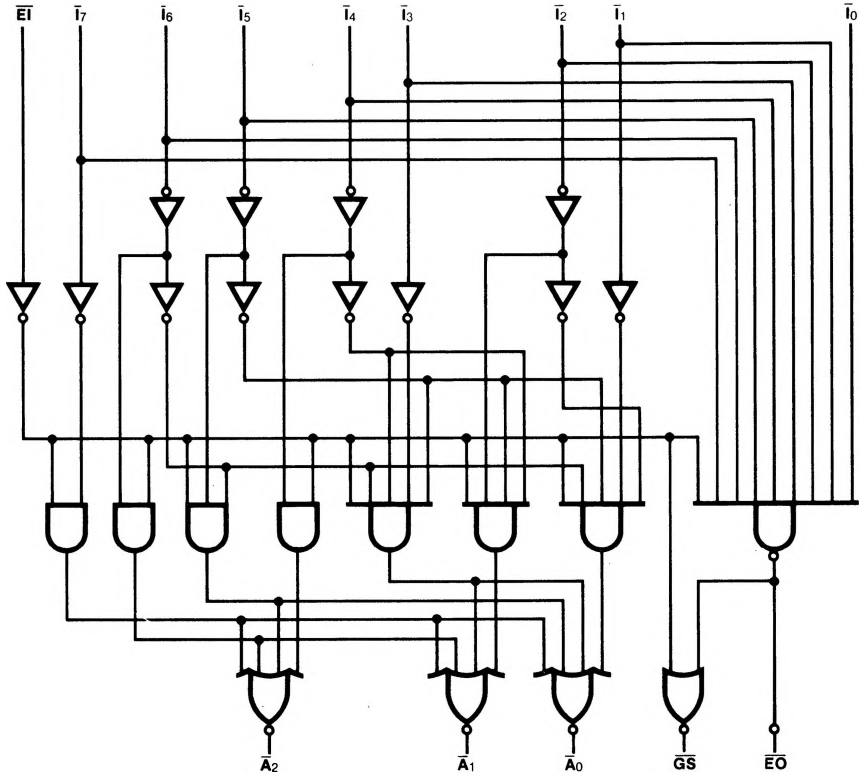
PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9318PC, 93L18PC		9B
Ceramic DIP (D)	A	9318DC, 93L18DC	9318DM, 93L18DM	6B
Flatpak (F)	A	9318FC, 93L18FC	9318FM, 93L18FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$\overline{I_0}$	Priority Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{I_1} - \overline{I_7}$	Priority Inputs (Active LOW)	2.0/2.0	1.0/0.5
$\overline{EI}$	Enable Input (Active LOW)	2.0/2.0	1.0/0.5
$\overline{EO}$	Enable Output (Active LOW)	20/10	10/5.0 (3.0)
$\overline{GS}$	Group Select Output (Active LOW)	20/10	10/5.0 (3.0)
$\overline{A_0} - \overline{A_2}$	Address Outputs (Active LOW)	20/10	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '18 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal output ($\overline{GS}$) and Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are in the inactive HIGH state when the input enable is HIGH.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current $\overline{I}_0$ - $\overline{I}_7$, $\overline{EI}$		1.0			mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{OS}	Output Short Circuit Current	-20	-70			mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		77		22	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{EO}$		10 18		18 50	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{GS}$		14 16		20 28	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{EO}$		14 22		20 36	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{A}_n$		17 17		33 26	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{GS}$		14 16		60 26	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{A}_n$		21 21		36 36	ns	Figs. 3-1, 3-20