signetics

DUAL SENSE AMPLIFIER | 8T25

V PACKAGE N8T25 0°C TO +75°C

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8T25 is a Dual MOS-to-TTL Sense Amplifier designed to accept low level MOS signals from the output of Random Access Memories and store the information in a latch in response to an external Strobe signal. A tristate buffer presents the data to the output using conventional TTL logic levels. The 8T25 operates from a single +5 volt supply.

CIRCUIT OPERATION

A logic "1" level on the Disable line will effectively disconnect the outputs of the Sense Amplifier from a common bus by turning both totem-pole transistors off. When the Disable line returns to a logic "0" level, the outputs will be preset to a logic "1" state. A low-going Strobe pulse will then transfer the data at Inputs A and B to their respective outputs non-inverted.

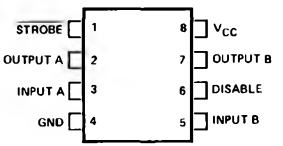
Due to the internal latch, output data will remain stable regardless of any change in input levels until a Disable signal again forces both outputs to the high impedance state.

The data inputs are current sensitive with a threshold of 300μA, although the driving source voltage must be greater than 1.6 volts in the high level.

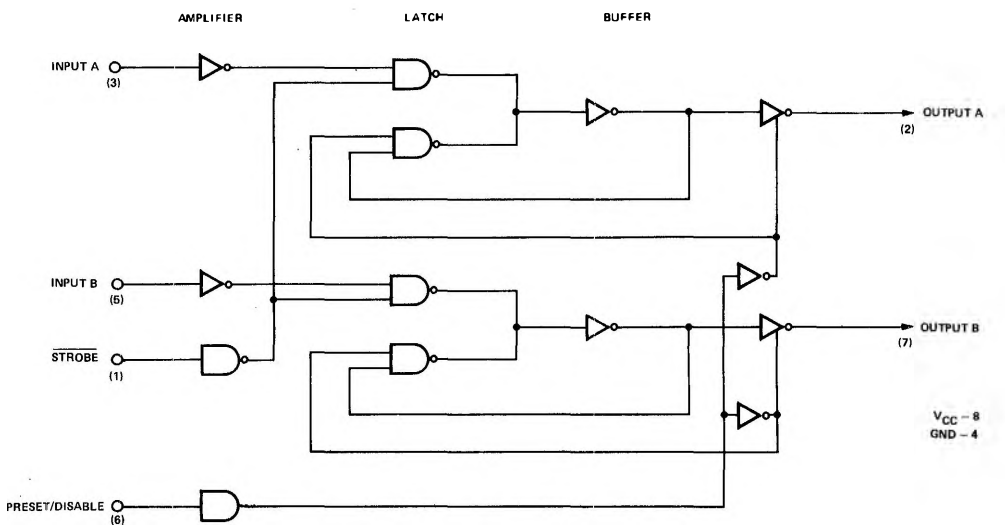
FEATURES

- MOS-TO-TTL CONVERTER
- INTERNAL LATCH
- TRISTATE OUTPUTS
- SINGLE +5V SUPPLY

PIN CONFIGURATION



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 0°C TO 75°C, V_{CC} = 5V ± 5%)

PARAMETER	LIMITS				INPUTS					
	MIN.	TYP.	MAX.	UNITS	A	B	DISABLE	STROBE	OUTPUTS	NOTES
"1" Output Voltage	2.8	3.5		V	400μA	400μA	0.8V	0.8V	-1.5mA	7
"0" Output Voltage			0.40	V	200μA	200μA	0.8V	0.8V	16mA	8
Output "1" Leakage Current										
Output "A"			100	μA	200μA	1.5mA	2.0V	0.8V	3.9V	
Output "B"			100	μA	1.5mA	200μA	2.0V	0.8V	3.9V	
Output "0" Leakage Current			100	μA	1.5mA	1.5mA	2.0V	0.8V	OV	
Input Clamp Voltage			-1.5	V			-12mA	-12mA		
Power/Current Consumption			210/40	mW/mA	400μA	400μA	4.5V	OV		11
"0" Input Current (Strobe, Disable)	-0.1		-1.6	mA			OV	OV		
"1" Input Current (Strobe, Disable)			40	μA			4.5V	4.5V		
Input Voltage Rating (Strobe, Disable)			5.5	V			1.0mA	1.0mA		
Output Short Circuit Current	-20		-70	mA				2.0V	OV	10, 11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Not more than one output should be shorted at a time.
10. V_{CC}=6.25V.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

PARAMETER	LIMITS				INPUTS					
	MIN.	TYP.	MAX.	UNITS	A	B	DISABLE	STROBE	OUTPUTS	NOTES
Propagation Delay										
Strobe to Output (t_{ds})		15	25	ns						Fig. 1
Disable to "0" Output (t_{PZL})		15	25	ns						Fig. 2
"0" Output to Disable (t_{PLZ})		8	15	ns						Fig. 2
Disable to "1" Output (t_{PZH})		15	25	ns						Fig. 3
"1" Output to Disable (t_{PHZ})		9	20	ns						Fig. 3

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (STROBE TO OUTPUT)

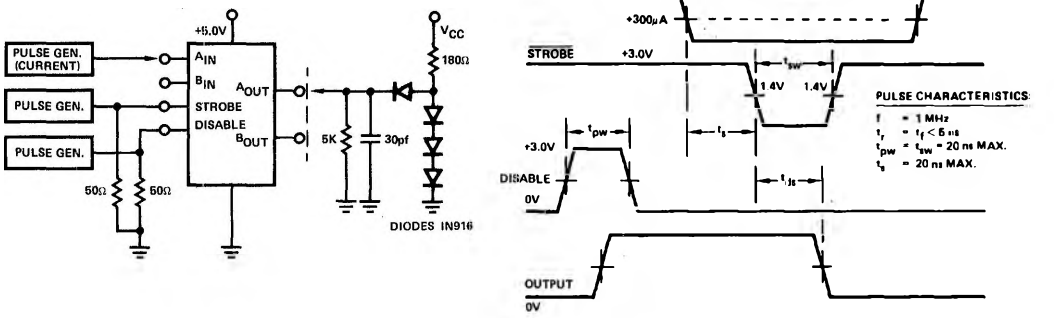
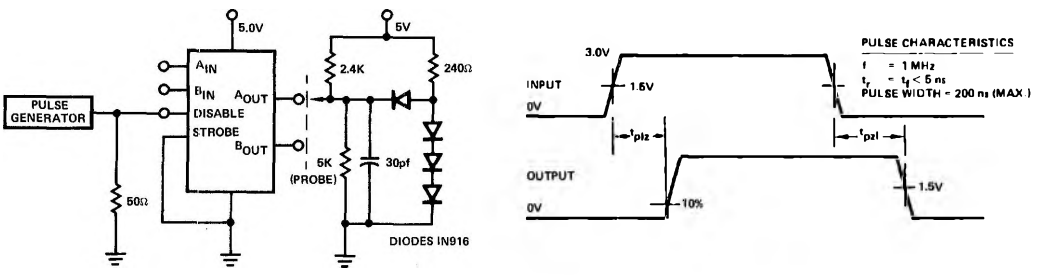


Fig. 1

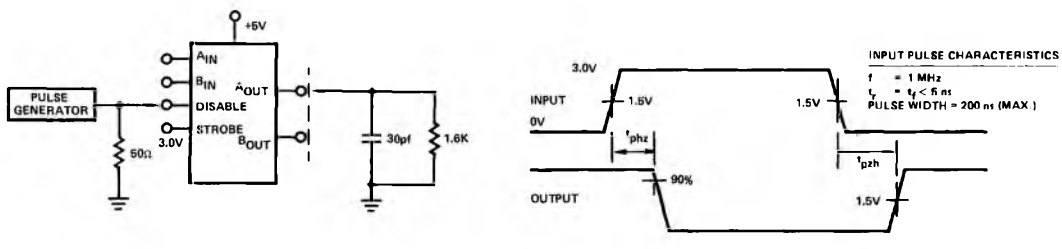
PROPAGATION DELAY (DISABLE TO OUTPUT)



NOTE: t_{plz} = "0" OUTPUT TO HIGH–Z
t_{pzl} = HIGH–Z TO "0" OUTPUT

Fig. 2

PROPAGATION DELAY (DISABLE TO OUTPUT)



NOTE: t_{phz} = "1" OUTPUT TO HIGH–Z
t_{pzl} = HIGH–Z TO "0" OUTPUT

Fig. 3

TYPICAL APPLICATION