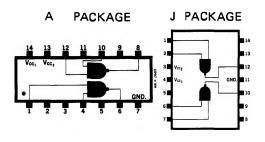
SIGNETICS 8T18 DUAL 2-INPUT NAND INTERFACE GATE INTEGRATED CIRCUITS



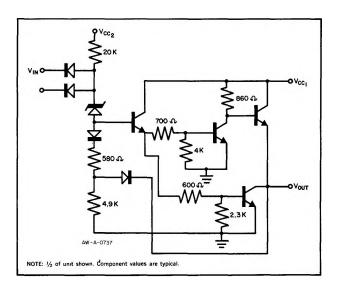
BASIC CIRCUIT SCHEMATIC

The 8T18 is a Dual 2-Input NAND Interface Gate. It is a high to low voltage interface gate which provides translation from up to 30-volt logic levels to standard logic levels of 5 volts.

The basic gate operates from two power supplies. The input structure functions from a high voltage supply between 20V and 30V and the second stage transistors and output structure operate from a standard 5V power supply.

The output structure features active pull-up and pull-down, providing a low impedance driving source in both "1" and "0" output states. This configuration is particularly suited for driving the high capacitance loads encountered in high fan-out and line driving applications.

Section 4 provides usage rules and applications information for the 8T18.



ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS							
		MIN.	TYP.	MAX.	UNITS	TEMP. S8T18	TEMP, N8T18	v _{cc} 1	v _{ee2}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5 A-3 A-4	"1" OUTPUT VOLTAGE	3,4 3.6 3,4			v v v	-55°C +25°C +125°C	0°C +25°C +75°C	4.75V 5.00V 4.75V	24.0V 24.0V 24.0V	6.5V 6.5V 6.5V		-225μA -225μA -225μA	7 7 7
A - 5 A - 3 A - 4	"0" OUTPUT VOLTAGE			0,35 0.35 0.35	v v v	-55°C +25°C +125°C	0°C +25°C +75°C	4.75V 5.00V 4.75V	20.0V 20.0V 20.0V	9.0V 9.0V 9.0V	9.0V 9.0V 9.0V	7.2mA 7.2mA 7.2mA	8 8 8
A-5 A-3 C-1	"0" INPUT CURRENT	-0.1 -0.1 -0.1		-1.8 -1.8 -1.8	mA mA mA	-55°C +25°C +125°C	0°C +25°C +75°C	5.25V 5.25V 5.25V	24.0V 24.0V 24.0V	0.35V 0.35V 0.35V	30V 30V 30V		
A-4	"1" INPUT CURRENT		. '	50	μA	+125°C	+75°C	5.00V	24.0V	30V	ov		
A-6	TURN-ON DELAY		12	20	ns	+25°C	+25°C	5.00V	24.0V			D.C. F.O. = 9	9,11
A-6	TURN-OFF DELAY		35	70	ns	+25°C	+25°C	5.00 V	24.0V			D.C. F.O. = 9	9,11
C-2	OUTPUT FALL TIME			75	ns	-55°C	0°C	4.75V	24.0V			A.C F.O. = 2	10,11
A-2	POWER CONSUMPTION (Vcc1 OUTPUT "0")			44.0	mW	+25°C	±25°C	5.25V	24.0V				
	(Per Gate) (V _{cc1} OUTPUT "1")			1.0	mW	+25°C	+25°C	5.25V	24.0V	0V			ŀ
	(V _{cc2} OUTPUT "0")			38.4	mW	+25°C	+25°C	5.25V	24.0V			!	1
	(V _{CC2} OUTPUT "1")			37.2	mW	+25°C	+25°C	5.25V	24.0V	ov			
A - 2	INPUT VOLTAGE RATING	50		i	l v	+25°C	+25*C	5.00V	24.0V	100μΑ	0V		
-	OUTPUT SHORT CIRCUIT CURRENT		-75		mA	+25°C	+25°C	5.00 V	24.0V	ov		ov	

Notes:

- All voltage and capacitance measurements are referenced to the ground terminal.

- All voltage and capacitance measurements are reterenced to the ground terminal. Terminals not specifically referenced are left electrically open.

 All measurements are taken with ground pin tied to zero volts.

 Positive current flow is defined as into the terminal referenced.

 Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".

 Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased,
- 6. Measurements apply to each gate element independently.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to $V_{\rm CC}$. One DC fan-out is defined as 0.8mA.
- 10. One AC fan-out is defined as 50pf.
- 11. Detailed test conditions for AC testing are in Section 3.