DESCRIPTION

The 8T13 is a monolithic Dual Line Driver designed to drive 50 ohm or 75 ohm coaxial transmission lines. TTL multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The outputs are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with impedances of 50Ωto 500Ω.

Key Design Benefits:

a. High-Power Drive Capability:
Specified at -75mA sink current rating at 2.4 volts (V "1" out) at 25°C.

b. Party-Line Operation:
Emitter-follower outputs enable two or more drivers to drive the same line. This permits multiple time-shared terminal connections since these drivers have no effect upon the transmission line unless activated.

c. Input gating structure allows employment of the "OR" as well as the "AND" function.

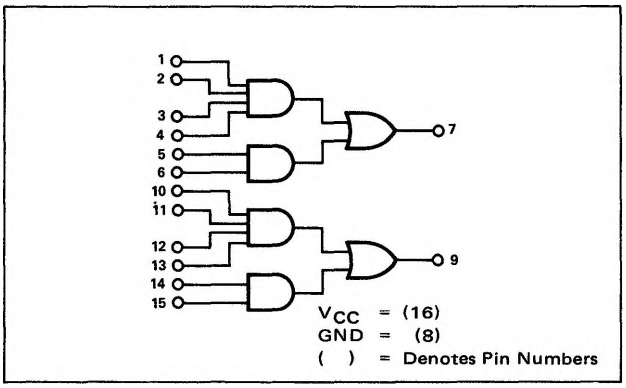
d. High Speed: $t_{on} = t_{off} = 20ns$ (max).

e. Input Clamp Diodes: Protects inputs from line ringing.

f. Single 5 Volt power supply.

g. Short Circuit Protection:
Incorporates a latch-back short circuit protection feature which protects the device by limiting the current it may source when operating under conditions of zero load resistance.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
					AND GATE #1		INPUTS OF #2 AND GATE	OUTPUTS	
	MIN.	TYP.	MAX.	UNITS	INPUT UNDER TEST	OTHER INPUTS			
"1" Output Voltage	2.4			V	2.0V	2.0V	0.8V	-75mA	6
"1" Output Leakage Current			80	μA	0V	0V	0V	3.0V	7
"0" Output Leakage Current			-800	μA	0.8V	4.5V	0V	0.4V	
"0" Input Current	-0.1		-1.6	mA	0.4V	4.5V			
"1" Input Current			40	μA	4.5V	0V			

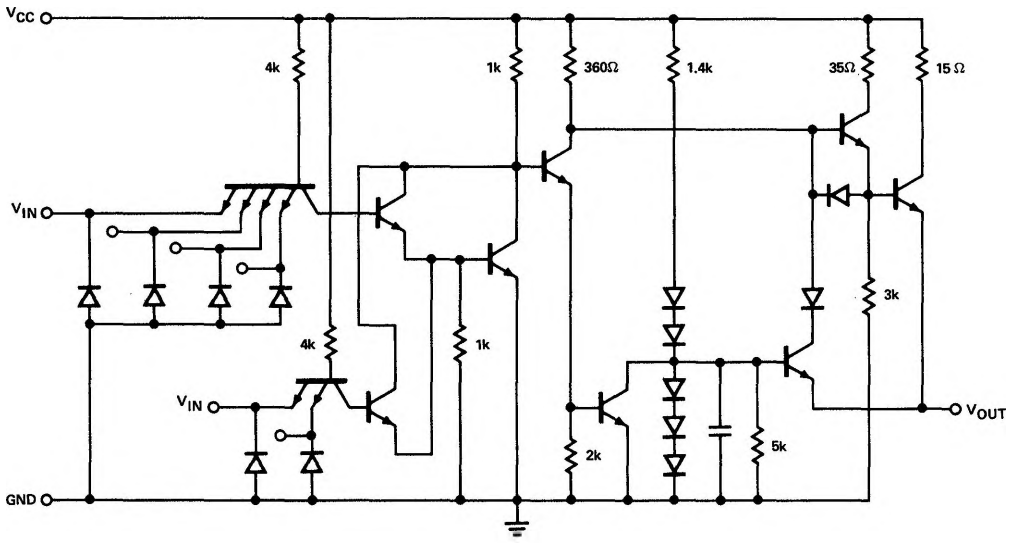
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS				NOTES
					AND GATE NO. 1		INPUTS OF NO. 2 AND GATE	OUTPUTS	
	MIN.	TYP.	MAX.	UNITS	INPUT UNDER TEST	OTHER INPUTS			
Turn-On Delay			20	ns					8.13
		32		ns					9.13
Turn-Off Delay			20	ns					8.13
		22		ns					9.13
Power/Current Consumption:									
Output at "0"			315/60	mW/mA	0.8V	0.8V	0.8V		12.15
Output at "1"			150/28	mW/mA	2.0V	2.0V	2.0V		12.15
Input Latch Voltage	5.5			V	10mA	0V	0V		11
"1" Output Current	-100		-250	mA	4.5V	4.5V	0V	2.0V	14
Output Short Circuit			-30	mA	4.5V	4.5V	0V	0V	14
Input Clamp Voltage			-1.5	V	-12mA				

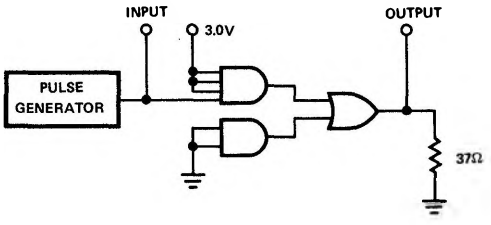
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. With forced output voltage of 3 volts no more than 500 μA will enter the driver when output is in "0" state. V_{CC} = 0V.
8. R_L = 37Ω to ground.
9. Load is 37Ω in parallel with 1000pF.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
12. I_{CC} is dependent upon loading. I_{CC} limit specified is for no-load test condition.
13. Reference AC Test Figure and Pulse Requirements.
14. Reference "Typical Output Current vs Output Voltage Curve."
15. V_{CC} = 5.25 volts. Power Consumption specified for both drivers in package.

SCHEMATIC DIAGRAM

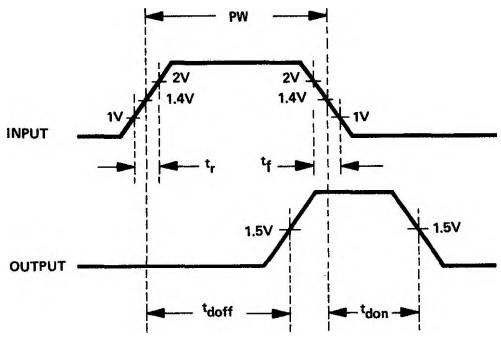


AC TEST FIGURE AND WAVEFORMS

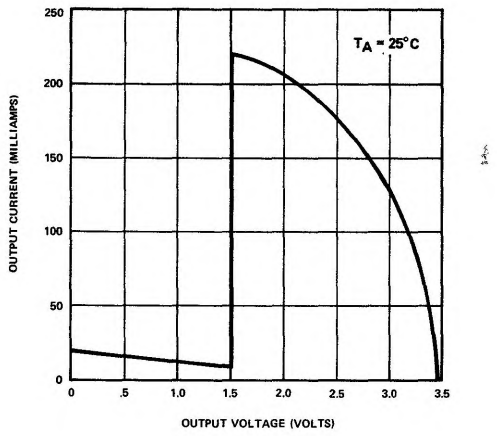


INPUT PULSE:
Amplitude = 3.0V
PW = 40ns (50% Duty Cycle)
$t_r = t_f \leq 5$ns (10% and 90% measurement points)

PULSE REQUIREMENTS



TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE CURVE



TYPICAL APPLICATIONS

A typical application for the 8T13 is shown in Figure 1. If only one line driver is to be used for each transmission line, the line may be terminated with 50 ohms on the receiving end only. See Figure 2.

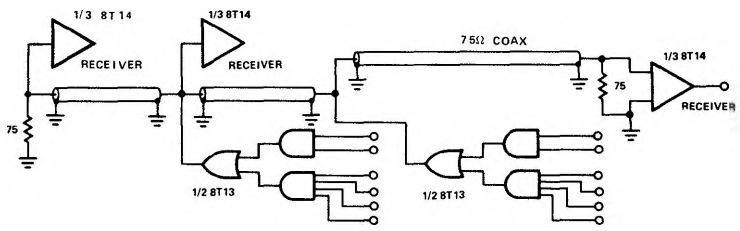


FIGURE 1

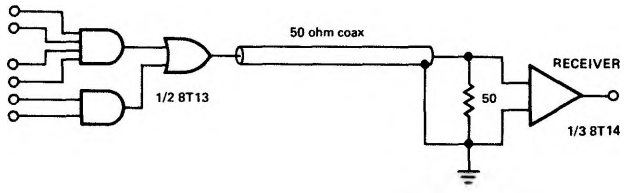


FIGURE 2