SIGNETICS DCL INTEGRATED CIRCUITS

8829 HIGH SPEED J-K BINARY

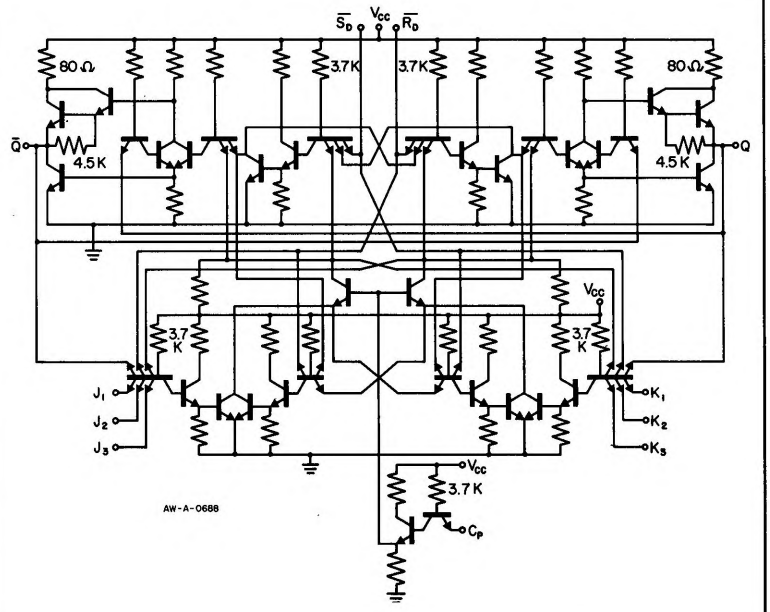
The 8829 is a high speed, direct-coupled J-K Binary which responds to the negative transition (falling edge) of the clock pulse. For logic flexibility, three J and three K inputs and asynchronous $\overline{SET}$ and $\overline{RESET}$ control lines are provided.

To prevent system errors, the 8829 features clock skew tolerances approximately equal to the clock pulse width. This feature is the result of "lock-out" of the logic inputs on the positive transition of the clock signal while the outputs are not activated until the negative transition of the clock signal.

The characterization of each logic element in the 8000 series includes loading rules for driving the 8829. A convenient summary of these DC loading rules is provided in Table 1-4, Section 1.

Detailed usage rules and application information may be found in Section 4.

BASIC CIRCUIT SCHEMATIC



TRUTH TABLE

J_n	K_n	Q_{n+1}	$\overline{S}_D$	$\overline{R}_D$	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	Q

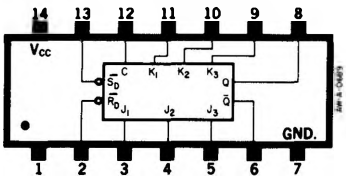
$J = J_1 J_2 J_3$ $\quad K = K_1 K_2 K_3$

n is time prior to clock

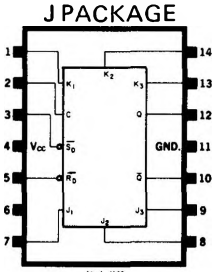
n + 1 is time following clock

† Both outputs in 0 state

A PACKAGE



J PACKAGE



8829

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 14)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	TEST LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS TEMP. S8829	TEMP. N8829	V_{cc}	SET	RESET	DRIVEN INPUT	J_1, J_2, J_3	K_1, K_2, K_3	CLOCK	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V	2.0V				OV	-500μA	7
A-3	(Q)	2.8			V	+25°C	+25°C	5.00V	0.8V	2.0V				OV	-500μA	7
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V	2.0V				OV	-500μA	7
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	2.0V	0.8V				OV	-500μA	7
A-3	($\bar{Q}$)	2.8			V	+25°C	+25°C	5.00V	2.0V	0.8V				OV	-500μA	7
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V	0.8V				OV	-500μA	7
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V	0.8V				OV	16mA	8
A-3	(Q)			0.4	V	+25°C	+25°C	5.00V	2.0V	0.8V				OV	16mA	8
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	0.8V				OV	16mA	8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	0.8V	2.0V				OV	16mA	8
A-3	($\bar{Q}$)			0.4	V	+25°C	+25°C	5.00V	0.8V	2.0V				OV	16mA	8
A-4				0.4	V	+125°C	+75°C	4.75V	0.8V	2.0V				OV	16mA	8
C-1	"0" INPUT CURRENT			-1.6	mA	-55°C	0°C	5.25V			0.4V					11
A-3	$J_1, J_2, J_3, K_1, K_2, K_3$, CLOCK	-0.1		-1.6	mA	+25°C	+25°C	5.25V			0.4V					11
C-1				-1.6	mA	+125°C	+75°C	5.25V			0.4V					11
C-1	"0" INPUT CURRENT			-4.8	mA	-55°C	0°C	5.25V			0.4V			OV		
A-3	$\bar{S}_D, \bar{R}_D$	-0.1		-4.8	mA	+25°C	+25°C	5.25V			0.4V			OV		
C-1				-4.8	mA	+125°C	+75°C	5.25V			0.4V			OV		
A-4	"1" INPUT CURRENT $J_1, J_2, J_3, K_1, K_2, K_3$, CLOCK			40	μA	+125°C	+75°C	5.00V			4.5V					
A-4	"1" INPUT CURRENT $\bar{S}_D, \bar{R}_D$			80	μA	+125°C	+75°C	5.00V			4.5V			OV		
A-6	TURN-ON DELAY			50	ns	+25°C	+25°C	5.00V							D.C. F.O. = 20	15
A-6	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.00V							D.C. F.O. = 20	15
A-6	TOGGLE RATE	15			mHz	+25°C	+25°C	5.00V								15
C-2	OUTPUT FALL TIME			50	ns	-55 C	0°C	4.75V							A.C. F.O. = 6	10,15
	INPUT SET-UP TIME		10		ns	+25°C	+25°C	5.00V								13,15
	INPUT TIME, T_x		10		ns	+25°C	+25°C	5.00V								13,15
C-2	INPUT CAPACITANCE $J_1, J_2, J_3, K_1, K_2, K_3$, CLOCK			3.0	pf	+25°C	+25°C	5.00V			2.0V					6
C-2	INPUT CAPACITANCE $\bar{S}_D, \bar{R}_D$			6.0	pf	+25°C	+25°C	5.00V			2.0V					6
A-2	POWER CONSUMPTION		75	132	mW	+25°C	+25°C	5.25V						OV		
C-1	INPUT LATCH VOLTAGE ALL INPUTS	5.5			V	+25°C	+25°C	5.00V			10mA					
A-2	OUTPUT SHORT Q	-20		-70	mA	+25°C	+25°C	5.00V		OV				OV	OV	
	CIRCUIT CURRENT $\bar{Q}$	-20		-70	mA	+25°C	+25°C	5.00V	OV					OV	OV	

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Capacitance as measured on Boonton Electronic Corporation Model 75A-58 Capacitance Bridge or equivalent. f = 1 MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
7. Output current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Input current measurements at J_1, J_2, J_3 require that Clock = 0V and R_D be momentarily grounded. Input current measurements at K_1, K_2, K_3 require that Clock = 0V and S_D be momentarily grounded.
12. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
13. Since logic "lock-out" occurs on the positive going transition of the clock pulse, the logic level present prior to that edge of the clock need only remain present for an additional 10ns (typ.). The logic inputs need not be stabilized again until 10ns (typ.) prior to the next positive transition of the clock. The clock skew tolerance is therefor typically the clock pulse width minus 10ns.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.