SIGNETICS DCL INTEGRATED CIRCUITS

8827 DUAL J-K BINARY

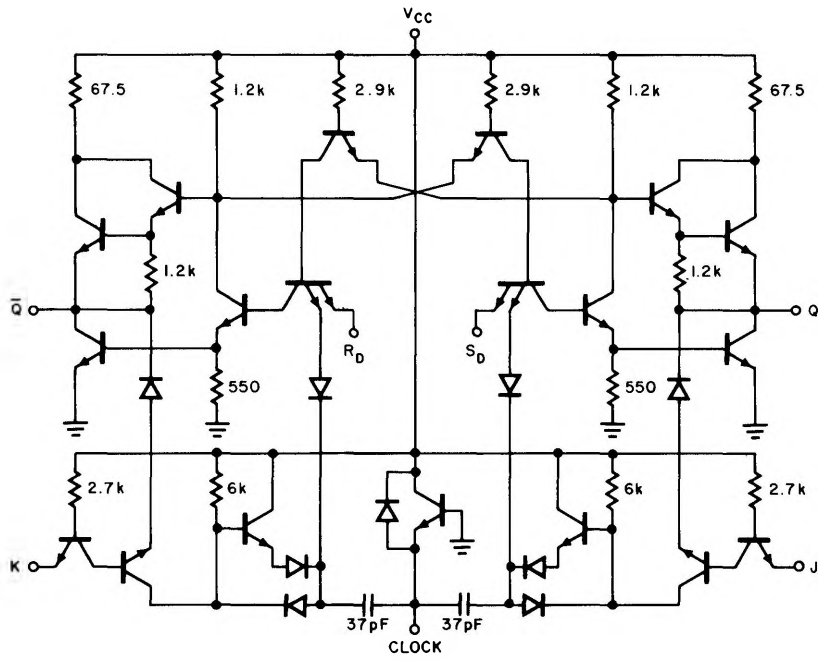
The 8827 is a Dual J-K Binary especially suited to high-speed parallel load counter and shift register applications. The clock and asynchronous reset inputs on the two binaries are common to allow separate Q, $\overline{Q}$, S_D (asynchronous set) and J and K. The S_D/R_D lines may be activated regardless of the state of the clock.

The clock input of the 8827 is capacitively coupled; clocking is effected on the negative-going transition of the clock pulse. All elements in the 8000 Series are characterized for AC fan-out to assure compatible operation under worst case conditions.

Table 1-5 of Section 1 summarizes AC loading guarantees for the 8827.

Section 4 provides detailed usage suggestions and applications.

BASIC CIRCUIT SCHEMATIC

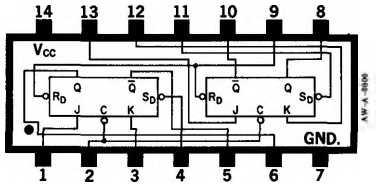


TRUTH TABLE

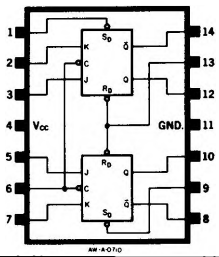
J_n	K_n	Q_{n+1}	$\overline{S}_D$	$\overline{R}_D$	Q
0	0	Q_n	1	1	Q
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	0	0	†

n is time prior to clock
n+1 is time following clock
† = both outputs in "1" state

A PACKAGE



J PACKAGE



8827

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 14)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS									
		MIN.	TYP.	MAX.	UNITS	TEMP. S8827	TEMP. N8827	V_{CC}	RESET	SET	CLOCK	J	K	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	2.0V	0.8V				-250μA	8
A-3	Q_1, Q_2	2.8			V	+25°C	+25°C	5.00V	2.0V	0.8V				-250μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V	0.7V				-250μA	8
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V	2.0V				-250μA	8
A-3	$\bar{Q}_1$, $\bar{Q}_2$	2.8			V	+25°C	+25°C	5.00V	0.8V	2.0V				-250μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.7V	2.0V				-250μA	8
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	0.8V	2.0V				8.0mA	9
A-3	Q_1, Q_2			0.4	V	+25°C	+25°C	5.00V	0.8V	2.0V				8.0mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	0.7V	2.0V				8.0mA	9
A-5	"0" OUTPUT VOLTAGE			0.4	V	-55°C	0°C	4.75V	2.0V	0.8V				8.0mA	9
A-3	$\bar{Q}_1$, $\bar{Q}_2$			0.4	V	+25°C	+25°C	5.00V	2.0V	0.8V				8.0mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	0.7V				8.0mA	9
C-1	"0" INPUT CURRENT	-0.1		-2.4	mA	-55°C	0°C	5.25V				0.4V	0.4V		
A-3	J_1, K_1, J_2, K_2	-0.1		-2.4	mA	+25°C	+25°C	5.25V				0.4V	0.4V		
C-1		-0.1		-2.4	mA	+125°C	+75°C	5.25V				0.4V	0.4V		
C-1	"0" INPUT CURRENT	-0.1		-4.0	mA	-55°C	0°C	5.25V	0.4V						
A-3	RESET	-0.1		-4.0	mA	+25°C	+25°C	5.25V	0.4V						
C-1		-0.1		-4.0	mA	+125°C	+75°C	5.25V	0.4V						
C-1	"0" INPUT CURRENT	-0.1		-2.0	mA	-55°C	0°C	5.25V		0.4V					
A-3	SET_1, SET_2	-0.1		-2.0	mA	+25°C	+25°C	5.25V		0.4V					
C-1		-0.1		-2.0	mA	+125°C	+75°C	5.25V		0.4V					
C-1	"0" INPUT CURRENT	-0.1		-20	μA	-55°C	0°C	5.25V			0.4V				
A-3	CLOCK	-0.1		-20	μA	+25°C	+25°C	5.25V			0.4V				
C-1		-0.1		-20	μA	+125°C	+75°C	5.25V			0.4V				
A-4	"1" INPUT CURRENT J_1, J_2, K_1, K_2, SET_1, SET_2			25	μA	+125°C	+75°C	5.00V		4.5V		4.5V	4.5V		12
A-4	"1" INPUT CURRENT RESET			50	μA	+125°C	+75°C	5.00V	4.5V						
A-4	"1" INPUT CURRENT CLOCK			50	μA	+125°C	+75°C	5.00V			4.5V				
A-2	POWER CONSUMPTION (Per Binary)			64	mW	+25°C	+25°C								
A-2	OUTPUT SHORT CIRCUIT CURRENT $\bar{Q}_1$, $\bar{Q}_2$	-20		-70	mA	+25°C	+25°C	5.00V	0V					0V	
A-2	OUTPUT SHORT CIRCUIT CURRENT Q_1, Q_2	-20		-70	mA	+25°C	+25°C	5.00V		0V				0V	
C-1	INPUT LATCH VOLTAGE														
	J_1, J_2, K_1, K_2, RESET, SET_1, SET_2,	5.5			V	+25°C	+25°C	5.00V	10mA	10mA		10mA	10mA		12, 13
	CLOCK	5.0		6.0	V	+25°C	+25°C	5.00V			10μA				
A-6	TURN-ON DELAY			35	ns	+25°C	+25°C	5.00V						D.C.F.O=10	10, 15
A-6	TURN-OFF DELAY			20	ns	+25°C	+25°C	5.00V						D.C.F.O=10	10, 15
A-6	TOGGLE RATE	25			MHz	+25°C	+25°C	5.00V							15
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V						A.C.F.O=2	11, 15
C-2	INPUT CAPACITANCE J_1, J_2, K_1, K_2, SET_1, SET_2			3.0	pf	+25°C	+25°C	5.00V		2.0V		2.0V	2.0V		7
C-2	INPUT CAPACITANCE RESET			6.0	pf	+25°C	+25°C	5.00V	2.0V						7
C-2	INPUT CAPACITANCE CLOCK			100	pf	+25°C	+25°C								7
A-6	CLOCK MODE HOLDING TEST			10	ns	+25°C	+25°C	5.00V			PULSE				15
A-6	CLOCK MODE SWITCHING TEST			50	ns	+25°C	+25°C	5.00V			PULSE				15

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. F = 1 MHz, V_{ac} = 25 mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8 mA.
11. One AC fan-out is defined as 50 pf.
12. To test "1" INPUT CURRENT and LATCH VOLTAGE RATING for J and RESET, ensure Q = "0". To test "1" INPUT CURRENT and LATCH VOLTAGE RATING for K and SET, ensure $\bar{Q}$ = "0".
13. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.