SIGNETICS DCL INTEGRATED CIRCUITS

8417 DUAL 3-INPUT EXPANDABLE NAND GATE

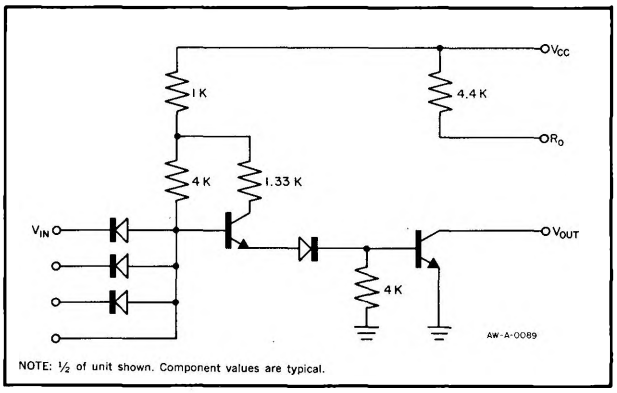
The 8417 Dual 3-Input Expandable NAND Gate implements the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

The optional pull-up resistor allows collector logic, or wired-AND, to be easily implemented. By paralleling optional pull-up resistors of two or more gates or by selecting discrete external pull-up resistors, more than 30 collectors may be tied together. The optional resistor is brought out at the pin adjacent to the output pin to simplify board layout when it is used.

An expansion node is provided for system flexibility. The compatibly characterized 8731 Diode Expander is recommended for this purpose.

Section 4 of this handbook provides helpful usage rules, including collector logic techniques, and applications for the 8417.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

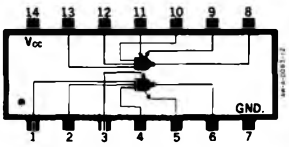
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8417	TEMP. N8417	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT LEAKAGE CURRENT			40	μA	+125°C	+75°C	5.0V	0.7V			11,12
	OUTPUT LOAD RESISTOR	3.5	4.4	5.3	KΩ	+25°C	+25°C	5.0V				11
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	8
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	8
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	8
C-1	"0" INPUT CURRENT	-0.1		-1.2	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-1.2	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-1.2	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-3	EXPANDER NODE	-0.1			mA	+25°C	+25°C	5.0V	0V			
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	50		150	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	9,14
C-2	FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 2	10,14
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	9,14
C-2	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.0V			D.C.F.O. = 1	9,14
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			22.6	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			7.3	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-0.94		-1.45	mA	+25°C	+25°C	5.0V	0V		0V	

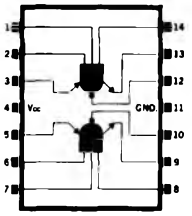
Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output sink current is supplied through a resistor to V_{cc}.
9. One DC fan-out is defined as 0.8mA.
10. One AC fan-out is defined as 50pf.
11. Optional pull-up resistor not connected to output.
12. Connect an external 1K ±1% resistor from V_{cc} to the output terminal for this test.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.

A PACKAGE



J PACKAGE



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