SIGNETICS DCL INTEGRATED CIRCUITS

8416 DUAL 4-INPUT EXPANDABLE NAND GATE

The 8416 Dual 4-Input Expandable NAND Gate implements the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

The DTL input structure provides an expansion node for logic flexibility. The compatibly characterized 8731 diode expander is recommended for this purpose.

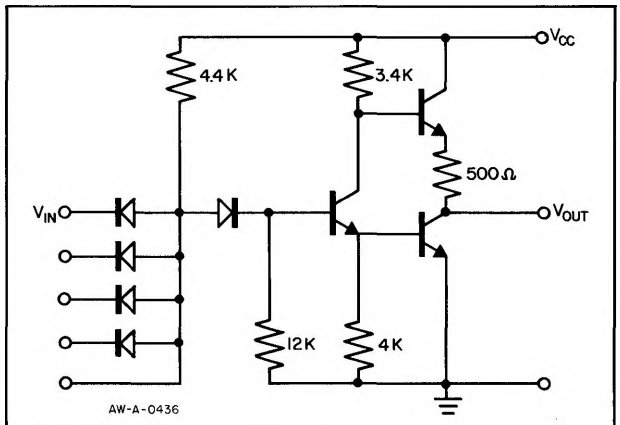
The active output structure of the 8416 provides high AC noise immunity due to it's low output impedance in both the "1" and "0" output states.

Output short circuit protection is provided by a current limiting resistor.

The values chosen for the collector and emitter resistors of the phase-splitter transistor, ensure optimum on-off relationships of the totem-pole output pair.

Section 4 of this handbook provides helpful usage rules and applications for the 8416.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

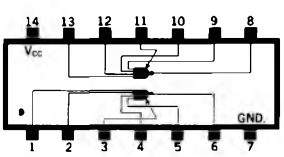
ELECTRICAL CHARACTERISTICS (NOTES: 1,2,3,4,5,6,12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8416	TEMP. N8416	V_{cc}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	3.4			V	-55°C	0°C	4.75V	0.7V		-225μA	8
A-3		3.6			V	+25°C	+25°C	5.0V	0.7V		-225μA	8
A-4		3.4			V	+125°C	+75°C	4.75V	0.7V		-225μA	8
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	9
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	9
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	9
C-1	"0" INPUT CURRENT	-0.1		-1.2	mA	-55°C	0°C	5.25V	0.35V	5.25V		
A-3		-0.1		-1.2	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-1.2	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-3	EXPANDER NODE	-0.1			mA	+25°C	+25°C	5.0V	0V			
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	30		95	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10,13
C-2	FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 2	11,13
C-2	TURN-ON DELAY			60	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10,13
C-2	TURN-OFF DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 1	10,13
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			25.2	mW	+25°C	+25°C	5.25V				
A-2	(Per Gate) OUTPUT "1"			7.3	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-4.0		-12.0	mA	+25°C	+25°C	5.0V	0V		0V	

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. Manufacturer reserves the right to make design and process changes and improvements.
13. Detailed test conditions for AC testing are in Section 3.

A PACKAGE



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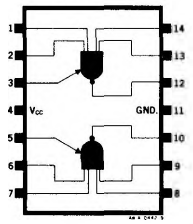

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