Silicon Gate MOS 8308

8192 BIT STATIC MOS READ ONLY MEMORY
Organization -- 1024 Words x 8 Bits

- **Fast Access – 450 ns**
- **Directly Compatible with 8080 CPU at Maximum Processor Speed**
- **Two Chip Select Inputs for Easy Memory Expansion**
- **Directly TTL Compatible – All Inputs and Outputs**
- **Three State Output – OR-Tie Capability**
- **Fully Decoded**
- **Standard Power Supplies +12V DC, ±5V DC**

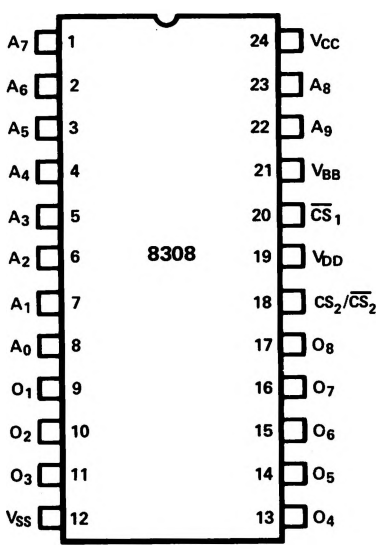
The Intel® 8308 is an 8,192 bit static MOS mask programmable Read Only Memory organized as 1024 words by 8-bits. This ROM is designed for 8080 microcomputer system applications where high performance, large bit storage, and simple interfacing are important design objectives. The inputs and outputs are fully TTL compatible.

A pin for pin compatible electrically programmed erasable ROM, the Intel® 8708, is available for system development and small quantity production use.

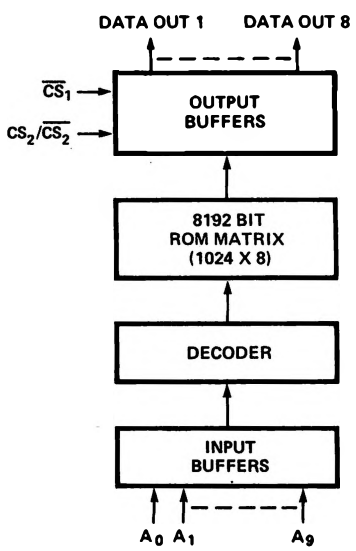
Two Chip Selects are provided – $\overline{CS}_1$ which is negative true, and $CS_2/\overline{CS}_2$ which may be programmed either negative or positive true at the mask level.

The 8308 read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0- A_9	ADDRESS INPUTS
O_1- O_8	DATA OUTPUTS
$\overline{CS}_1$, CS_2	CHIP SELECT INPUTS

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To V_{BB} . . . . . -0.3V to 20V
Power Dissipation . . . . . 1.0 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

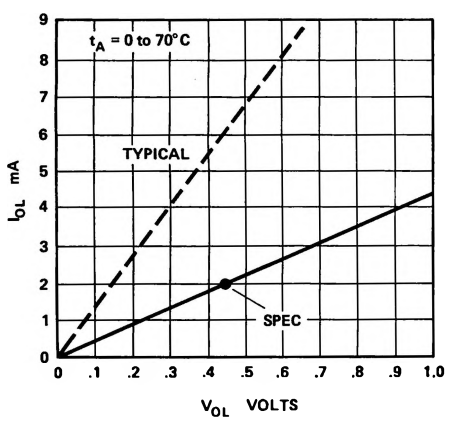
D.C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%; V_{DD} = 12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V Unless Otherwise Specified.

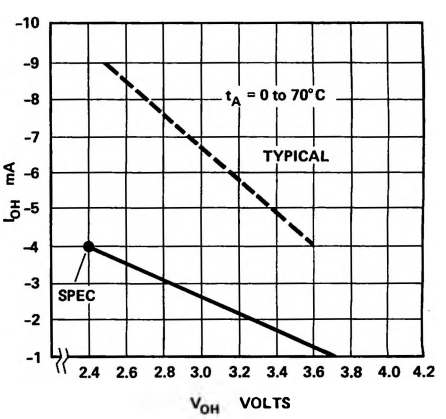
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins Except $\overline{CS_1}$)			10	μA	V_{IN} = 0 to 5.25V
I_{LCL}	Input Load Current on $\overline{CS_1}$			1.6	mA	V_{IN} = 0.45V
I_{LPC}	Input Peak Load Current on $\overline{CS_1}$			4	mA	V_{IN} = 0.8V to 3.3V
I_{LKC}	Input Leakage Current on $\overline{CS_1}$			10	μA	V_{IN} = 3.3V to 5.25V
I_{LO}	Output Leakage Current			10	μA	Chip Deselected
V_{IL}	Input "Low" Voltage	V_{SS}-1		0.8V	V	
V_{IH}	Input "High" Voltage	3.3		V_{CC}+1.0	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2mA
V_{OH1}	Output "High" Voltage	2.4			V	I_{OH} = -4mA
V_{OH2}	Output "High" Voltage	3.7			V	I_{OH} = -1mA
I_{CC}	Power Supply Current V_{CC}		.8	2	mA	
I_{DD}	Power Supply Current V_{DD}		32	60	mA	
I_{BB}	Power Supply Current V_{BB}		10μA	1	mA	
P_D	Power Dissipation			775	mW	

NOTE 1: Typical values for T_A = 25°C and nominal supply voltage

D.C. OUTPUT CHARACTERISTICS



D.C. OUTPUT CHARACTERISTICS



A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%; V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Specified.

Symbol	Parameter	Limits[2]			Unit
		Min.	Typ.	Max.	
t_{ACC}	Address to Output Delay Time		200	450	ns
t_{CO1}	Chip Select 1 to Output Delay Time		85	160	ns
t_{CO2}	Chip Select 2 to Output Delay Time		125	220	ns
t_{DF}	Chip Deselect to Output Data Float Time		125	220	ns

NOTE 2: Refer to conditions of Test for A.C. Characteristics. Add 50 nanoseconds (worst case) to specified values at V_{OH} = 3.7V @ I_{OH} = -1mA, C_L = 100pF.

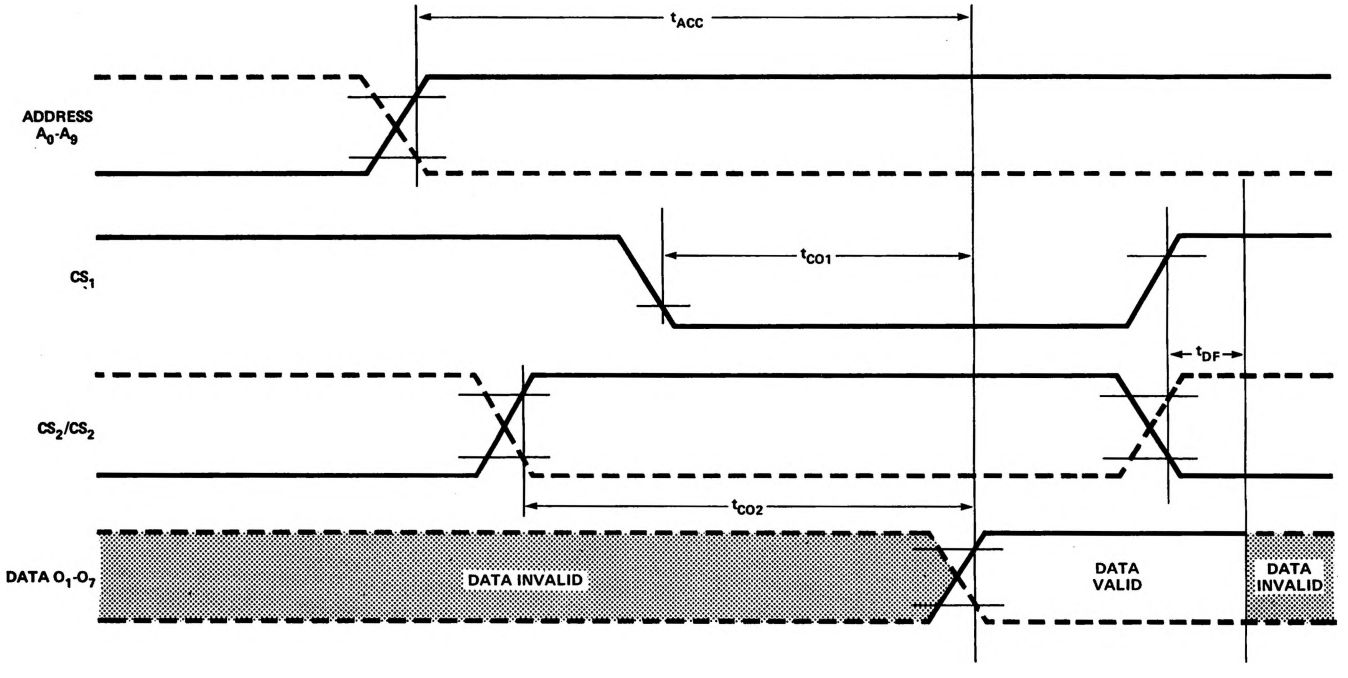
CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . . 1 TTL Gate, and C_{LOAD} = 100pF
Input Pulse Levels . . . . . .65V to 3.3V
Input Pulse Rise and Fall Times . . . . . 20 nsec
Timing Measurement Reference Level
. . . . . 2.4V V_{IH}, V_{OH}; 0.8V V_{IL}, V_{OL}

CAPACITANCE

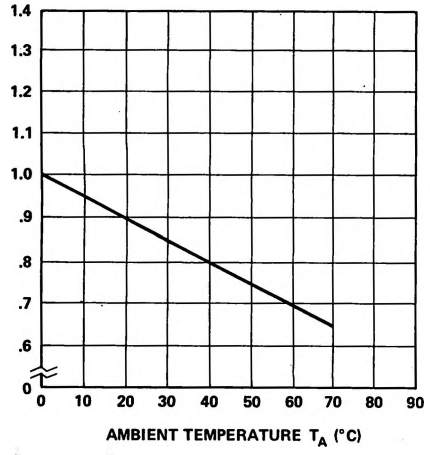
T_A = 25°C, f = 1 MHz, V_{BB} = -5V, V_{DD}, V_{CC} and all other pins tied to V_{SS}.

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	Input Capacitance		6pF
C_{OUT}	Output Capacitance		12pF

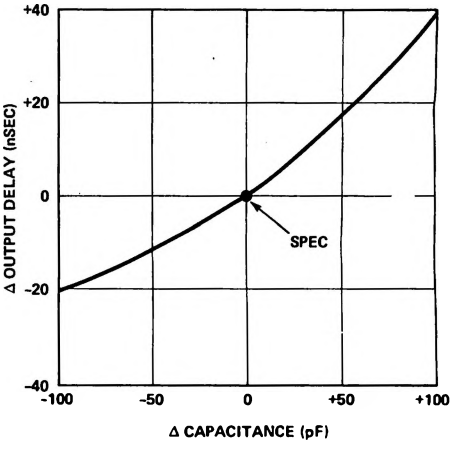


Typical Characteristics (Nominal supply voltages unless otherwise noted.)

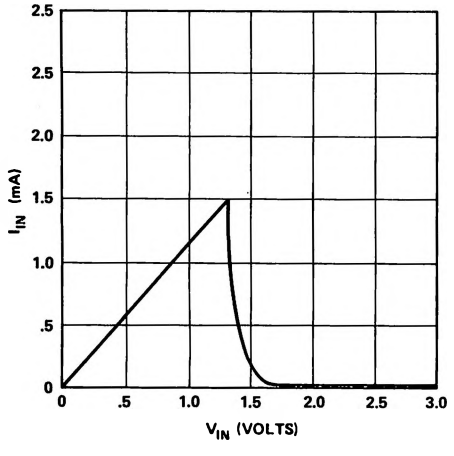
I_{DD} VS. TEMPERATURE (NORMALIZED)



Δ OUTPUT CAPACITANCE VS. Δ OUTPUT DELAY



$\overline{CS}_1$ INPUT CHARACTERISTICS



T_{ACC} VS. TEMPERATURE (NORMALIZED)