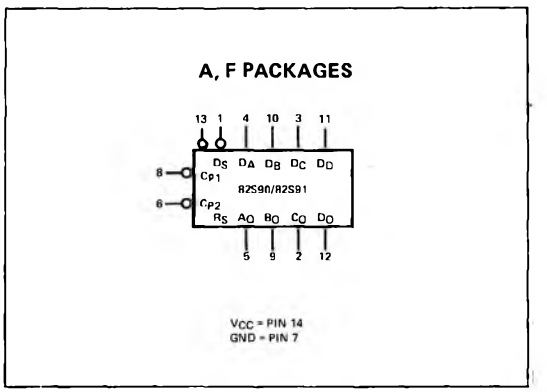
DESCRIPTION

The 82S90 Decade Counter and 82S91 Binary Counter are very high speed versions of the popular 8290 Decade and 8291 Binary Counters. They are multifunctional MSI building blocks capable of being used in counting frequency synthesis, digital integration where high speed is essential.

FEATURES

- **100 MHz TYPICAL COUNT FREQUENCY**
- **HIGH IMPEDANCE PNP INPUTS**
- **VARIABLE MODULUS, ÷2, 4, 5, 8, 10, and 16**
- **STROBED PARALLEL ENTRY**
- **PIN REPLACEABLE for the 8290/8291, 74196/74197**

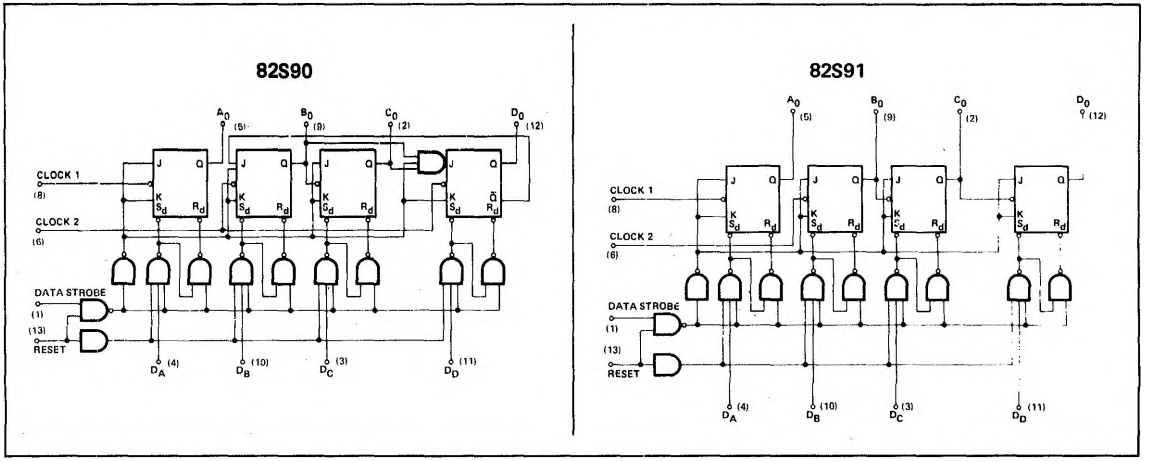
LOGIC SYMBOL



PIN DESIGNATIONS

CP_1	Clock input to counter first stage (active low going edge)
CP_2	Clock input to counter last three stages (active low going edge)
DS	Data Strobe Input for enabling data entry
RS	Reset Input for resetting all stages and outputs to zero
D_A, D_B, D_C, D_D	Data Inputs
A_O, B_O, C_O, D_O	Data Outputs

LOGIC DIAGRAMS



D.C. ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN	TYP	MAX	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	2.0V	2.0V			−1mA	6, 8
"0" Output Voltage			0.5	V	0.8V	0.8V	0.8V			20mA	6, 9
"0" Input Current											
Data Strobe			-0.4	mA			5.25V				
Data Inputs			-0.4	mA							
Reset			-0.4	mA	5.25V						
Clock 1			-6.0	mA	5.25V						
Clock 2 (8290)			-6.0	mA	5.25V						
Clock 2 (8291)			-3.0	mA	5.25V						
"1" Input Current											
Data Strobe			10	μA	4.5V		0.0V				
Data Inputs			10	μA		4.5V					
Reset			10	μA	0.0V		4.5V				
Clock 1			100	μA	0.0V			4.5V			
Clock 2 (8290)			100	μA	0.0V				4.5V		
Clock 2 (8291)			50	μA	0.0V				4.5V		
Output Short Circuit Current	-40		-100	mA	0.0V	4.5V				0.0V	11,12
Input Voltage Rating											
Data Strobe	5.5			V	10mA						
Clock 1 & 2	5.5			V				10mA	10mA		
Data Inputs	5.5			V		10mA					
Reset	5.5			V			10mA				
Power Consumption/		308	461	mW/			0.0V	0.0V	0.0V		12
Supply Current		62	88	mA							

A.C. ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_{CC} = 5.0V

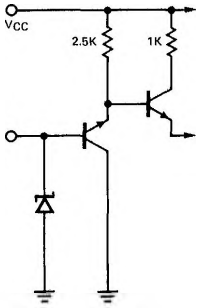
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN	TYP	MAX	UNITS	DATA STROBE	DATA INPUTS	RESET	CLOCK 1	CLOCK 2	OUTPUTS	
Strobe Pulse Width		5		ns					A_{OUT}		9
Reset Pulse Width		7		ns					A_{OUT}		9
Strobe/Reset Release Time		10		ns					A_{OUT}		9
Clock Mode t_{on} Delay											
Bit A		9	12	ns							9
Bits B, C, D		10	13	ns							9
Clock Mode t_{off} Delay											
Bit A		5	8	ns							9
Bits B, C, D		6	10	ns							9
Strobed Data t_{on} Delay											
(All Bits)		15	22	ns							9
Strobed Data t_{off} Delay											
(All Bits)		13	20	ns							9
Toggle Rate	85	100		MHz							9

NOTES:

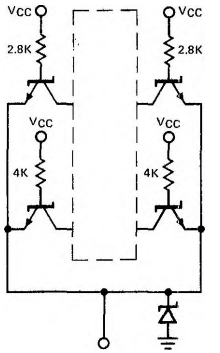
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figures.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. Not more than one output should be shorted at a time.
12. V_{CC} = 5.25V.

INPUT AND OUTPUT STRUCTURES

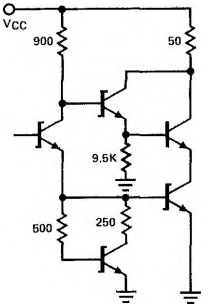
DATA, STROBE and RESET INPUTS



CLOCK INPUTS

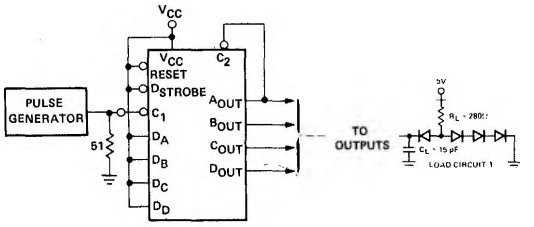


OUTPUTS

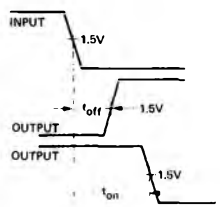


AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY

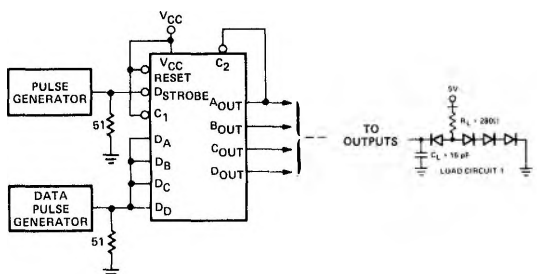


Note:
t_{on} and t_{off} are measured from the clock input of each binary to the Q

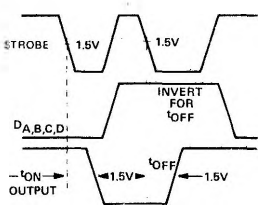


INPUT PULSE:
Amplitude = 2.6V
PW = 30ns, 50% to 50%
$t_r = t_f = 5ns$

STROBED DATA t_{on}/t_{off} DELAY



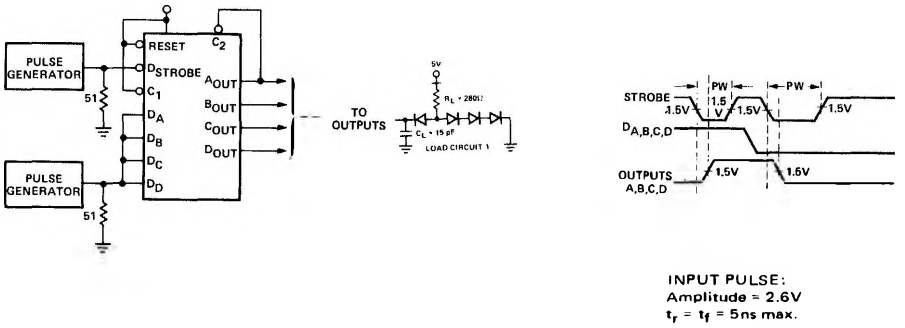
Strobe,
P.A. = 2.6V
P.W. = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f = 5ns$



Data,
P.A. = 2.6V
P.W. = 500ns, 50% to 50%
PRR = 500KHz
$t_r = t_f = 5ns$

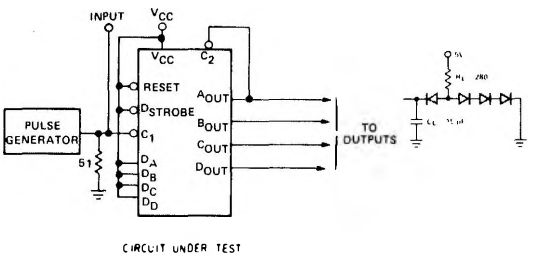
AC TEST FIGURES AND WAVEFORMS (Cont'd)

MINIMUM STROBE PULSE WIDTH



INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.

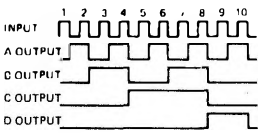
TOGGLE RATE



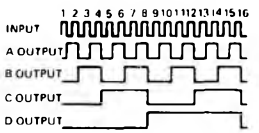
CIRCUIT UNDER TEST

INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz, 50% duty cycle
$t_r = t_f$ = 5ns max.

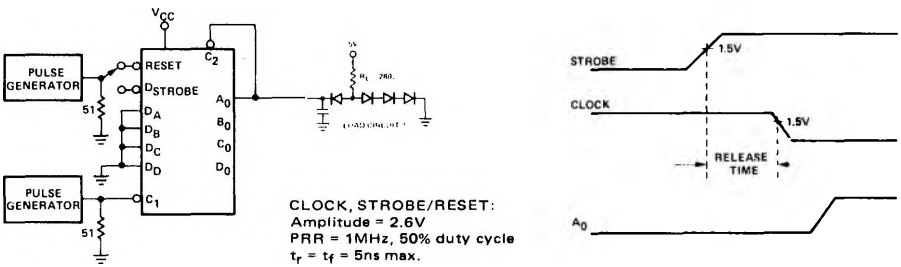
82S90



82S91



STROBE/RESET RELEASE TIME



CLOCK, STROBE/RESET:
Amplitude = 2.6V
PRR = 1MHz, 50% duty cycle
$t_r = t_f$ = 5ns max.

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.
3. All diodes are 1N916.

FUNCTIONAL DESCRIPTION

1. 82S90 Decade Counter

The 82S90 can be used in three basic count modes as follows:

a. BCD Counter. The CP2 input must be connected to the A_O output and CP1 receives the count input. The count sequence obtained is BCD in accordance with the truth table.

b. Bi-Quinary Counter. If a symmetrical output is required for divide by 10 operation, the D_O output must be connected to the CP1 input and the count input applied to CP2. A symmetrical square wave is then obtained at A_O of one-tenth the input frequency present at CP2 in accordance with the truth table.

c. Separate Divide by Two and Five Counters. Because the inherent structure of the counter is that of two separate divide by two and divide by five sections, no other connections are required for this mode of operation. An input presented to CP1 will appear at A_O output at half the input frequency. An input presented to CP2 will appear at outputs B_O, C_O and D_O as a binary divide by five count (i.e., from 0 = 000 to 4 = 100). Operation of the D_S and R_S inputs remain common to all four flip flops as with any other count mode.

TRUTH TABLES

Decade (BCD)				
Input	A_O	B_O	C_O	D_O
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

Bi-Quinary (5-2)				
Input	A_O	B_O	C_O	D_O
0	0	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	1	1	0
4	0	0	0	1
5	1	0	0	0
6	1	1	0	0
7	1	0	1	0
8	1	1	1	0
9	1	0	0	1

2. 82S91 Binary Counter

The 82S90 can be used in two basic count modes as follows:

a. Binary Counter—For this mode of operation A_O output must be connected to CP2 input and the count input connected to CP1. Subdivisions of the count input frequency then appear at A_O = ÷2, B_O = ÷4, C_O = ÷8, D_O = ÷16 as shown in the truth table.

b. Separate Divide by Two and Divide by Eight Counters—In similar manner to the 82S90 the 82S91 inherent structure allows separate use of the first and last three stages. In the first stage the input count frequency presented to CP2 appears at outputs B_O = ÷2, C_O = ÷4 and D_O = ÷8 simultaneously. Operation of the D_S and R_S inputs remains common to all stages.

TRUTH TABLE

Binary				
Input	A_O	B_O	C_O	D_O
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

3. Operation of the D_S Data Strobe and R_S Reset Inputs:

a. Data Strobe D_S Input—When D_S = 0 the four stages of the 82S90/91 can be used as four separate latches with the outputs A_O - D_O following the data presented to the inputs D_A - D_D regardless of clock inputs.

With D_S = 1 the four stages remain unchanged until the next clock inputs, which activate counting in accordance with the various modes described previously. The Reset R_S inputs when low overrides D_S as described below.

b. Reset R_S Input—With R_S = 0 the clock inputs CP1/CP2 and D_S input are overridden, all stages of the 82S90/91 are cleared and zeros appear at the counter outputs A_O - D_O. When R_S = 1, operation is controlled by D_S or CP1/CP2 clock inputs as described.