signetics

BINARY-TO-OCTAL DECODER
BCD-TO-DECIMAL DECODER

82S50
82S52

A,F PACKAGES 82S50
B,F PACKAGES 82S52

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S50 and 82S52 are gate arrays for decoding and logic conversion applications.

The 82S50 converts 3 lines of input to a one-of-eight output. The fourth input line (D) is utilized as an inhibit to allow use in larger decoding networks.

The 82S52 converts a 4 line input code (with 1-2-4-8 weighting) to a one-of-ten output as shown in the Truth Table.

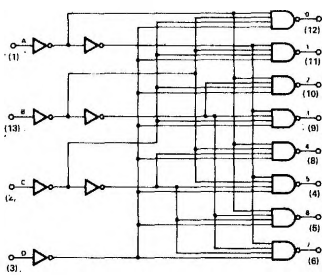
The 82S52 is a direct replacement for the 9301 with all outputs being forced high when a binary code greater than nine is applied to the inputs. The selected output is a logic "0".

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- INHIBIT INPUT FORCES ALL OUTPUTS HIGH (82S50)
- 82S52 REPLACES 9301 FOR HIGHER SPEED

LOGIC DIAGRAMS

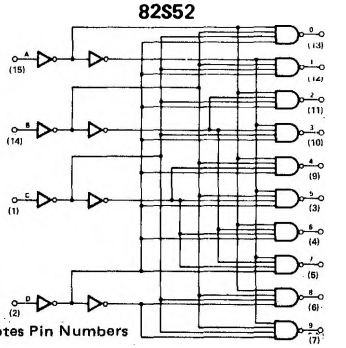
82S50



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

*NOTE: PIN-OUT FOR DUAL IN-LINE PACKAGE ONLY

82S52



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

TRUTH TABLE

INPUT STATE				OUTPUT STATES									
				82S50								82S52	
A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS						
"1" Output Voltage	2.7			V					−1mA	6, 10
"0" Output Voltage			0.5	V					20mA	7,10
"1" Input Current			10	μA	4.5V	4.5V	4.5V	4.5V		
"0" Input Current (ALL)			−400μA	mA	0.5V	0.5V	0.5V	0.5V		

$T_A = 25^oC$ and $V_{CC} = 5.0V$

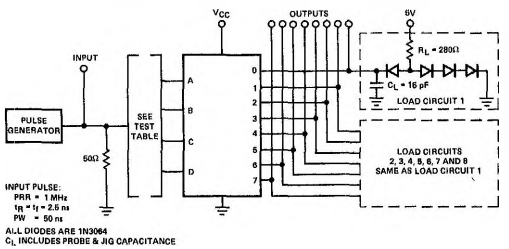
CHARACTERISTICS	LIMITS				A	B	C	D	OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS						
Turn-on Delay t_{on}			16	ns						8
Turn-off Delay t_{off}			16	ns						8
Power/Current Consumption										
(82S50 Only)			380/72	mW/mA	5.25V	5.25V	5.25V	0V		11
(82S52 Only)			450/85	mW/mA						11
Input Clamp Voltage			−1.2	V	−18mA	−18mA	−18mA	−18mA		
Output Short Circuit Current (ALL)	−40		−100	mA	4.0V	4.0V	4.0V	4.0V	0V	9,11

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1". "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Not more than one output should be shorted at a time.
10. Inputs for "1" and "0" output voltage test is per TRUTH table with threshold levels of 0.8V for logical "0" and 2.0V for logical "1".
11. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS

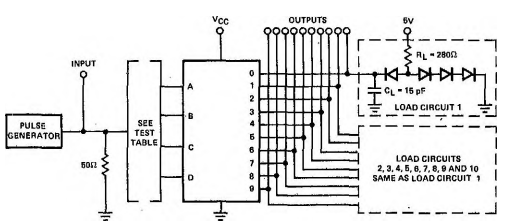
82S50



TEST TABLE													
TEST NO.	INPUTS A	B	C	D	OUTPUTS 0	1	2	3	4	5	6	7
1	1	1	PG	0								T
2	1	1	PG	0				T				T
3	PG	1	0	0			T	T				
4	0	PG	1	0					T		T	
5	0	0	0	PG	T							
6	1	0	PG	0		T				T		

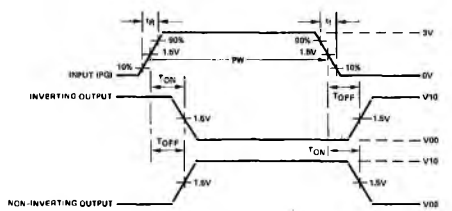
"1" = 2.7V "0" = GROUND

82S52



TEST TABLE														
TEST NO.	INPUTS A	B	C	D	OUTPUTS 0	1	2	3	4	5	6	7	8	9
1	0	0	PG	0				T						
2	PG	1	0	0		T	T							
3	0	0	0	PG	T							T		
4	1	0	PG	0		T			T					
5	1	PG	0	1										T
6	PG	1	1	0										

"1" = 2.7V "0" = GROUND



NOTE:

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.