signetics

2-INPUT 4-BIT DIGITAL MULTIPLEXER

82S33
82S34

B,F PACKAGES

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

These devices are 2-input, 4-Bit Digital Multiplexers designed for general purpose data-selection applications.

The 82S33 features non-inverting data paths; and, the 82S34 features inverting data paths.

The 82S34 has open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as forty four-bit words can be multiplexed by using twenty 82S34's in the WIRED-AND mode.

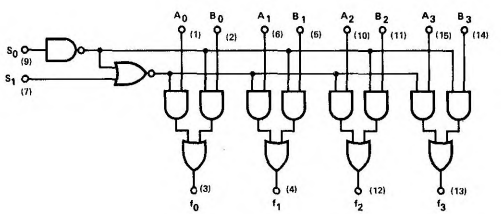
The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUTS (82S34)
- INHIBIT STATE

LOGIC DIAGRAM

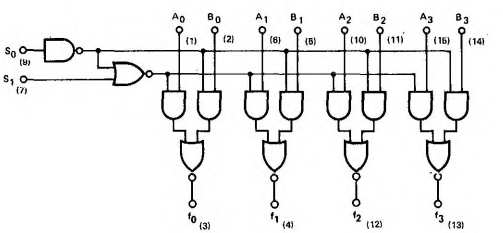
82S33



S_0	S_1	f_n
0	0	B
1	0	A
0	1	B
1	1	0

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

82S34 (OPEN COLLECTOR)



S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

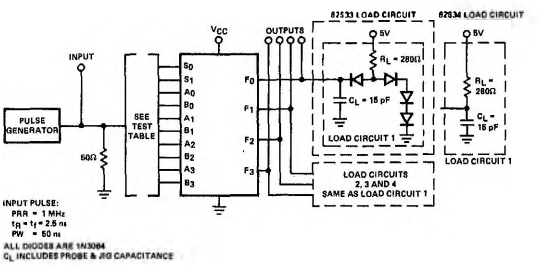
CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUTS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1		
"1" Output Voltage (82S33)	2.7			V	2.0V	2.0V	0.8V	0.8V	−1mA	6
"0" Output Voltage (82S33)			0.5	V	0.8V	2.0V	2.0V	0.8V	20mA	7
"0" Output Voltage (82S34)			0.5	V	0V	2.0V	0.8V	0.8V	20mA	7
"1" Output Leakage Current (82S34)			250	μA	2.0V	2.0V	2.0V	2.0V	5.5V	9
"0" Input Current (ALL)			400	μA	0.5V	0.5V	0.5V	0.5V		
"1" Input Current (ALL)			−10	μA	4.5V	4.5V	4.5V	4.5V		
Output Short Circuit Current (82S33)	−40		−100	mA	5V	5V	0V	0V	0V	10, 11
Input Clamp Voltage (ALL)			−1.2V	V	−18mA	−18mA	−18mA	−18mA		

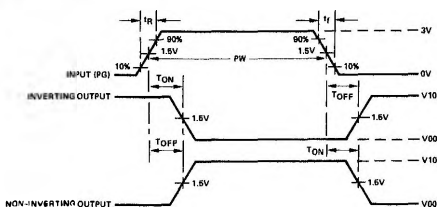
$T_A = 25^oC$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS INPUTS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A_n	B_n	S_0	S_1		
Power/Current Consumption:										
82S33			305/58	mW/mA		0V		0V		10
82S34			265/50	mW/mA		0V		0V		10
82S33/34 Turn-On/Turn-Off Times										
A_n, B_n to f_n			12	ns						8,1
S_0 to f_n			20	ns						8,1
S_1 to f_n			18	ns						8,1

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures and Test Table.
9. Connect an external 1K ± 1% resistor to V_{CC} for this test.
10. V_{CC} = 5.25V.
11. Not more than one output should be shorted at a time.

AC TEST FIGURES AND WAVEFORMS





TEST TABLE

TEST NO.	INPUTS S_0	S_1	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	OUTPUTS F_0	F_1	F_2	F_3
1	PG	0	1	0	1	0	1	0	1	0	T			
2	PG	0	1	0	1	0	1	0	1	0	T	T	T	T
3	PG	0	0	1	0	1	0	1	0	1		T		
4	1	PG	1	0	1	0	1	0	1	0			T	
5	0	0	0	PG	0	0	0	0	0	0	T			
6	0	1	0	0	0	PG	0	0	0	0		T		
7	1	0	0	0	0	0	PG	0	0	0			T	
8	1	0	0	0	0	0	0	0	PG	0				T

"1" = 2.7V "0" = GROUND

NOTE:
1. A.C. TEST JIG'S MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIG'S MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.