82S230-F,N • 82S231-F,N

DESCRIPTION

The 82S230 and 82S231 include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S230 and 82S231 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S230/231, F or N, and for the military temperature range (-55°C to +125°C) specify S82S230/231, F.

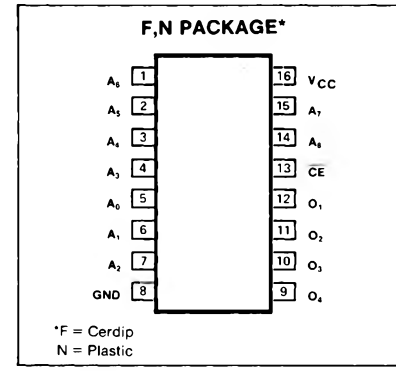
FEATURES

- **Address access time:**
  N82S230/231: 50ns max
  S82S230/231: 70ns max
- **Power dissipation: 0.3mW/bit typ**
- **Input loading:**
  N82S230/231: -100μA max
  S82S230/231: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S230: Open collector
  82S231: Tri-state
- **Fully compatible with Signetics 82S130/131 PROMs**
- **Fully TTL compatible**

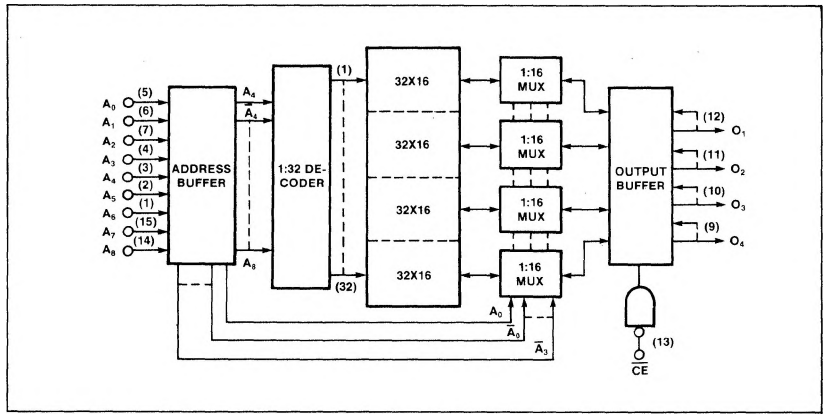
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S230)	+5.5	
V_O	Off-state (82S231)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S230/231	0 to +75	
	S82S230/231	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S230/231: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S230/231: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S230/231			S82S230/231			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S231)	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100		-150		
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S230)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S231)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit (82S231)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			120	140		120	140	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN}= 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

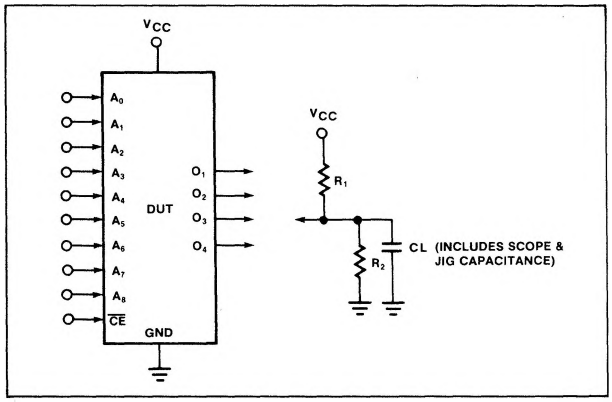
R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF[1]
N82S230/231: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S230/231: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S230/231			S82S230/231			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		40	50		40	70	
T_{CE}	Output	Chip enable		20	30		20	35	
Disable time									ns
T_{CD}	Output	Chip disable		20	30		20	35	

NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM