DESCRIPTION

The 82S21 is a TTL 64 bit Write-While-Read Random Access Memory organized in 32 words of 2 bits each. The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5 input decoder when the Read-Write enable input, CE is at logic "1". $\overline{W_0}$ and $\overline{W_1}$ are the write inputs for bit 0 and bit 1 of the word selected. $\overline{C}$ is the write control input. When $\overline{W_X}$ and $\overline{C}$ are both at logic "0" data on the I_0 and I_1 data lines are written into the addressed word. The read function is enabled when either $\overline{W_X}$ or $\overline{C}$ is at logic "1".

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$, is logic "1" and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When $\overline{L}$ goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When $\overline{L}$ goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

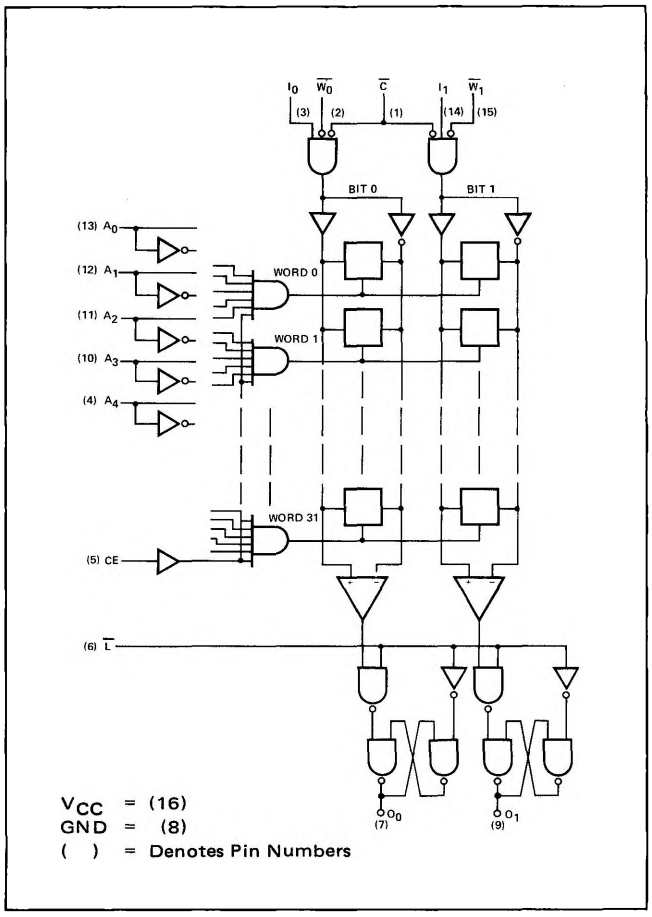
FEATURES

- BUFFERED ADDRESS LINES
- ON CHIP LATCHES
- ON CHIP DECODING
- BIT MASKING CONTROL LINES
- ENABLE CONTROL LINE
- OPEN COLLECTOR OUTPUTS WITH 40mA CAPABILITY
- PROTECTED INPUTS
- VERY HIGH SPEEDS (25ns TYP)

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
CONTROL STORE

LOGIC DIAGRAM



TRUTH TABLE

CE	$\overline{C}$	$\overline{W_0}$	$\overline{W_1}$	$\overline{L}$	Mode	Outputs
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	1	Read & Write Disabled	Disabled logic "1"
1	1	X	X	X	Read	Data stored in addressed word
1	0	1	1	X	Read	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when L went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	0	1	X	Write Data into Bit 0 Only	If $\overline{L}$ = 0: Data from last word address when L went from "1" to "0"
1	0	1	0	X	Write Data into Bit 1 Only	If $\overline{L}$ = 1: Data being written into the selected bit location and stored in other addressed location

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C; 4.75V \leq V_{CC} \leq 5.25V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			.45	V	V_{out} = 32mA	
"1" Output Leakage Current			40	μA	V_{out} = 5.5V	
"0" Input Current (All Inputs)			−1.6	mA	V_{in} = 0.45V	
"1" Input Current (All Inputs)			25	μA	V_{in} = 5.5V	
Input "0" Voltage (V_{IL})			0.85	V		
Input "1" Voltage (V_{IH})	2.0			V		
Power Consumption			130/683	mA/mW		
Input Clamp Voltage	−1.2			V	I_{in} = −18mA	

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C, 4.75 \leq V_{CC} \leq 5.25V$

CHARACTERISTICS		LIMITS				TEST CONDITIONS	NOTES
		MIN.	TYP.	MAX.	UNITS		
Read Access Time Address to Output	t_1		25	50	ns		
Address Set-Up Time	t_2		8	15	ns		
Data Set-Up Time	t_3		15	20	ns		
Address Hold Time	t_4			0	ns		
Control or Write Pulse Width	t_5		15	20	ns		
Write Access Time	t_6		20	25	ns		
Address to Latch Set-Up Time	t_7		25	50	ns		
Latch Address to Address Hold Time	t_8		7	10	ns		
Delatch Access Time	t_9		15	25	ns		
Data Hold Time	t_{10}		0	5	ns		

AC WAVEFORM

Read Access Time

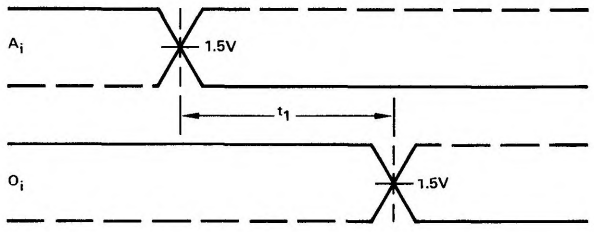
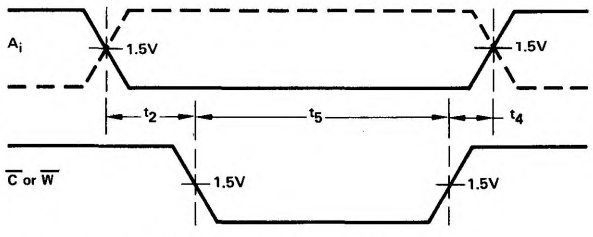


FIGURE 1

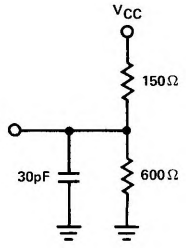
Address Setup and Hold Time



$t_r = t_f \leq 5$ ns, INPUT VOLTAGE = 2.8 Volts

FIGURE 2

TEST LOAD



AC WAVEFORMS

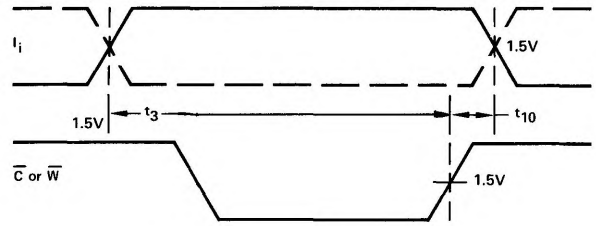


Fig. 3 Data Setup and Hold Time

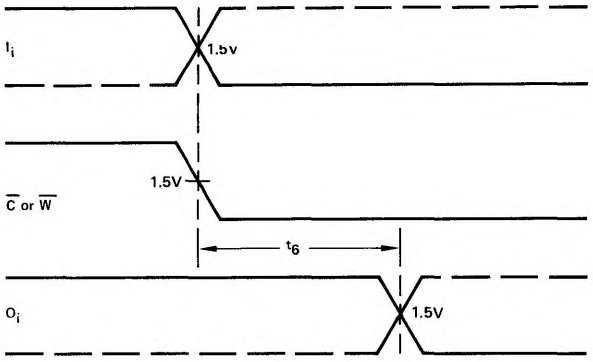


Fig. 4 Write Access Time

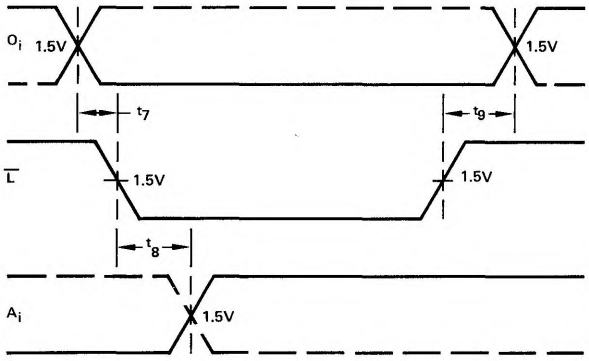
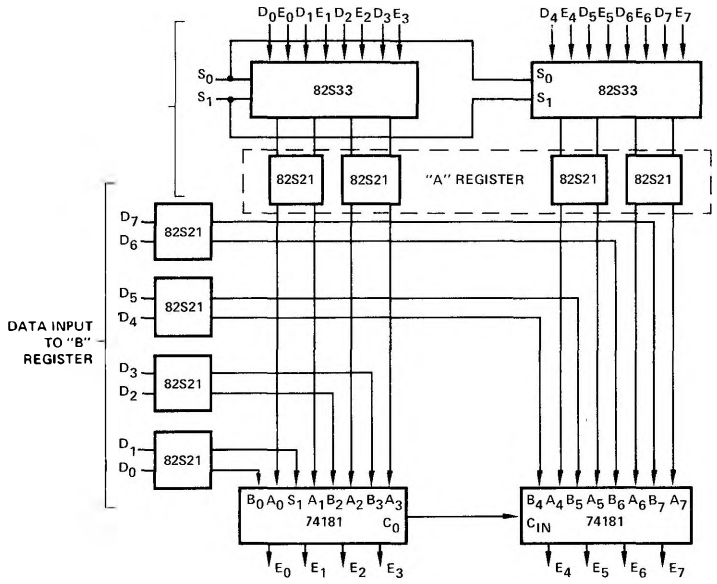


Fig. 5 Latch Times

TYPICAL APPLICATION



BASIC 8 BIT FULLY BUFFERED ACCUMULATOR

By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32 x 8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B → A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.