DESCRIPTION

The 82S208 and 82S210 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

The address inputs have a latch feature controlled by a latch control pin ($\overline{L}$). In the Transparent mode, the $\overline{L}$ pin is held high and the read or write location is accessed directly from the address inputs. In the Latched mode, a negative transition on the $\overline{L}$ line causes the present address state to be held in the address latches, independent of any other control signals. A positive pulse on the $\overline{L}$ line will cause a new address state to be strobed into the latches.

FEATURES

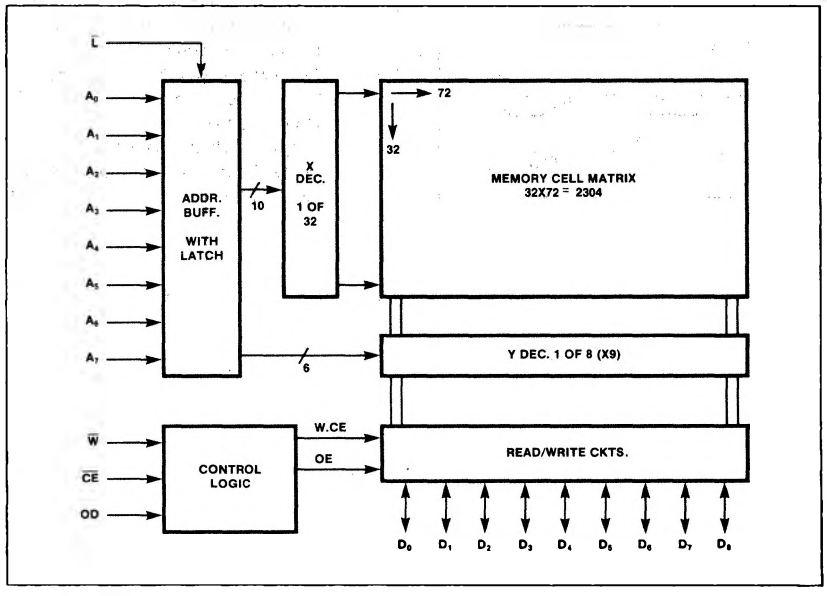
- **Access time:**
  Address: 60ns max
  Strobe: 70ns max
- **On-chip address latches**
- **Tri-state outputs**
- **Schottky clamped TTL**

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	OD	$\overline{L}$	D_N IN/OUT
Disable output	X	X	1	X	High Z
Disable R/W	X	1	X	X	High Z
Write	0	0	1	X	Data in
Read	1	0	0	X	Data out
Transparent address	X	X	X	1	—
Hold address	X	X	X	0	—

X = Don't care

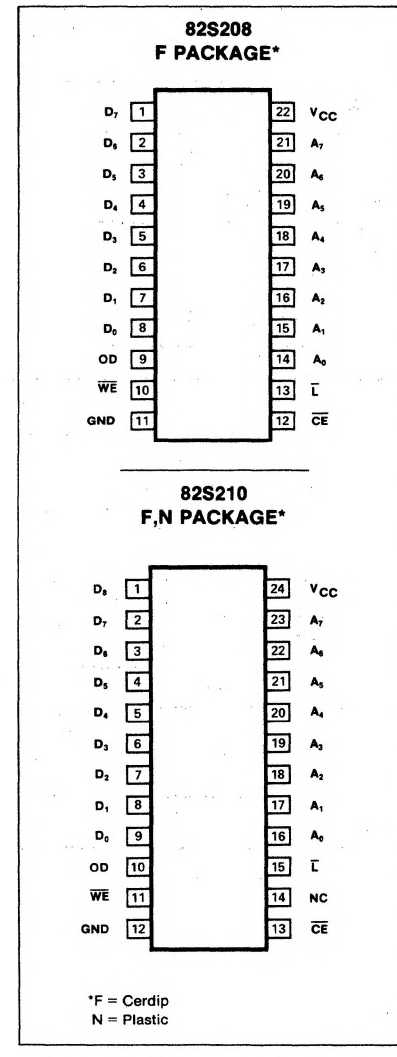
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

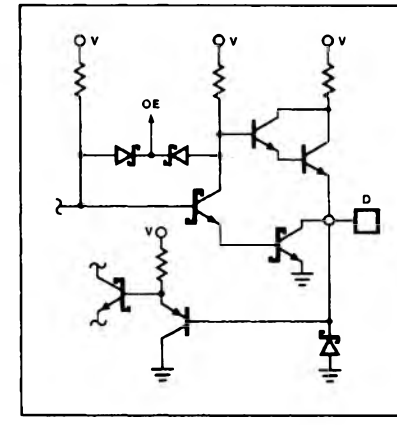
	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

PIN CONFIGURATION



*F = Cerdip
N = Plastic

TYPICAL I/O STRUCTURE



DC ELECTRICAL CHARACTERISTICS $0°C \le T_A +75°C$, $4.75V \le V_{CC}$ 5.25V[1]

PARAMETER		TEST CONDITIONS	LIMITS[2]			UNIT
			Min	Typ[3]	Max	
	Input voltage					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp[4]	I_{IN} = -18mA		-0.8	-1.2	
	Output voltage	CE = Low, OD = Low				V
V_{OL}	Low	I_{OUT} = 9.6mA			0.5	
V_{OH}	High	I_{OUT} = -2mA, High stored	2.4	3.3		
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			-100	
I_{IH}	High	V_{IN} + 5.5V			25	
	Output current					
$I_{O(OFF)}$	Hi-Z state	CE = Low, OD = High, V_{OUT} = 5.5V			40	μA
		CE = High, V_{OUT} = 0.5V			-100	
I_{OS}	Short circuit[4,5]	V_{OUT} = 0V	-20		-70	mA
I_{CC}	Supply current			135	185	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V, CE = High, OD = High		8		

AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Access time						ns
T_{AA}	Address	Output	Address			60	
T_{AL}	Strobe	Output	Latch			70	
	Enable time						ns
T_{OE}	Output	Output	OD			35	
T_{CE}	Output	Output	Chip enable			35	
	Disable time						ns
T_{OD}	Output	Output	OD			35	
T_{CD}	Output	Output	Chip enable				
	Pulse width						ns
T_{WL}	Strobe			20			
T_W	Write			40			
	Setup and hold time						ns
T_{SL}	Setup time	Latch	Address	5			
T_{HL}	Hold time	Address	Latch	10			
T_{SSA}	Setup time (strobe)	Latch	Address	0			
T_{SC}	Setup time	Write	Chip enable	5			
T_{HC}	Hold time	Chip enable	Write				
T_{SD}	Setup time	Write	Data	35			
T_{HD}	Hold time	Data	Write	10			
T_{SA}	Setup time	Write	Address	10			
T_{HA}	Hold time	Address	Write				
T_{SLW}	Setup time	Write	Latch	15			
T_{HLW}	Hold time	Latch	Write	10			
T_{S01}	Setup time (from disabled state)	Chip enable	OD	5			
T_{S02}	Setup time (from enabled state)	Data in	OD	35			
T_{HO}	Hold time	OD	Chip enable	5			

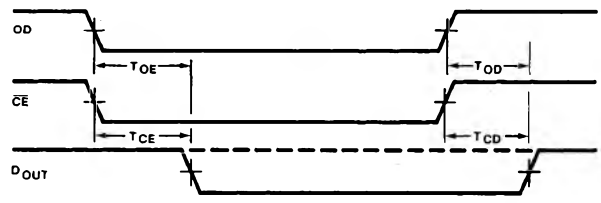
NOTES on following page.

NOTES

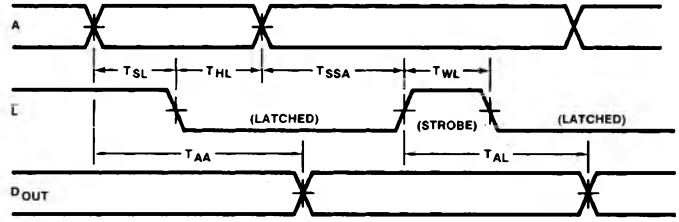
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at V_{CC} = 5V, T_A = 25°C.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.

TIMING DIAGRAMS

ENABLE/DISABLE



READ MODE



WRITE MODE