DESCRIPTION

The 82S130 and 82S131 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S130 and 82S131 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S130 and 82S131 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0° to +75°C) specify N82S130/131, F or N, and for the military temperature range (-55°C to +125°C) specify S82S130/131, F.

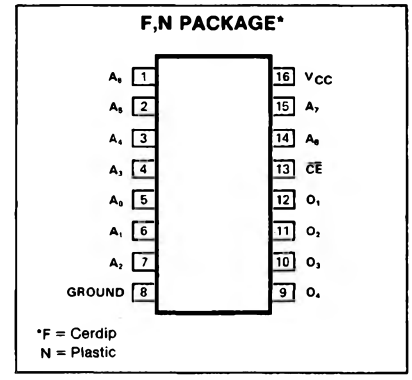
FEATURES

- **Address access time:**
  N82S130/131: 50ns max
  S82S130/131: 70ns max
- **Power dissipation: 0.3mW/bit typ**
- **Input loading:**
  N82S130/131: -100μA max
  S82S130/131: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S130: Open collector
  82S131: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

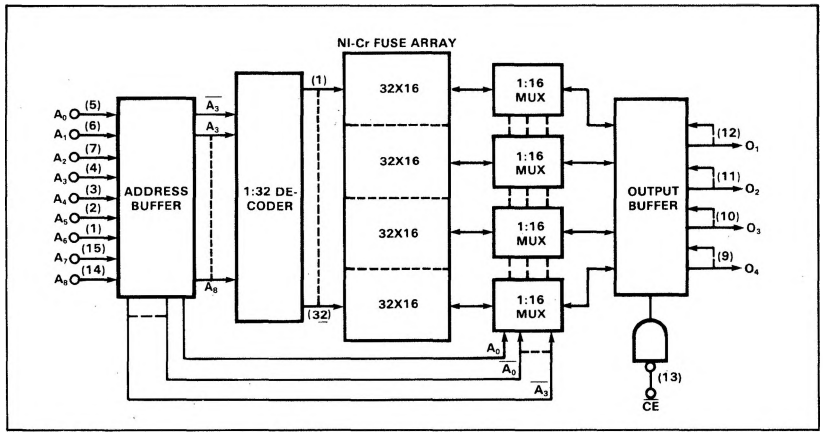
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S130)	+5.5	
V_O	Off-state (82S131)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S130/131	0 to +75	
	S82S130/131	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S130/131: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S130/131: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S130/131			S82S130/131			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S131)	$\overline{CE}$ = low, I_{OUT} = -2mA high stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		40				-150	
I_{IH}	High	V_{IN} = 5.5V		.85				50	
	Output current								
I_{OLK}	Leakage (82S130)	$\overline{CE}$ = high, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S131)	$\overline{CE}$ = high, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE}$ = high, V_{OUT} = 0.5V			-40			-60	
I_{OS}	Short circuit (82S131)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			120	140		120	140	mA
	Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V							pF
C_{IN}	Input			5			5		
C_{OUT}	Output			8			8		

AC ELECTRICAL CHARACTERISTICS

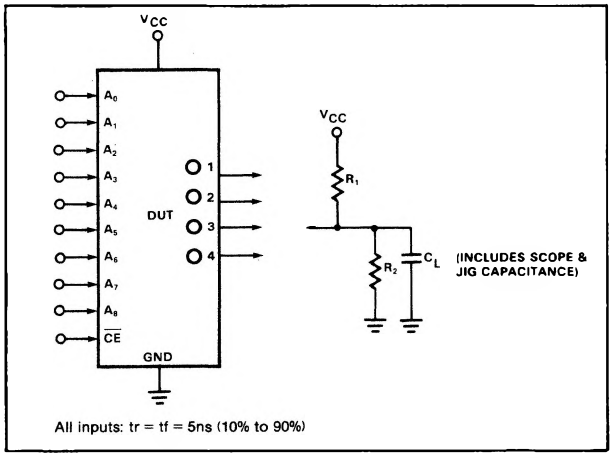
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$[2]
N82S130/131: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S130/131: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S130/131			S82S130/131			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
Access time									ns
T_{AA}	Output	Address		40	50		40	70	
T_{CE}	Output	Chip enable		20	30		20	40	
Disable time									ns
T_{CD}	Output	Chip disable		20	30		20	40	

NOTES

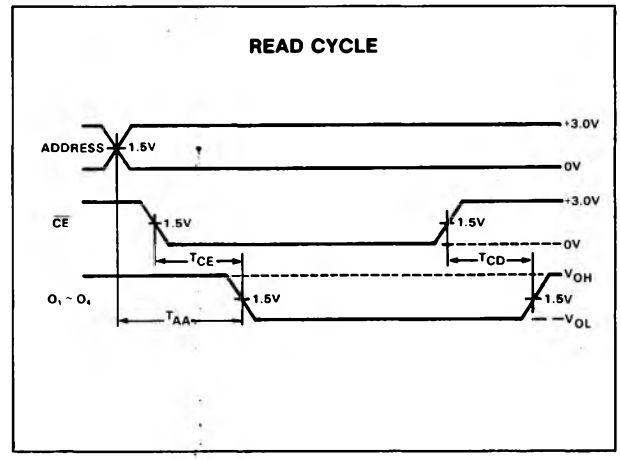
1. Typical values are at V_{CC} = 5.0V, T_A = +25°C.
2. Positive current is defined as into the terminal referenced.

TEST LOAD CIRCUIT



All inputs: tr = tf = 5ns (10% to 90%)

VOLTAGE WAVEFORM



PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 375 ± 75mA, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	300		450	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	V_{CCP} = V_{CCP}			12	sec
T_{PSI}	Initial programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

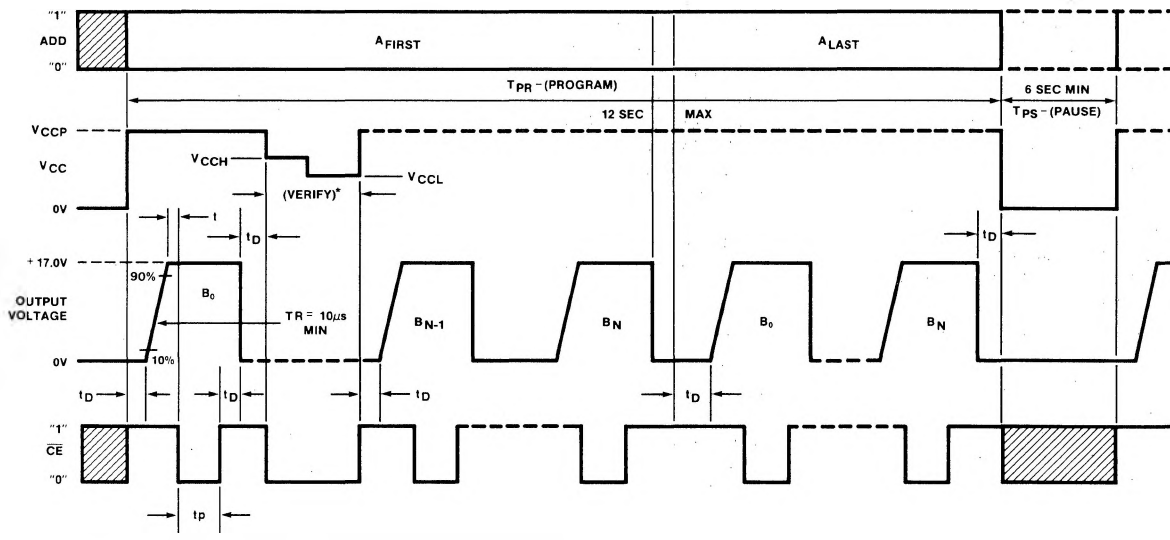
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. VS is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10K resistor to V_{CC}. Apply $\overline{CE}_1$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the CE input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.