signetics

HIGH SPEED MULTIPORT MEMORY (8x4 MULTIPORT RAM)

82S12 82S112

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S12/112 is a Schottky TTL 32 bit multiport memory organized in 8 words of 4 bits each. The device is ideally suited for high speed accumulators and buffer memories.

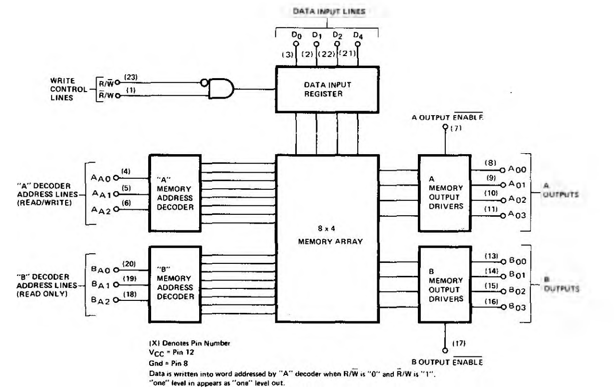
Stored data is addressed through 2 independent sets of 3-input decoders, and read out when the corresponding output enable line is low. Two separate word locations can, therefore, be read at the same time by enabling both the A and B output drivers. In addition, data can be read and written at the same time by utilizing the "A" address to specify the location of the word to be written, and the "B" address to specify the word to be read.

The 82S12/112 can be used in larger memory arrays since it includes all the control logic required to disable the chip and the outputs are open-collector devices suitable for "Wire-ORing."

FEATURES

- LOW CURRENT INPUT BUFFERS (–25μA TYPICAL)
- SEPARATE INPUT DECODERS FOR EACH WORD
- SEPARATE OUTPUT ENABLE LINES FOR EACH WORD
- OPEN COLLECTOR (82S12) OR TRI-STATE (82S112) OUTPUTS
- 2 WRITE ENABLE LINES
- FAST ACCESS (20 ns TYPICAL)
- USEFUL 8 X 4 ORGANIZATION
- TTL COMPATIBLE
- NON INVERTING DATA LINES

BLOCK DIAGRAM

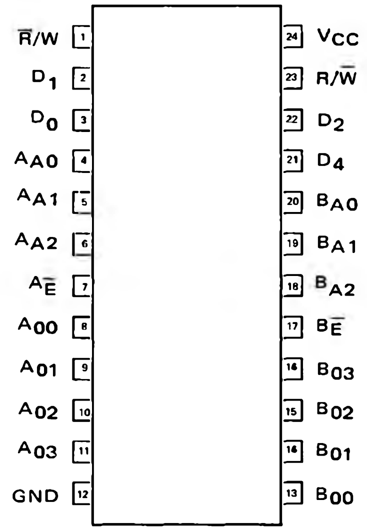


(X) Denotes Pin Number
V_{CC} = Pin 12
Gnd = Pin 8
Data is written into word addressed by "A" decoder when $R/\overline{W}$ is "0" and $\overline{R}/W$ is "1".
"one" level in appears as "one" level out.

APPLICATIONS

SCRATCH PAD MEMORY
BUFFER MEMORY
ACCUMULATOR REGISTER
GENERAL REGISTER

PIN CONFIGURATION



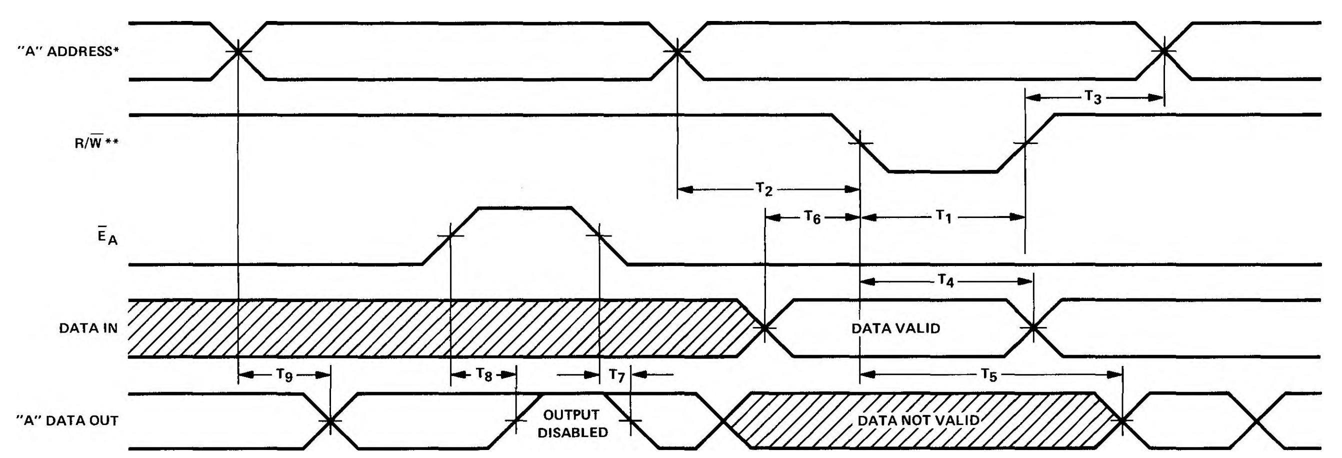
TRUTH TABLE

$\overline{R}/W$	$R/\overline{W}$	A OUTPUT $\overline{\text{ENABLE}}$	B OUTPUT $\overline{\text{ENABLE}}$	MODE	OUTPUTS A	OUTPUTS B
0	X	1	1	Outputs Disabled	"1"	"1"
0	X	1	0	Read	"1"	Data
0	X	0	1	Read	Data	"1"
0	X	0	0	Read	Data	Data
1	1	1	1	Read	"1"	"1"
1	1	1	0	Read	"1"	Data
1	1	0	1	Read	Data	"1"
1	1	0	0	Read	Data	Data
1	0	1	1	Write	"1"	"1"
1	0	1	0	Write	"1"	Data "B" Address
1	0	0	1	Write	Data Being Written	"1"
1	0	0	0	Write	Data Being Written	Data "B" Address

OBJECTIVE ELECTRICAL SPECIFICATIONS $0°C \leqslant T_A \leqslant 75°C$; $-4.75\ V \leqslant V_{CC} \leqslant 5.25\ V$.

CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS
	MIN.	TYP.	MAX.		
Input "0" Current			−250	μA	$V_{in} = 0.45$ V
Input "1" Current			25	μA	$V_{in} = 5.5$ V
Input "0" Threshold Voltage			0.85	V	
Input "1" Threshold Voltage	2.0			V	
Input Clamp Voltage	−1.2			V	$I_{in} = -18$ mA
Output "0" Current	16			mA	$V_{out} = 0.5$ V
Output "0" Current	9.6				$V_{out} = 0.45$ V
Output "1" Voltage(825112)	2.6			Volts	$I_{out} = -3.2$ mA
Output Off Current (82S12)			40	μA	$V_{out} \leqslant 5.5$ V
Output Off Current (82S112)	−40		+40	μA	$0.45 \leqslant V_{out} \leqslant 5.5$ V
Power Consumption		110/550	160/840	mA/mW	Outputs Enabled
Write Pulse Width T_1		15	30	ns	$T_A = 25°C$ Only
T_1			45	ns	$0°C \leqslant T_A \leqslant 75°C$
Address Set Up Time T_2		10		ns	
Address Hold Time T_3		0		ns	
Data Input Hold Time T_4		15		ns	
Write Access Time T_5		30		ns	
Data Input Set Up Time T_6		5		ns	
Output Enable Time T_7		10	20	ns	
Output Disable Time T_8		10	20	ns	
Address Access Time T_9		20	30	ns	

TIMING DIAGRAM



T_1 WRITE PULSE WIDTH – Width of write pulse (when R/W="1" and R/W="0")

T_2 ADDRESS SETUP TIME – Required delay between beginning of valid Address and beginning of Write pulse.

T_3 ADDRESS HOLD TIME – Required delay between end of Write pulse and end of valid Address.

T_4 DATA INPUT HOLD TIME – Required delay between start of Write pulse and end of Valid Data input.

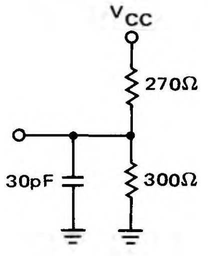
T_5 WRITE ACCESS TIME – Delay between beginning of Write pulse and Data Out at new value.

T_6 DATA INPUT SET-UP TIME – Required delay between beginning ov Valid Data Input and start of Write pulse.

T_7 OUTPUT ENABLE TIME – Delay between beginning of Output Enable high and when Data Output becomes valid.

T_8 OUTPUT DISABLE TIME – Delay between when Output Enable becomes low and Data Output is in off state.

T_9 ADDRESS ACCESS TIME – Delay between beginning of Valid Address (with Output Enable high, R/W high and R/W low) and when Data Output becomes valid.



A. C. LOAD

NOTES

*"B" Address functions identically in read mode. No write mode through B address decoder.

**R/W input is either the reverse of R/W or held high.

Outputs can be disabled during write cycle to penetrate a known output state during write.