DESCRIPTION

The 82S06 and 82S07 are ideal devices for use in Control Stores, small buffers, scratch pads, "cache" type buffer stores, memory maps, etc. The typical read time (the time between applying an address and obtaining valid output data) is 45ns. The typical write time (the time between applying one address and storing data) is 20ns. The circuit has 3 chip enable inputs which greatly simplifies the circuit configuration when used in large memories. The 82S06 and 82S07 also feature very low input loadings, 25 microamperes for a "1" state and -100 microamperes for "0".

The memories are TTL compatible and operate from single 5 volt supply.

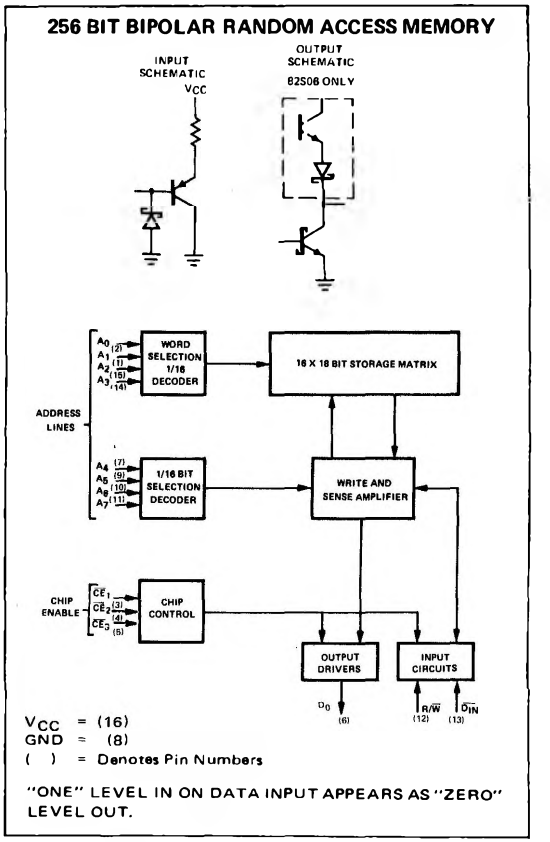
APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK

FEATURES

- **256 X 1 ORGANIZATION**
- **30 NANOSECOND ACCESS TIME TYPICAL**
- **LOW 1.5 mw/BIT POWER DISSIPATION TYPICAL**
- **LOW 100 μA INPUT LOADING**
- **TRI-STATE (82S06) OR OPEN COLLECTOR (82S07) OUTPUT**
- **ON CHIP DECODING**

BLOCK DIAGRAM



OBJECTIVE ELECTRICAL CHARACTERISTICS (T_A = 0 to 75°C, V_{CC} = 5.0V ±5) Note 1, 2, 3

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Input Current		-10	-100	μA	V_{in} = 0.5V	
"1" Input Current		<1.0	25	μA	V_{in} = 5.25V	
"0" Output Voltage		.35	.5	V	I_{out} = 16mA	
Output Leakage Current (82S07)		<1.0	100	μA	$\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$ = "1", V_{out} = 2.7V	
Output "off" Current (82S06)		<1.0	±100	μA	$\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$ = "1", 0.5 ≤ V_{out} ≤ 2.7V	
"1" Output Voltage (82S06)	2.6			V	$\overline{CE}_1 = \overline{CE}_2 = \overline{CE}_3$ = "0" I_{out} = -3.2mA	
"0" Input Threshold			.85	V		
"1" Input Threshold	2.0			V		
Power Consumption		110/550	130/683	mA/mW		
Input Clamp Voltage	-1.5	-.8		V	I_{in} = - 12mA	
Input Capacitance		5		pF		
Output Capacitance		8		pF		

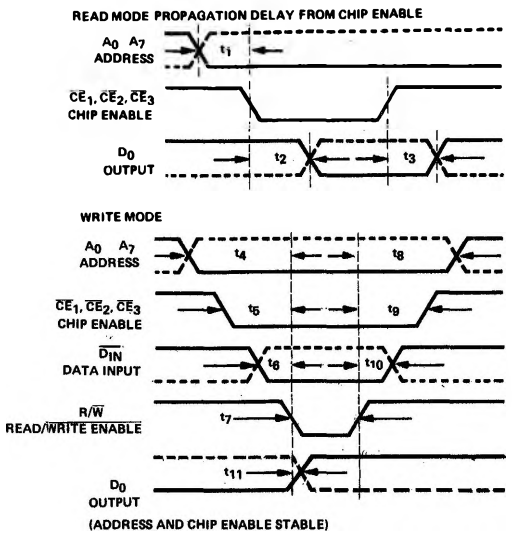
OBJECTIVE ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

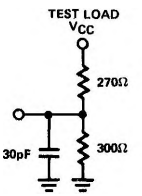
CHARACTERISTICS		LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	NOTES
Access Time—Address to Output			45	65	ns		4,5
Address Set-Up Time (read)	t_1		10		ns		
Propagation Delay							4,5
Chip Enable to Output Enable	t_2		25	40	ns		
Propagation Delay							• 4,5
Chip Enable to Output Disable	t_3		25	40	ns		
Address to Write Enable							4,5
Set-Up Time	t_4	25	5		ns		
Chip Enable to Write Enable							4,5
Set-Up Time	t_5	10	0		ns		
Data Input to Write Enable							4,5
Set-Up Time	t_6	10	0		ns		
Write Enable Pulse Width	t_7	30	15		ns		4,5
Address Hold Time	t_8	10	0		ns		4,5
Chip Enable Hold Time	t_9	10	0		ns		4,5
Data Input Hold Time	t_{10}	10	0		ns		4,5
Write Enable Propagation Delay	t_{11}		30	40	ns		4,5
Output Short Circuit Current (82S06)		−20		−100	mA	V_{out} = 0V	4,5

NOTES:

1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.
3. Applied voltages must not exceed 6.0V, Input currents must not exceed ±30mA, Output currents must not exceed ±100mA, Storage temperature must be between -60°C to +150°C.
4. Refer to Timing Diagram for definition of terms and test load.
5. Rise and fall times for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5 volts.

TIMING DIAGRAM





t_1 = set up time for an address input to chip enable for valid data at output
t_2 = propagation delay from chip enable to valid data at output
t_3 = propagation delay from chip disable to output turn off
t_4 = set up time from address to write enable
t_5 = set up time from chip enable to write enable
t_6 = set up time from data input to write enable
t_7 = write enable pulse width
t_8 = hold time for address from write enable
t_9 = hold time for chip enable from write enable
t_{10} = hold time for data input from write enable
t_{11} = propagation delay from write enable to valid data at output