DESCRIPTION

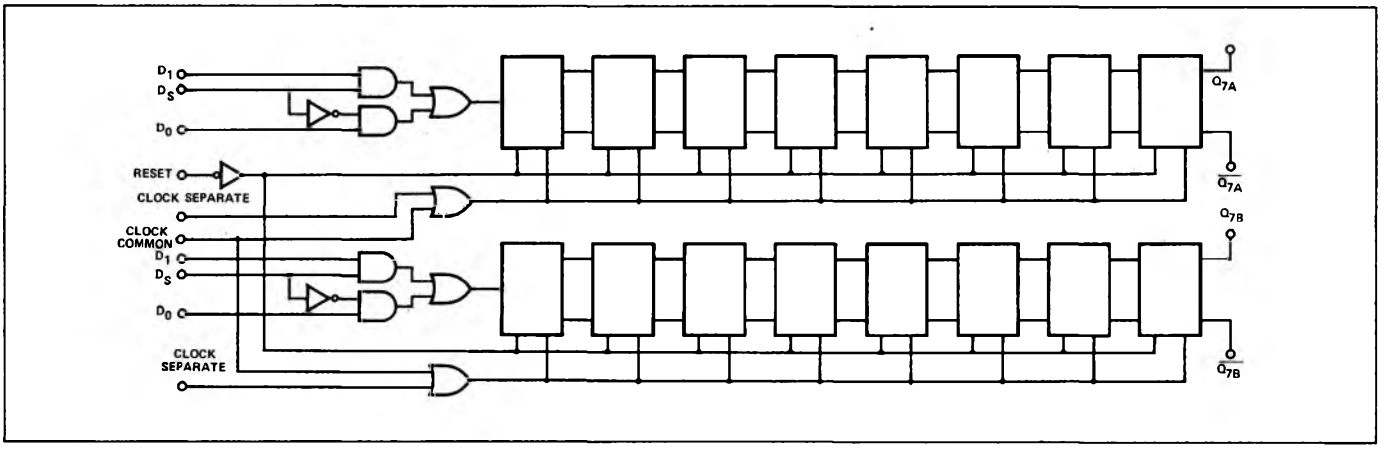
The 8277 is a dual 8-Bit Shift Register which provides the designer with sixteen (16) bits of serial storage operating at a typical shift rate of 20MHz. Features of the 8277 are:

1. TRUE and COMPLEMENT outputs are provided on each register's eighth bit.
2. Positive edge triggering on clock input.
3. SEPARATE CLOCK lines (pins 7 and 10) for each 8-bit register are provided as well as a COMMON CLOCK line (pin 9) for all sixteen storage bits.
4. Common RESET (pin 1).
5. AND-OR gating to the input of each 8-bit register is provided to accomplish the multiplex function.
6. Direct replacement for 9328.

TRUTH TABLE

D_S	D_0	D_1	Reset	Function
0	0	x	1	Shift in "0"
0	1	x	1	Shift in "1"
1	x	0	1	Shift in "0"
1	x	1	1	Shift in "1"
x	x	x	0	Reset "Q" to "0"

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

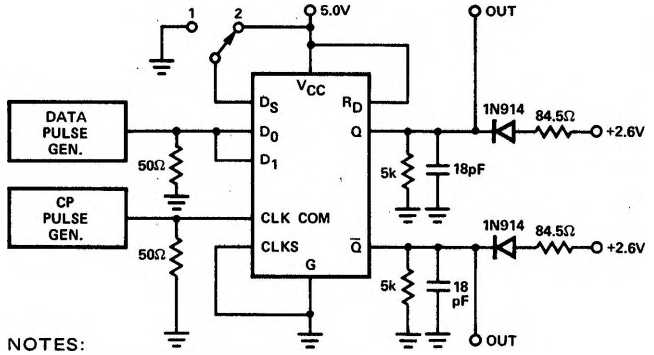
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA D_1, D_0	DATA SELECT	CLK COMMON	CLK SEP	RESET	OUTPUTS	
"1" Output Voltage (Q)	2.6	3.5		V	2.0V	2.0V	Pulse	0.8V	2.0V	-800μA	6
"1" Output Voltage (Q)	2.6	3.5		V	0.8V	2.0V	0.8V	Pulse		-800μA	6
"0" Output Voltage (Q)			0.4	V	0.8V	0.8V	Pulse	0.8V		16mA	7
"0" Output Voltage (Q)			0.4	V	2.0V	0.8V	Pulse	0.8V		16mA	7
"0" Input Current											
Data, Reset, Data Select			-1.6	mA	0.4V	0.4V			0.4V		
Clock Separate			-1.6					0.4V			
Clock Common			-3.2	mA			0.4V				
"1" Input Current											
Data, Reset, Clock Separate			40	μA	4.5V	4.5V		4.5V	4.5V		
Clock Common			80	μA			4.5V				
Power/Current Consumption			540/ 103	mW mA							11
Input Voltage Rating											
All Inputs	5.5			V	10mA	10mA	10mA	10mA	10mA		

T_A = 25° C and V_{CC} = 5.0V

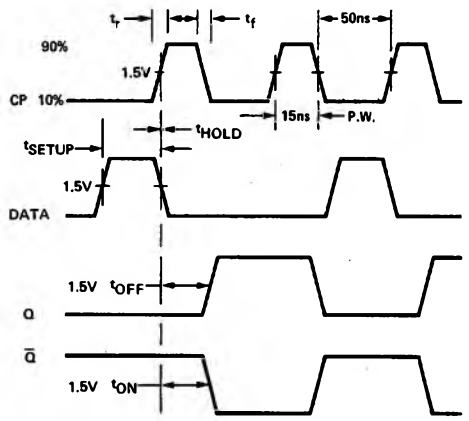
CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	DATA D_1, D_0	DATA SELECT	CLK COMMON	CLK SEP	RESET	OUTPUTS	
Turn-on Delay											
Clock To Output		25	40	ns							10
Reset To Output		25	40	ns							10
Turn-off Delay											
Clock To Output		25	40	ns							10
Reset To Output		25	40	ns							10
Clock Pulse Width	15			ns							10
Shift Rate	15	20		MHz							10
Data Set-up Time		20	30	ns							10
Data Hold Time		5	10	ns							10

NOTES:
1. All voltage measurments are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive Logic Definitions: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Manufacturer reserves the right to make design and process changes and improvements.
9. Clock input is driven by a 1kHz square wave for at least 8 cycles prior to measurement.
10. Refer to AC Test Figure.
11. V_{CC} = 5.25V

AC TEST FIGURE AND WAVEFORMS



NOTES:
1. Each register is tested separately.
2. All T delay measurements taken at 1.5V level.
3. Tie all unused inputs to 2.6V.
4. 18 pF on outputs includes probe and jug capacitance.



CLOCK PULSE:
P.A. = 3.0V
P.R.R. = 15 MHz
P.W. = 15 ns
$T_r = T_f$ = 5ns

DATA PULSE:
P.A. = 3.0V
P.R.R. = 7.5 MHz
P.W. = 25 ns
$T_r = T_f$ = 5 ns
T_{SETUP} = 25 ns
T_{HOLD} = 0 ns.

TYPICAL APPLICATION

8-BIT SERIAL ADD/SUBTRACTOR