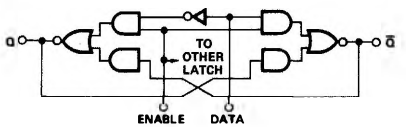
DESCRIPTION

The 8275 is a QUAD LATCH circuit designed to provide temporary storage of four bits of information. A common application is as a holding register between a counter and a display driver (such as the 8280 and 8T01.) Separate enable lines to latches 1-2 and 3-4 allow individual control of each pair of latches. Initially, data is transferred on the rising edge of the enable pulse. While the enable is high, output Q follows the data input. When the enable falls, the input data present at fall time is retained at the Q output. Both Q and $\overline{Q}$ are accessible.

LOGIC DIAGRAM AND TRUTH TABLE



Refer to Page 3-11 for Pin Configuration

(Each Latch)			
ENABLE	DATA	Q	$\overline{Q}$
1	1	1	0
1	0	0	1
0	1	*	*
0	0	*	*

*No Change.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUT	ENABLE INPUT	OUTPUTS	
"1" Output Voltage (Q, $\overline{Q}$)	2.6	3.5		V			-800μA	6, 11
"0" Output Voltage (Q, $\overline{Q}$)			0.4	V			16mA	7, 11
"0" Input Current (Data)	-0.1		-3.2	mA	0.4V	5.25V		
"0" Input Current (Enable)	-0.1		-6.4	mA	5.25V	0.4V		
"1" Input Current (Data)			80	μA	4.5V	0.0V		
"1" Input Current (Enable)			160	μA	0.0V	4.5V		

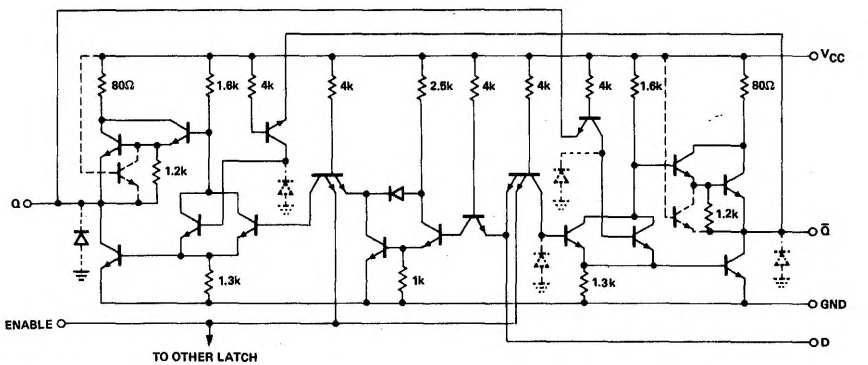
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
	MIN.	TYP.	MAX.	UNITS	DATA INPUT	ENABLE INPUT	OUTPUTS	
t_{setup} (1) at D input		12	20	ns				8, 12
t_{setup} (0) at D input		14	20	ns				8, 12
t_{hold} (1) at D input	0	15		ns				8, 13
t_{hold} (0) at D input	0	6		ns				8, 13
t_{pd} (1) D to Q		16	30	ns				8
t_{pd} (0) D to Q		14	25	ns				8
t_{pd} (1) D to $\overline{Q}$		24	40	ns				8
t_{pd} (0) D to $\overline{Q}$		7	15	ns				8
t_{pd} (1) E to Q		16	30	ns				8
t_{pd} (0) E to Q		12	20	ns				8
t_{pd} (1) E to $\overline{Q}$		16	30	ns				8
t_{pd} (0) E to $\overline{Q}$		12	20	ns				8
Power Consumption/Supply Current		205/39	265/50	mW/mA				11
Input Voltage Rating (Data)	5.5			V	10mA	0.0V		
Input Voltage Rating (Enable)	5.5			V	0.0V	10mA		
Output Short Circuit Current	-20		-70	mA	0.0V		0.0V	9

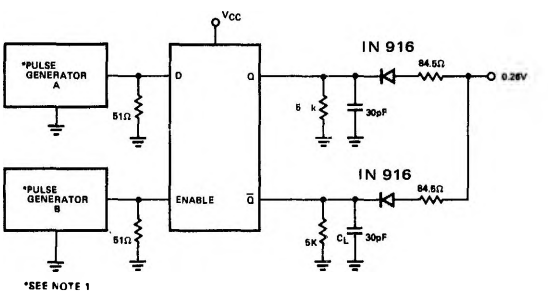
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Not more than one output should be shorted at a time.
10. Inputs for output voltage test is per TRUTH TABLE with threshold levels of 0.8V for logical "0" and 2.0V for logical "1".
11. V_{CC} = 5.25 volts.
12. t_{setup} is defined as the time prior to the fall of the clock.
13. t_{hold} is defined as the time after the fall of the clock.

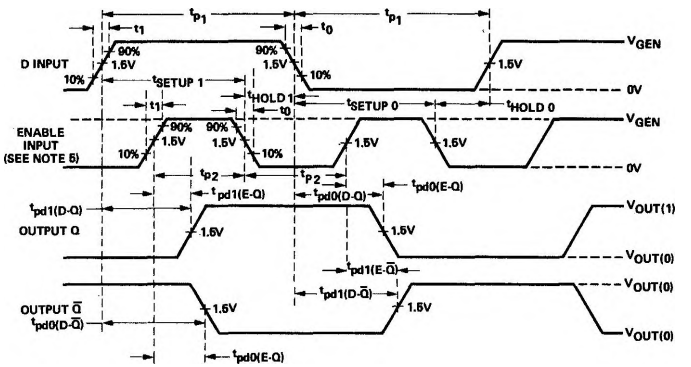
SCHEMATIC DIAGRAM



AC TEST FIGURE



AC TEST WAVEFORMS



NOTES:

1. The pulse generators have the following characteristics: V_{gen} = 3V, $t_1 = t_0 \leq 10$ns, and $Z_{out} \approx 50\Omega$. For pulse generator A, t_{p1} = 1µs and PRR = 500kHz. For pulse generator B, tp2 = 500ns and Prr = 1MHz. Positions of D-input and enable input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. When measuring $t_{pd}1$ (D-Q), $t_{pd}0$ (D-Q), $t_{pd}0$ (D-$\overline{Q}$), and $t_{pd}1$(D-$\overline{Q}$), enable input must be held at logical 1.

TYPICAL APPLICATION

OUTPUT STROBING OF RIPPLE COUNTER TO ACHIEVE SYNCHRONOUS OUTPUT CHANGES