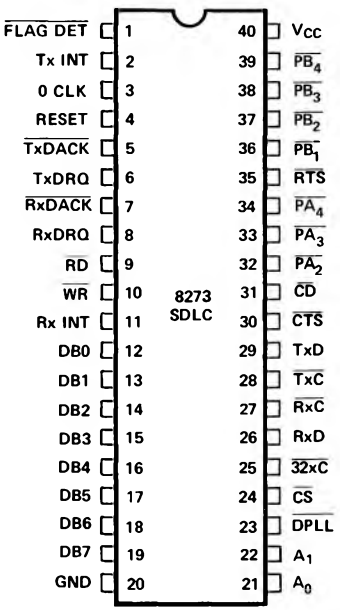
8273
SDLC PROTOCOL CONTROLLER

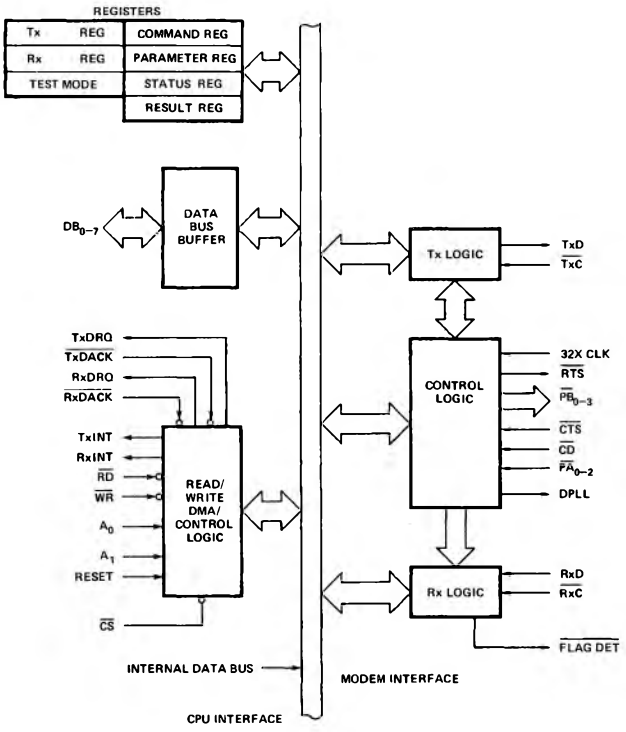
- **IBM (SDLC) Compatible**
- **Full Duplex Operation—56K BAUD**
- **SDLC Loop Operation**
- **User Programmable Modem Control Ports**
- **Programmable NRZI Encode/Decode**
- **N-Bit Reception Capability**
- **Digital Phase Locked Loop—Clock Recovery**
- **Minimum CPU Overhead**
- **Single +5Volt Supply**
- **40 Pin Package**

The 8273 SDLC (Synchronous Data Link Control) Protocol controller is a single chip device designed to support the SDLC protocol within a microcomputer system environment. Its internal supervisory instruction set is oriented to frame level (SDLC) functions with a minimum of CPU overhead.

PIN CONFIGURATION



BLOCK DIAGRAM



General

The IBM Synchronous Data Link Control (SDLC) communication protocol is a bit oriented communication protocol vs the BI-SYNC protocol which is character or code oriented. The SDLC protocol greatly reduces the overall CPU software on one hand and increases the throughput on the other because of its ability to go full-duplexed mode.

The 8273 SDLC chip is designed to handle the IBM SDLC protocol with minimum CPU software. The 8273 handles the zero-insertion technique used in SDLC protocol, as well as performing NRZI encoding and decoding for the data. Modem handshake signals are provided so that the CPU intervention is minimized. The FCS (Frame check sequence) is also generated and checked by the SDLC chip as well as Flags (01111110) and Idle characters.

One implementation of SDLC is the Loop-configuration typified by IBM 3650 Retail Store System which can also be handled by the 8273 by going into 1-bit delay mode. In such configuration a two wire pair can be effectively used for data transfer between controllers and loop stations. Digital phase Locked Loop pin-out can be used by the loop station without the presence of an accurate 1X clock.

Hardware Description

The 8273 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	I/O	Description
V_{CC}		+5V supply
GND		Ground
RESET	I	A high signal on this pin will force the 8273 to an idle state. The 8273 will remain idle until a command is issued by the CPU. The modem interface output signals are forced high.
$\overline{CS}$	I	The I/O Read and I/O Write inputs are enabled by the chip.
DB_7-DB_0	I/O	The Data Bus lines are bidirectional three-state lines.
$\overline{WR}$	I	The Write signal is used to control the transfer of either a command or data from CPU to the 8273.
$\overline{RD}$	I	The Read signal is used to control the transfer of either a data byte or a status word from the 8273 to the CPU.
TxINT	O	The Transmitter interrupt signal indicates that the transmitter logic requires service.
RxINT	O	The Receiver interrupt signal indicates that the Receiver logic requires service.
TxDRQ	O	The Transmitter DMA Request signal indicates the transmitter Buffer is empty and is ready to transmit another data byte.
RxRDQ	O	The Receiver DMA Request signal indicates the Receiver Buffer is full.
$\overline{TxDACK}$	I	The Transmitter DMA acknowledge signal notifies the 8273 that the TxDMA cycle has been granted.
$\overline{RxDACK}$	I	The Receiver DMA acknowledge signal notifies the 8273 that the RxDMA cycle has been granted.
A_1-A_0	I	These two lines are used to select the destination or source of data to be accessed by the control logic.
TxD	O	The NRZI encoded data are transmitted through the TxD line.
$\overline{TxC}$	I	The transmitter clock controls the TxD BAUD rate.
RxD	I	The Receiver Data line receives the NRZI encoded data from the communication data channel.
$\overline{RxC}$	I	The Receiver clock is the 1X BAUD rate that RxD is received.
$\overline{32X\ CLK}$	I	The 32X clock is used to provide clock recovery when Asynchronous modem is used. In loop configuration the loop station can run without an accurate 1X clock by using the 32X CLK.
$\overline{DPLL}$	O	Digital Phase Locked Loop output can be tied to RxC and/or TxC when 1X clock is not available. DPLL is used with 32X CLK.
$\overline{FLAG\ DET}$	O	Flag Detect signals that a flag (01111110) has been detected.
$\overline{RTS}$	O	Request to send signals the terminal is ready to transmit Data.
$\overline{CTS}$	I	Clear to send signals that the modem is ready to accept data for transmission.
$\overline{CD}$	I	Carrier Detect signals that the line transmission has started and the 8273 may begin sample data on RxD line.
$\overline{PA_{0\text{-}2}}$	I	General Purpose input Ports. The logic levels on these lines can be Read by the CPU through the Data Bus Buffer.
$\overline{PB_{0\text{-}3}}$	O	General Purpose output Ports. The CPU can write these output lines through Data Bus Buffer.
ϕ CLK	I	A 4 MHz Square Wave Clock.

Principles of Operation

The 8273 is fully compatible with Intel microprocessors. It accepts commands from the CPU, executes these Commands and provides a Result at the end of execution. Communication with CPU is through the activating of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ pins. The A_1A_0 select the appropriate registers on chip:

A1	A0	CS•RD	CS•WR
0	0	Status Reg	Command Reg
0	1	Result Reg	Parameter Reg
1	0	TX Reg	—
1	1	RX Reg	—

The SDLC chip operation is composed of the following general sequence of events:

The Command Phase

During the Command Phase, the CPU issues a command byte to the 8273. The command byte provides a general description of the type of operation requested. Many operations require more detailed information about the command. In such case, from zero to four parameters are written following the command byte to provide such information. The various commands that the 8273 can recognize are listed in the Software Operation Section.

The Execution Phase

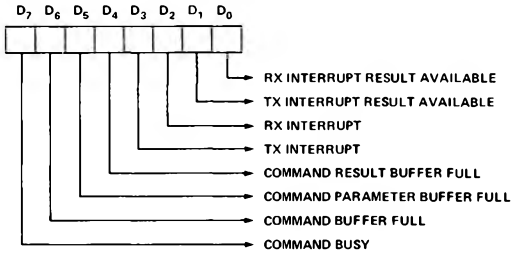
After the last parameter is written into the 8273, the SDLC chip enters the Execution Phase. During this phase there is no need for CPU involvement. The system might interface with the 8257 (DMA controller) if programmed to do so, for high speed data transfers (see System Diagram). On the other hand for low speed data rate communication TxINT and RxINT can be used.

The Result Phase

During the Result Phase, the SDLC chip notifies the CPU of the outcome of the command execution. This phase may be initiated by:

1. The successful completion of an operation.
2. An error detected during an operation.

In the Result Phase, the CPU Reads the Status Register which provides the following information.

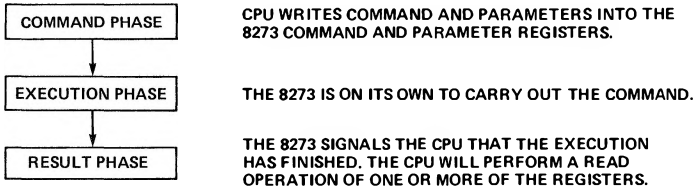


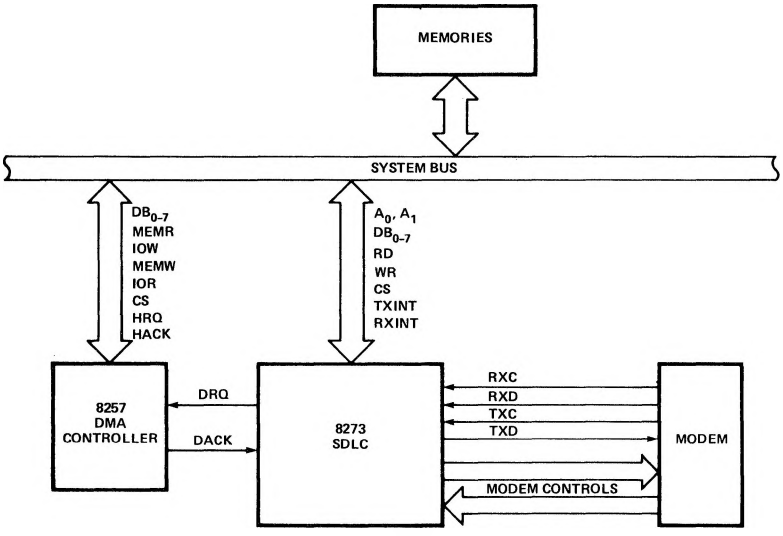
Based on the status of the Status Register, the CPU may Read the Tx Reg, Rx Reg, or Result Register, if more information is needed.

Software Operation

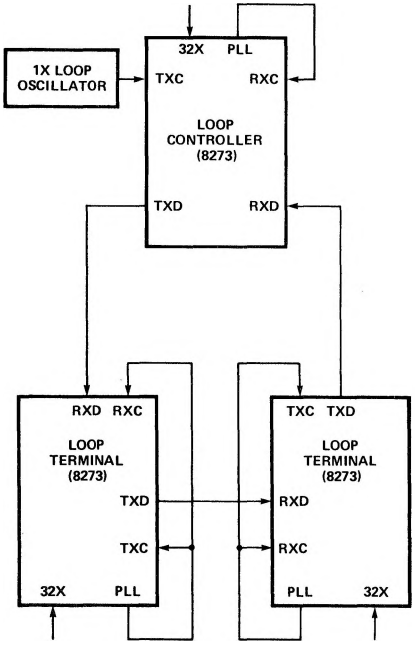
The 8273 can accept many powerful commands from the CPU. The following is a list of such commands (associated parameters not shown).

General Receive
Selective Receive
Selective Loop Receive
End of Polling Search
Receive Disable
Transmit Frame
Loop Transmit
Transparent Transmit
Abort Tx Frame
Abort Loop Tx
Abort Transparent Tx
Read Port A
Read Port B
Set/Reset 1 Bit Delay
Set/Reset Serial I/O
Set/Reset Operating Mode
Set/Reset Port A/B Bit

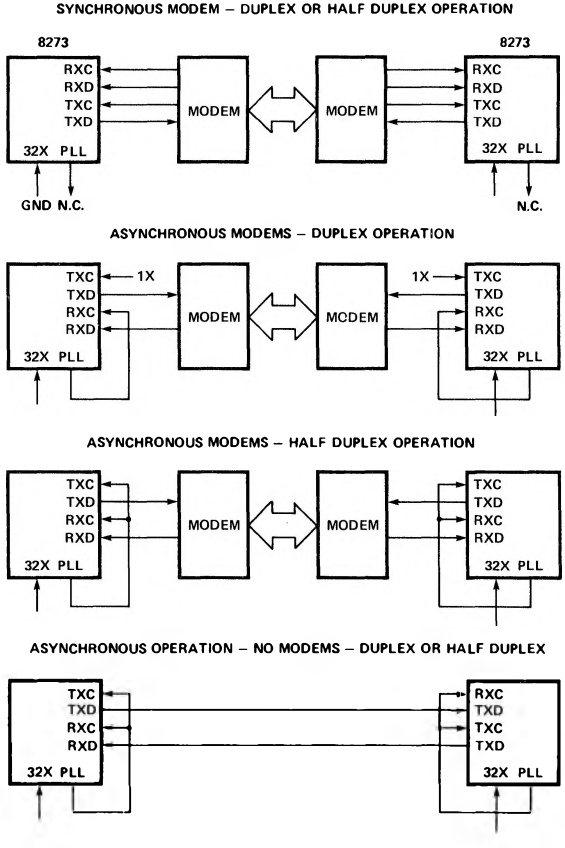




8273 SYSTEM DIAGRAM



SDLC LOOP APPLICATION



8273 MODEM OPERATION