

REFER TO PAGE 16 FOR B, E AND R PACKAGE PIN CONFIGURATIONS.

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8273, 10-Bit Shift Register is an array of binary elements interconnected to perform the serial-in, parallel-out shift function. This device utilizes a common buffered reset and operates from either a positive or negative edge clock pulse. Clock 1 is triggered by a negative going clock pulse and clock 2 is triggered by a positive going clock pulse. The unused clock input performs the inhibit function. The circuit configuration is arranged as a single serial input register with ten true parallel outputs.

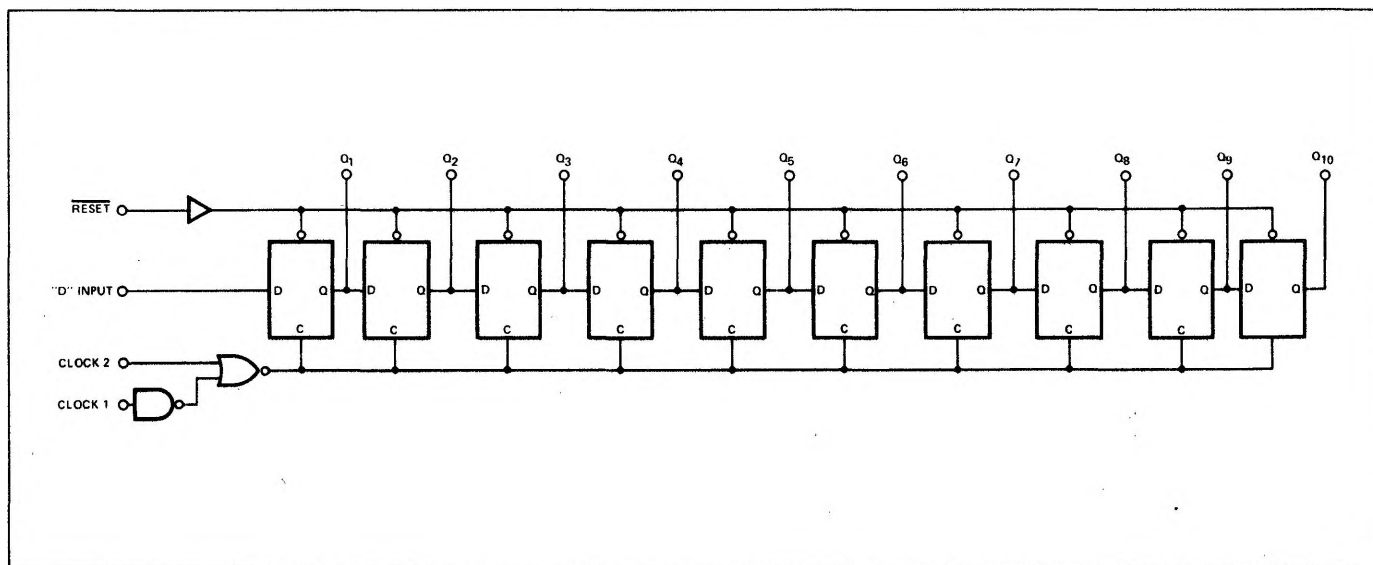
TRUTH TABLE

INPUT	RESET	CLOCK 1	CLOCK 2	$Q_n + 1$
1	1	Pulse	0	1
0	1	Pulse	0	0
1	1	1	Pulse	1
0	1	1	Pulse	0
1	1	Pulse	1	Q
0	1	Pulse	1	Q
1	1	0	Pulse	Q
0	1	0	Pulse	Q

NOTE: The unused clock input performs the INHIBIT function.

RESET = 0 \Rightarrow Q = 0

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS	"D" INPUT	CLOCK 1	CLOCK 2	RESET		
"1" Output Voltage	2.6	3.4		V	2.0V	Pulse	0.8V		-500 μ A	6
"0" Output Voltage		0.2	0.4	V	0.8V	Pulse	0.8V		9.6mA	7
"0" Input Current										
"D" Input	-0.1		-1.6	mA	0.4V					
Clock 1	-0.1		-1.6	mA		0.4V				
Clock 2	-0.1		-1.6	mA			0.4V			
Reset	-0.1		-1.6	mA				0.4V		
"1" Input Current										
"D" Input			40	μ A	4.5V					
Clock 1			40	μ A		4.5V				
Clock 2			40	μ A			4.5V			
Reset			40	μ A				4.5V		

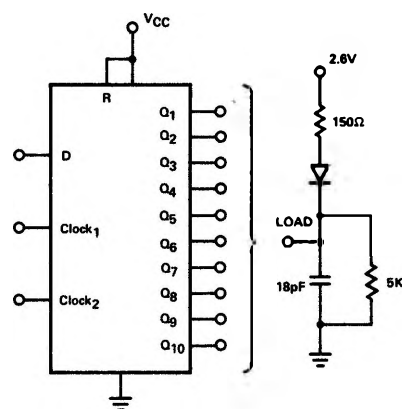
$T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{V}$

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS	"D" INPUT	CLOCK 1	CLOCK 2	RESET		
Max. Data Transfer Rate	25	35		MHz						
Turn-On Delay										
Clock 1 to Output		32	40	ns			0.0V	4.5V		
Clock 2 to Output		28	40	ns				4.5V		
Reset to Output		35	50	ns		4.5V				
Turn-Off Delay										
Clock 1 to Output		25	40	ns			0.0V			
Clock 2 to Output		19	40	ns		4.5V				
Clock Pulse Width										
Clock 1		16	25	ns			0.0V			
Clock 2		12	20	ns		4.5V				
Set-Up Time ($t_{\text{set-up}}$)										
Clock 1			15	ns			0.0V			
Clock 2			10	ns		4.5V				
Hold Time (t_{hold})										
Clock 1			15	ns			0.0V			
Clock 2			10	ns		4.5V				
Power Consumption			540	mW						8
Short Circuit Output Current	-20		-70	mA						
Input Voltage Rating (All Inputs)	5.5			V	10mA	10mA	10mA	10mA		

NOTES:

- All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current flow is defined as into the terminal referenced.
- Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC} .
- $V_{CC} = 5.25\text{V}$.
- Manufacturer reserves the right to make design and process changes and improvements.
- See AC Test Figure.

AC TEST FIGURE AND WAVEFORMS



NOTES:

- Unused clock 2 input must be grounded.
- Input pulse characteristics
CLOCK
Amplitude = 3.0V
 $t_r = t_f \leq 5\text{ns}$.