DESCRIPTION

The 82S116 and 82S117 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading to 25μA for a "1" level, and −100μA for a "0" level.

During WRITE operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as "Cache", buffers, scratch pads, writable control stores, etc.

Both 82S116 and 82S117 devices are available in the commercial temperature range. For the commercial temperature range, (0°C to +75°C) specify N82S116/117, B or F.

FEATURES

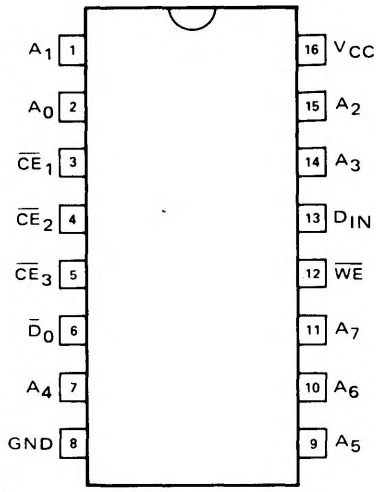
- **ORGANIZATION – 256 X 1**
- **ADDRESS ACCESS TIME – 40ns, MAXIMUM**
- **WRITE CYCLE TIME – 25ns, MAXIMUM**
- **POWER DISSIPATION – 1.5mW/BIT TYPICAL**
- **INPUT LOADING – (−100μA) MAXIMUM**
- **OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE**
- **ON-CHIP ADDRESS DECODING**
- **OUTPUT OPTION:**
  TRI-STATE – 82S116
  OPEN COLLECTOR – 82S117
- **16 PIN CERAMIC DIP**

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

B, F PACKAGE*



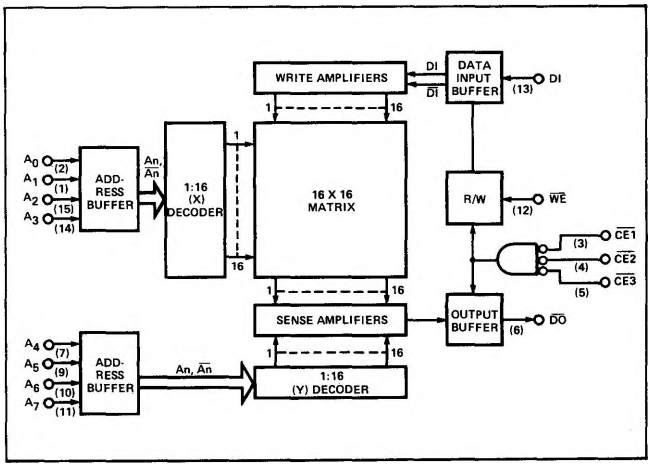
*B – Plastic
C – Cerdip

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S116	82S117
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	1
WRITE "1"	0	0	1	0	0
DISABLED	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_{OUT}	High Level Output Voltage (82S117)	+5.5	Vdc
V_O	Off-State Output Voltage (82S116)	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant 75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS		LIMITS			UNIT	NOTES
				MIN	TYP[2]	MAX		
V_{IH}	High-Level Input Voltage	V_{CC} = 5.25V		2.0			V	
V_{IL}	Low-Level Input Voltage	V_{CC} = 4.75V				0.85	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = −12 mA			−1.0	−1.5	V	1,8
V_{OH}	High-Level Output Voltage (82S116)	V_{CC} = 4.75V, I_{OH} = −3.2 mA		2.6			V	1,6
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 16 mA			0.35	0.45	V	1,7
I_{OLK}	Output Leakage Current (82S117)	V_{OUT} = 5.5V			1	40	μA	5
$I_{O(OFF)}$	HI-Z State Output Current (82S116)	V_{OUT} = 5.5V			1	40	μA	5
		V_{OUT} = 0.45V			−1	−40	μA	5
I_{IH}	High-Level Input Current	V_{CC} = 5.25V, V_{IN} = 5.5V			1	25	μA	8
I_{IL}	Low-Level Input Current	V_{CC} = 5.25V, V_{IN} = 0.45V			−10	−100	μA	8
I_{OS}	Short-Circuit Output Current (82S116)	V_{CC} = 5.25V, V_O = 0V		−20		−70	mA	3
I_{CC}	V_{CC} Supply Current (82S116)	V_{CC} = 5.25V			80	115	mA	4
	V_{CC} Supply Current (82S117)	V_{CC} = 5.25V			80	115	mA	4
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0V		5		pF	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V			8		pF	

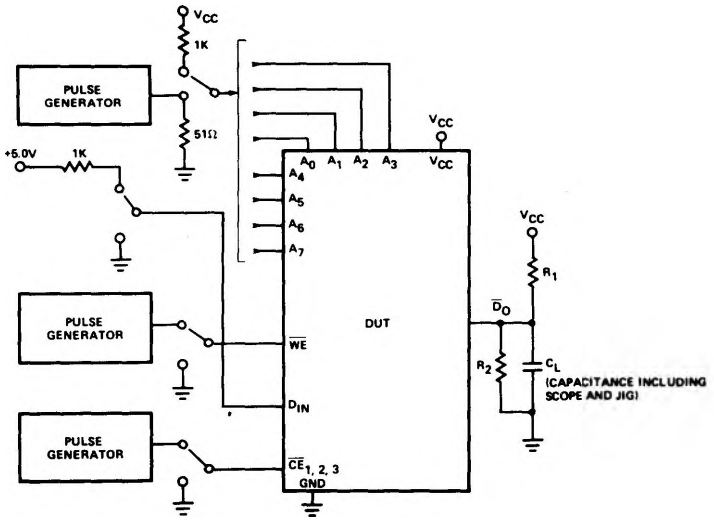
NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with a logic "0" stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
7. Measured with a logic "1" stored. Output sink current is supplied through a resistor to V_{CC}.
8. Test each input one at the time.

SWITCHING CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

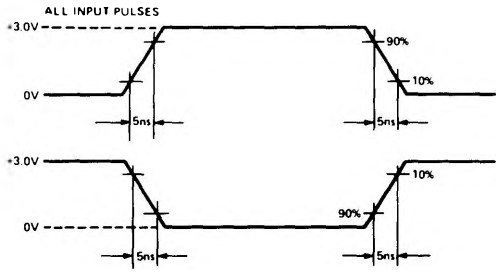
PARAMETER		TEST CONDITIONS	LIMITS			UNIT	NOTE
			MIN	TYP[1]	MAX		
Propagation Delays							
T_{AA}	Address Access Time	$R_1 = 270\Omega$ $R_2 = 600\Omega$ $C_L = 30pF$		30	40	ns	
T_{CE}	Chip Enable Access Time			15	25	ns	
T_{CD}	Chip Enable Output Disable Time			15	25	ns	
T_{WD}	Write Enable to Output Disable Time			30	40	ns	
Write Set-up Times							
T_{WSA}	Address to Write Enable		0	-5		ns	
T_{WSD}	Data In to Write Enable		25	15		ns	
T_{WSC}	$\overline{CE}$ to Write Enable		0	-5		ns	
Write Hold Times							
T_{WHA}	Address to Write Enable		0	-5		ns	
T_{WHD}	Data In to Write Enable		0	-5		ns	
T_{WHC}	$\overline{CE}$ to Write Enable		0	-5		ns	
T_{WP}	Write Enable Pulse Width		25	15		ns	2

AC TEST LOAD

LOADING CONDITION



INPUT PULSES

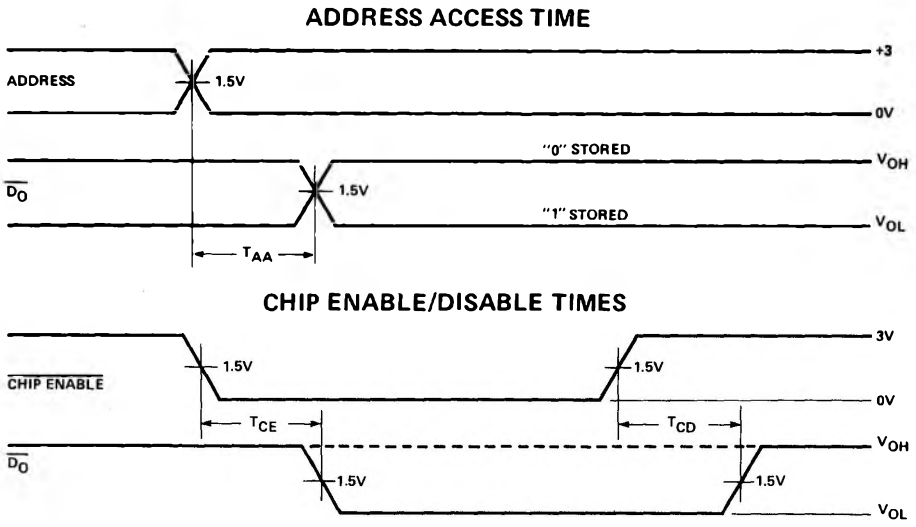


MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

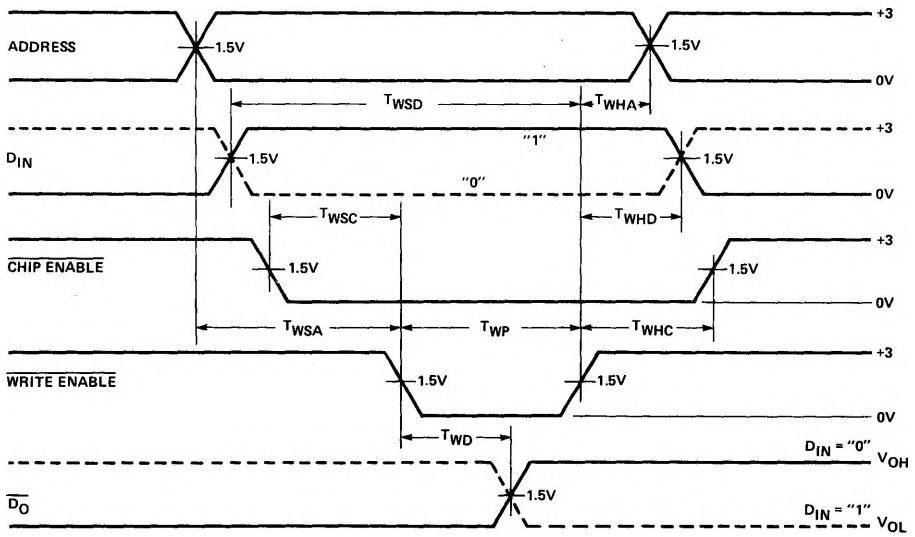
NOTES:
1. Typical values are at $V_{CC} = +5.0V$, and $T_A = +25°C$.
2. Minimum required to guarantee a WRITE into the slowest bit.

SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.