DESCRIPTION

The 8223 is a TTL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to the high state when the chip enable input is high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which permits wired AND operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum. The 8223 may be programmed to any desired pattern by the user. (See fusing procedure.) This feature is ideal for prototype hardware and systems requiring propriety codes.

A Truth Table/Order Blank is included on page 4-43 for ordering custom patterns.

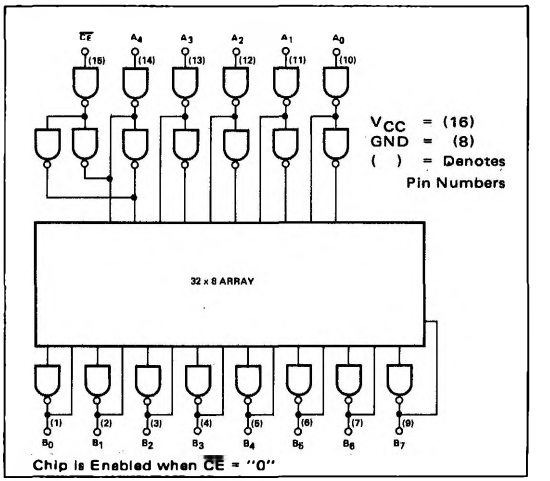
FEATURES

- **BUFFERED ADDRESS LINES**
- **ON THE CHIP DECODING**
- **CHIP ENABLE CONTROL LINE**
- **OPEN COLLECTOR OUTPUTS**
- **DIODE PROTECTED INPUTS**
- **NO SEPARATE FUSING PINS**
- **BOARD LEVEL PROGRAMMABLE**

APPLICATIONS

PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS ($S8223$ $-55°C \leq T_A \leq +125°C$ $N8223$ $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$)

CHARACTERISTICS	LIMITS				"0" A_n	"1" A_n	$\overline{\text{CHIP ENABLE}}$	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS					
"1" Output Leakage Current (N8223–)			100	μA			2.0V		13
(S8223–)			250	μA					
"0" Output Voltage (N8223–) (S8223–)			0.4	V	0.8V	2.0V	0.8V	9.6mA	6,10
(N8223–)			0.5	V	0.8V	2.0V	0.8V	16mA	6,10
"1" Input Current									
An, Address			40	μA		4.5V			
$\overline{\text{Chip Enable}}$ Input			80	μA			4.5V		
"0" Input Current									
An, $\overline{\text{Chip Enable}}$	-0.1		-1.6	mA	0.4V		0.4V		

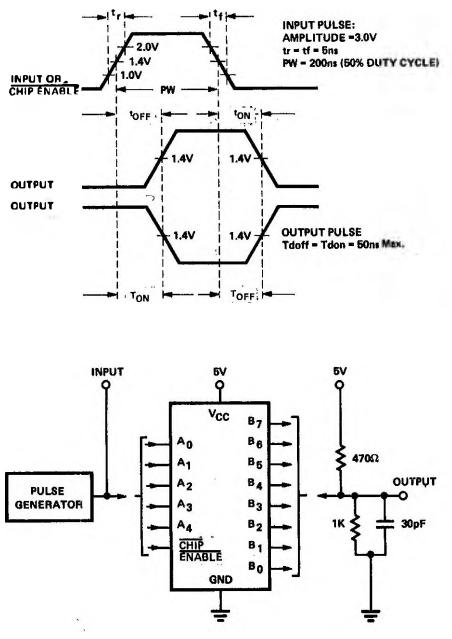
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				"0" A_n	"1" A_n	$\overline{\text{CHIP ENABLE}}$	OUTPUTS	NOTES
	MIN.	TYP.	MAX.	UNITS					
Propagation Delay									
An to Bn		35	50	ns				DC F.O.=12	7,12
$\overline{\text{Chip Enable}}$ to B_n		35	50	ns		4.5V		DC F.O.=12	7,12
Power Consumption		310/62	400/77	mW/mA		4.5V	4.5V		14
Input Latch Voltage	5.5			V			10mA		11

NOTES:

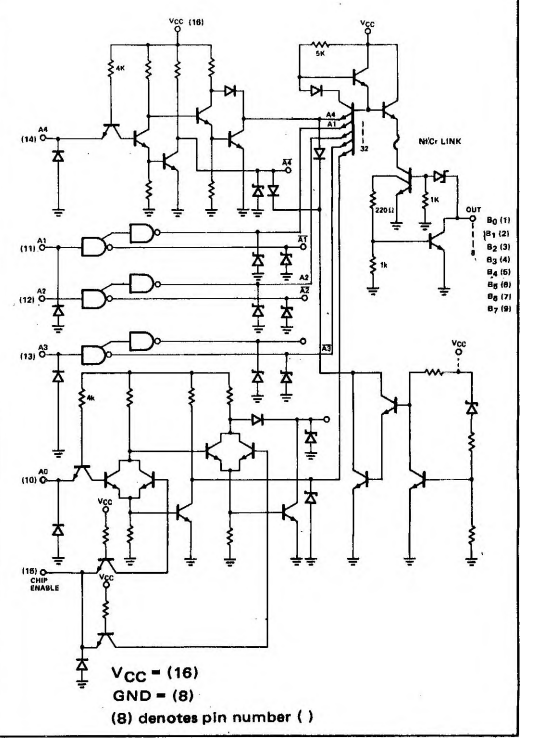
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1" "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8mA.
8. One AC fan-out is defined as 50pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed test conditions, see AC testing.
13. Connect an external 1k resistor from V_{CC} to the output terminal for this test.
14. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS



Ground Pin 15 When Testing Address-Output Delays

SCHEMATIC DIAGRAM



8223 PROGRAMMING PROCEDURE

The 8223 may be programmed by using Curtis Electro Devices, Spectrum Dynamics or Data I/O Programmers.

The 8223 Standard part is shipped with all outputs at logical "0". To write a logical "I" proceed as follows:

Programming Procedure A

Simple Programming Procedure using "bench" Equipment

1. Start with pin 8 grounded and V_{CC} removed from pin 16.
2. Remove any load from the outputs.
3. Ground the Chip Enable.
4. Address the desired location by applying ground (i.e., 0.4V maximum) for a "0", and +5.0V (i.e., +2.8V minimum) for a "1" at the address input lines.
5. Apply +12.5V ± 0.5V to the output to be programmed through a 390 ohm ± 10% resistor. Program one output at a time.
6. Apply +12.5V to V_{CC} (pin 16) for 50 msec to 1sec (max.) with a V_{CC} rise time of 50μsec or less. If 1.0 second is exceeded, the duty cycle should be limited to a maximum of 25%. The V_{CC} overshoot should be limited to 1.0V maximum. If necessary, a clamping circuit should be used. The V_{CC} current requirement is 40 mA maximum at +12.5V. Several fuses can be programmed in sequence until 1.0 sec of high V_{CC} time is accumulated before imposing the duty cycle restriction.

   NOTE: Normal practice in test fixture layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A capacitor of 10 microfarads minimum, connected from the +12.5V to ground, should be located close to the unit being programmed.
7. Remove the programming voltage from pin 16.
8. Open the output.
9. Proceed to the next output and repeat, or change address and repeat procedure.
10. Continue until the entire bit pattern is programmed into your custom 8223.

Fast Programming Procedure – Programming Procedure B

1. Remove V_{CC} (open or ground pin 16).
2. Remove any load from the output.
3. Ground $\overline{CE}$ (pin 15).
4. Address the word to be programmed by applying 5 volts of a "1" and ground for a "0" to the address lines. (Solid TTL logic levels are ok, but we suggest buffer drivers or Utilogic OR/NOR gates for the addressing).
5. Apply +12.5V ± 0.5V to the output to be programmed through a 390 ohm ± 10% resistor. Program one output at a time.
6. Apply +12.5V to V_{CC} (pin 16) for 25-50mS. The V_{CC} rise time must be 50μsec or less. Limit the V_{CC} overshoot to 1.0 volts max.
7. Reduce V_{CC} to ground (< 0.5V) and remove the load from the output.
8. Immediately repeat steps 5 and 6 for other outputs of the same word, or repeat 4 through 6 for a different word. Continue programming for a max of 1 second. Then remove power for 4 seconds and continue until the entire bit pattern is programmed.

After programming the 8223, the unit should be checked to insure the code is correct. If additional fuses must be opened, they may be programmed during verification.

Fast Programming Procedure – Programming Procedure C

Steps 1 through 5 are the same as in Procedure B.

6. Apply a 5mS pulse to V_{CC} (pin 16). Limit the V_{CC} overshoot.
7. Reduce V_{CC} to 5 volts for 10-15uS and verify the fuse opened (output is now a "1". If the bit programmed go on to the next bit to be programmed. If the bit did not program, then reduce V_{CC} to ground (or open) for 1-5uS and repeat step 6 and 7 until the fuse programs (1 second total time max).
8. Continue programming at this rate for 1 second. Remove all power from the device for 4 seconds then continue programming procedure.

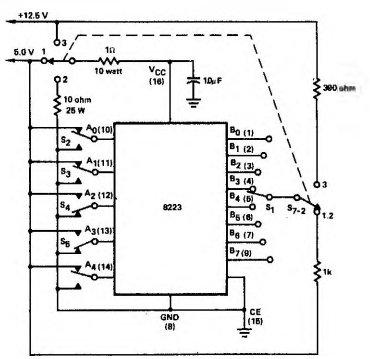
V_{CC} Waveform

BOARD LEVEL PROGRAMMING PROCEDURE FOR THE 8223

The chip select controls which 8223 is being programmed when several PROMS are collector OR'd. To program in this manner, the only changes required are:

1. The 390 ohm resistor is reduced to $\frac{200 \text{ ohm}}{N}$ where N is the number of outputs tied together ($2 \leq N \leq 12$).
2. Reduce max fuse pulse width from 1 second max to 0.92 sec max.

MANUAL PROGRAMMER DIAGRAM



S_1 = Single pole 9 position switch

S_2 through S_6 = single pole 2 position switch

S_7 = Two pole 3 position switch with ground connected to the middle position of the section connected to V_{CC}, pin 16 to go from 5 volts to 12.5V the switch will momentarily ground V_{CC}) and positions 1 and 2 of the other section connected to 5.0V to provide the needed 5 volts to the output for verification.

NOTE:
1. The 10μf capacitor across pin 16 to ground is required to eliminate noise from V_{CC}.
2. During programming switch S_7 must be in position 2 long enough for the 1.0μf capacitor to discharge to less than 0.5 volts.